# TMPZ84C10AP-6 / TMPZ84C10AM-6 / TMPZ84C10AT-6
# CMOS-Z80 DMA : DIRECT MEMORY ACCESS CONTROLLER

## 1. GENERAL DESCRIPTION AND FEATURES

TMPZ84C10A (hereinafter referred to as DMA) is the CMOS Z80 DMA (Direct Memory Access Controller) which provides low power consuming but powerful and versatile operations.

This DMA is designed to improve system performance by allowing the system memory and peripheral LSI's to directly transfer data between them.
Memory-to-memory and I/O-to-I/O (I/O devices as peripheral LSI or I/O devices such as printer, etc.) data transfer capability is also provided.

The TMPZ84C10A is fablicated using Toshiba's CMOS Silicon Gate Technology. The principal functions and features of the TMPZ84C10A are as follows.

(1) Compatible with the Zilog Z80 DMA.

(2) DC to 6MHz operatio

(3) Single 5V power supply (at 5V ± 10%)

(4) Data transfer rate 3M bytes/sec (at 6MHz)

(5) Data transfer in max. 64K byte block length.

(6) Address generation with incrementing, decrementing, or fixed address by source and destination.

(7) Built-in daisy chain structure interrupt circuit.

(8) Low power consumption
10μA MAX (5V, stand-by)

(9) Extended operating temperarure
−40℃ to 85℃

(10) Transfer, search, or transfer/search operations can be specified.

(11) Byte, burst or continuous modes can be specified.

(12) Bit maskable byte searching function.

(13) Built-in Reset logic that is synchronized external signal, Software and when powered on.

Further, in the following text and explanations for charts and tables, hexadecimal numbers are directly used without giving an identification to explanation of address, etc. to the extent not to cause confunctions.

Note : Z80 is a trademark of Zilog Inc., U.S.A.

# 2. PIN ASSIGNMENTS AND PIN FUNCTIONS

The pin assignments and I/O pin names and brief functions of the TMPZ84C10A are shown below.

## 2.1 PIN ASSIGNMENTS

The pin assignments of the TMPZ80C10A are as shown in Figure 2.1, Figure 2.2.

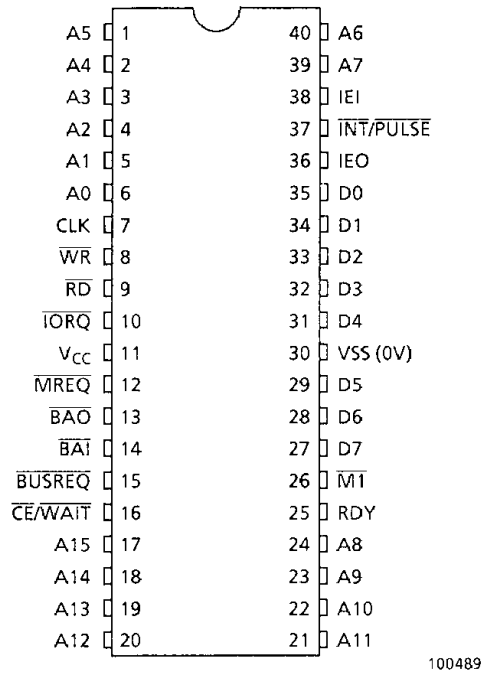


Figure 2.1 DIP, SOP Pin Assignments

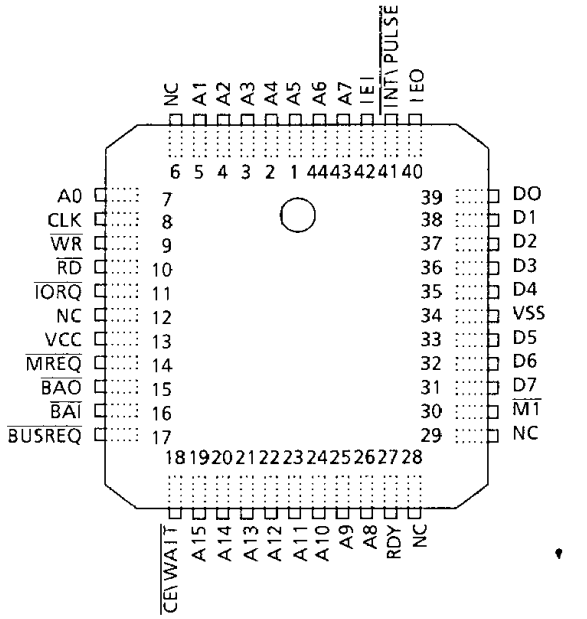


Figure 2.2 PLCC Pin Assignments

## 2.2 PIN NAMES AND FUNCTIONS

Table 2.1 Pin Names and Functions (1/2)

| Pin Name | Number of Pin | Input/Output 3-state | Function |
|---|---|---|---|
| A0~A15 | 16 | Output 3-state | 16-bit address bus.<br>DMA output address bus to source port and destination port. |
| CLK | 1 | Input | Single phase clock signal.<br>Clock input to DMA. The same clock as that for MPU can be used. |
| $\overline{WR}$ | 1 | I/O 3-state | Write signal.<br>When used as input, MPU writes to DMA control register. When used as output, DMA controls write to the memory or I/O port address. |
| $\overline{RD}$ | 1 | I/O 3-state | Read signal.<br>When used as input, MPU reads out of DMA status register. When used as output, DMA controls read from the memory or I/O port address. |

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Table 2.1 Pin Names and Functions (2/2)

| Pin Name | Number of Pin | Input/Output 3-state | Functions |
|---|---|---|---|
| $\overline{IORQ}$ | 1 | I/O 3-state | I/O request signal. When I/O data is read or written, DMA controls read/write. |
| $\overline{MREQ}$ | 1 | Output 3-state | Memory request signal. When memory data is read or written, DMA controls read/write. |
| $\overline{BAO}$ | 1 | Output | Bus line enable output signal. In the several DMA configuration, controls priority for the bus using right. |
| $\overline{BAI}$ | 1 | Input | Bus line enable input signal. Indicates that the system bus using right is released for DMA control. |
| $\overline{BUSREQ}$ | 1 | I/O | Bus line enable input signal. Indicates that the system bus control are sent to MPU. Open drain. |
| $\overline{CE/WAIT}$ | 1 | Input | Chip enable/wait signal. Normally, operates as $\overline{CE}$ but it is possible to program to operate as $\overline{WAIT}$ at time of data transfer. |
| RDY | 1 | Input | Ready signal. Monitored by DMA to determine effective polarity. Effective polarity is programmable. |
| $\overline{M1}$ | 1 | Input | Signal showing machine cycle 1. Indicates that MPU is in the operation code fetch cycle or interruption acknowledge. |
| D0-D7 | 8 | I/O 3-state | 8-bit bidirectional data bus. Control byte from MPU, status byte from DMA and data from the memory or I/O are transferred through these terminals. |
| IEO | 1 | Output | Interrupt enable output signal. Using jointly with IEI, forms the daisy chain structure for interrupt priority when several peripheral LSI's are connected. |
| IEI | 1 | Input | Interrupt enable input signal. Using jointly with IEO, forms the daisy chain structure for interrupt priority when several peripheral LSI's are connected. |
| $\overline{INT}/\overline{PULSE}$ | 1 | Output | Interrupt request signal. For interrupt request and pulse generation. Open drain. |
| VCC | 1 | Power supply | + 5V |
| VSS | 1 | Power supply | 0V |

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# 3. DESCRIPTION OF OPERATION

## 3.1 BLOCK DIAGRAM

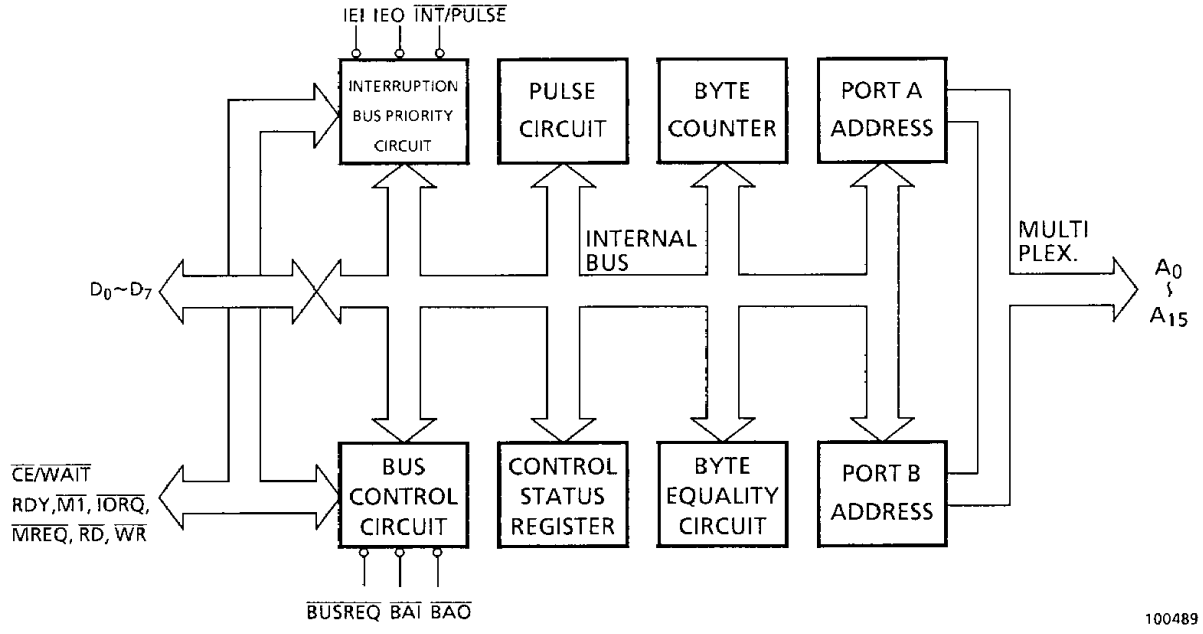


Figure 3.1 Block Diagram

## 3.2 SYSTEM CONFIGURATION

The architecture (system configuration and functions) which must be known in using DMA will be described here.

Components

(1) Reset circuit
(2) Control & status register group
(3) Bus control circuit
(4) Pulse circuit
(5) Byte counter
(6) Byte equality circuit
(7) Port A address, Port B address
(8) Interrupt priority circuit
(9) Basic function
(10) Interrupts

3.2.1 Reset logic

DMA has following three reset functions.

(1) Power on reset

DMA has reset circuit that is synchronized automaticaly when powered on.

(2) External signal reset

When $\overline{M1}$ signal is active more than two system clocks without an active $\overline{RD}$ or $\overline{IORQ}$ signal, the DMA is reset at rising edge of $\overline{M1}$ signal.

(3) Soft ware reset

3.2.2 Control & status register group

The DMA is provided with 21 writable register control register group and 7 readable register status register group. Registers are all in 8 bits but 2 byte data is held in optional 2 continued registers. The Z80 Microprocessor (hereinafter referred to as MPU) is capable of setting and monitoring values in respective registers.

The control register group is classfied into 7 groups of WR0 to WR6 (Figure 3.2), each of which is consisting of the basic register and related registers. The operation of DMA is controlled by programming in the control register group.

The status regiser group consists of PR0 to PR6 (Figure 3.3) and are used to know state of execution or end of DMA operation.

Further, these registers are described in detail in 3.4 Commands.

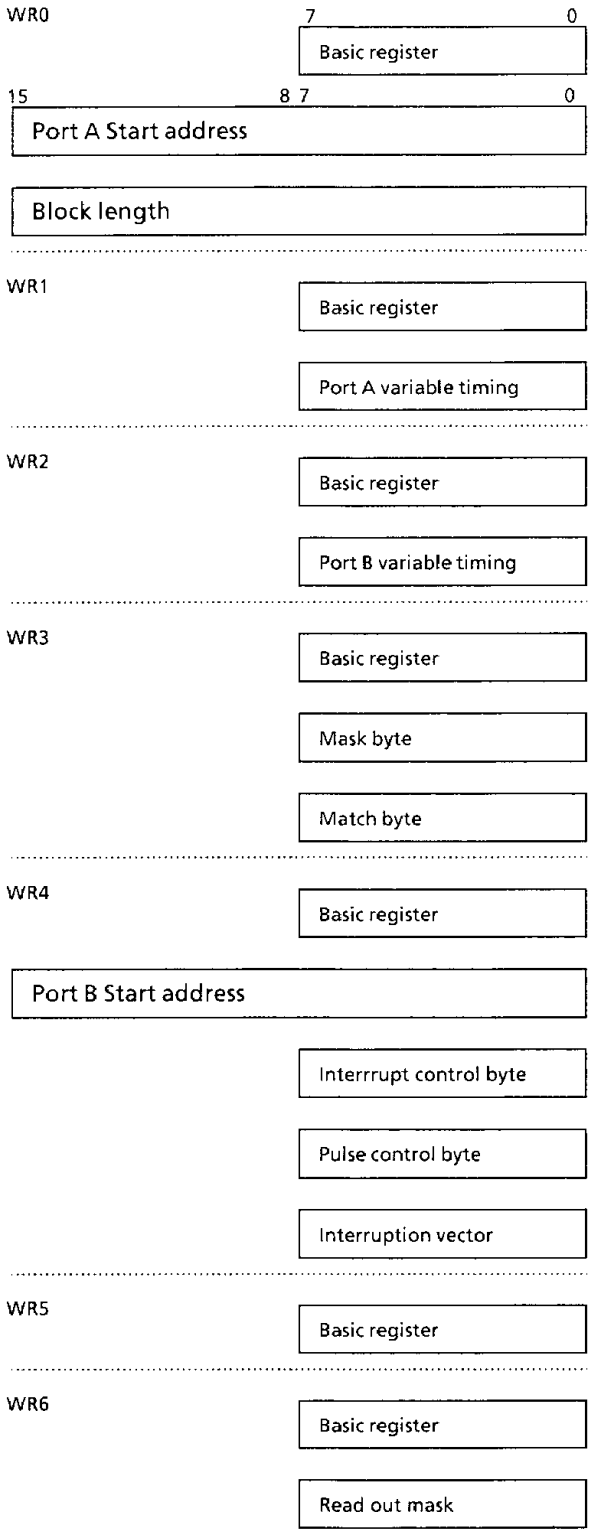


Figure 3.2 Control Register

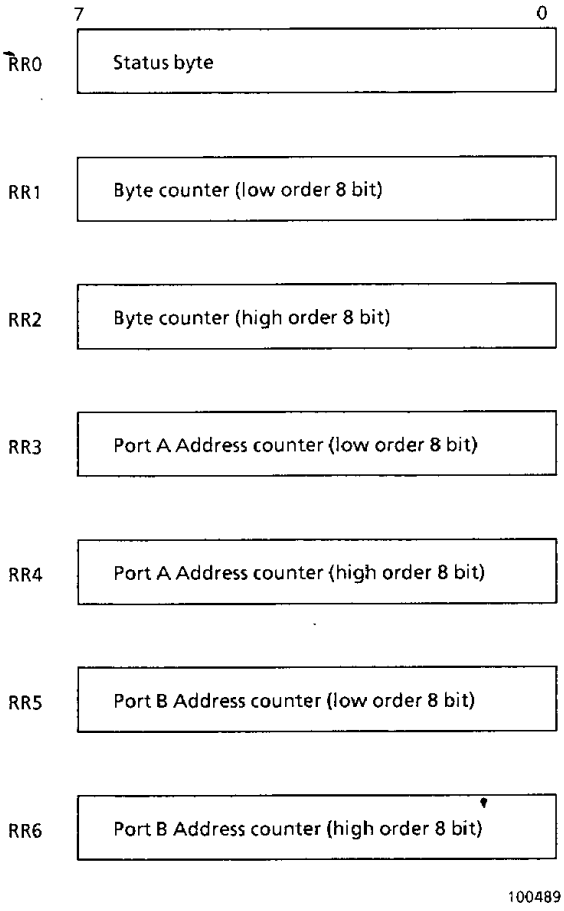


Figure 3.3 Status Register

### 3.2.3 Bus control circuit

The bus control circuit controls bus direction between DMA and system bus at time of programming, while controls the control bus at time to data transfer according to the data transfer direction between the memory and I/O devices. In addition, it controls updating of required address counter and byte counter.

(1) Bus direction control

- At time of programming, the bus master is MPU and the control bus and data bus (when data is written into the control regiser) are in the direction from the system bus to DMA. Further, when data (status, etc.) is read from the control register, the direction will be from DMA to the system bus. At this time, the address bus buffer is disabled.
- At time data transfer, the bus master is DMA. The control bus buffer and address bus buffer are enabled, and the bus direction will become from DMA to the system bus.
- When data is read out of the memory or I/O device, the data bus direction is from the system bus to DMA but it becomes in the direction from DMA to the system bus at time of data write.

(2) Bus request

If DMA requested MPU to transfer the bus control right and received it, MPU cannot fetch commands from the memory and is placed in the completely idle state.

For DMA to request the bus control right to MPU, following 2 enable conditions are required:

(a) Enable command from MPU

(b) Active RDY condition

### 3.2.4 Pulse circuit

The pulse circuit generates pulse signals in the INT line for every 256 bytes of 0 to 255 when data transfer is started. The details are described in 3.3.2 (2) (k).

### 3.2.5 Byte counter

The byte counter is cleared when data is transferred and is incremented by one whenever data is transferred for every 1 byte. A value of this counter is always compared with block length of WR0 and when they agree with each other, the DMA operation ends.

### 3.2.6 Byte equality circuit

DMA always monitors data being transferred during the data teansfer and when equality is detected, generation of interruption becomes possible.

3.2.7 Port A address, Port B address

Data transfer is performed between Port A and Port B. Either port is specified by the source and destination specified by WR0.

3.2.8 Interrupt priority circuit

The Z80 system used the daisy chain structure to control interrupt among peripheral LSI's and the bus priority among multiple DMA's.
Further, for the interrupt timing, refer to 3.2.2 (2) (j).

(1) Interrupt daisy chain

When the interrupt priority is connected in the daisy chain structure, connect IEI and IEO. When the interrupt is acknowledged, the interrupt configuration of MPU is disabled. In order to allow other peripheral LSI to make the interrupt into MPU, it is necessary to enable the MPU's interrupt configuration by the interrupt enable command. The interrupt enable command is normally executed in the service routine. When the interrupt enable command is executed in the early part of the service routine, a peripheral LSI with higher priority can make the interrupt even when MPU is executing the service routine. (Interrupt in the nest structure is authorized.)

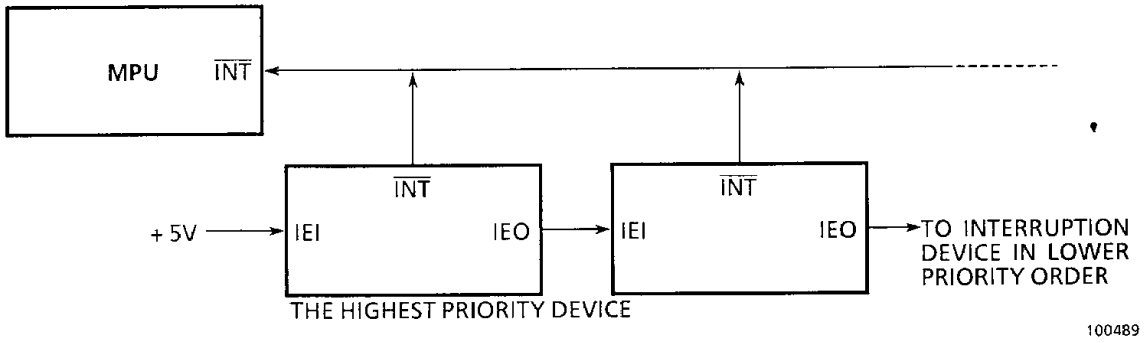


Figure 3.4 Interruption Daisay Chain

(2) Bus request daisy chain

When multiple DMA's are used, priority can be controlled by the daisy chain structure connection. Since $\overline{\text{BUSREQ}}$ signal of each DMA is bidirectional type, each DMA in the daisy chain is able to know bus requests as an input and until a DMA having the bus completes its operation, the bus requests of other DMA's are kept in wait state. Until completion of the operation, any DMA is not able to release the bus in operation by force. Further, the bus request daisy chain has no nesting function but is able to hold the bus until its process is completed. The priority among DMA 's in the daisy chain is in order from high order to low order corresponding to distances drom MPU. Priority is so decided that low order DMA will not receive $\overline{\text{BUSACK}}$ signal through $\overline{\text{BAI}}/\overline{\text{BAO}}$ chain of DMA when multilpe DMA's made the bus request in the same clock cycle period.

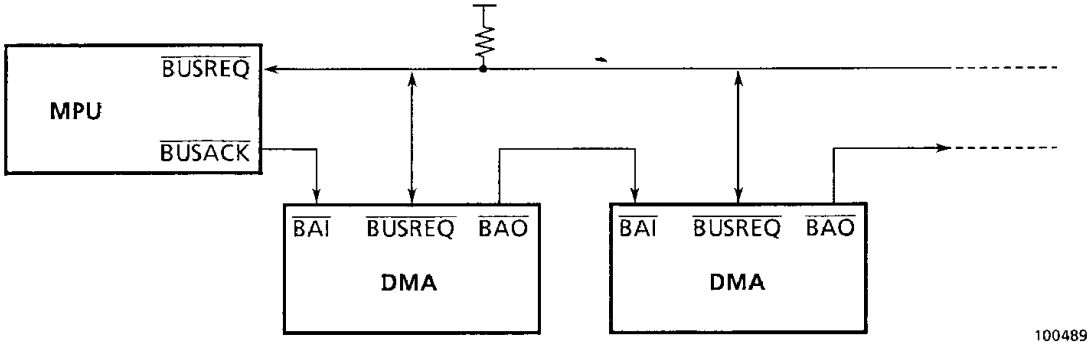


Figure 3.5 BUS REQUEST Daisy Chain

3.2.9 Basic functions

DMA is provided with the following basic functions:

(1) Data transfer paths

① Transfer between memory and I/O
② Transfer between memories
③ Transfer between I/O and I/O
④ Memory search
⑤ I/O search

(2) Operating classes

(3) Operation modes

① Byte mode
② Burst mode
③ Continuous mode

(4) Transfer speed

(5) Operating conditions

(6) Automatic restart

(7) Variable cycle

(8) Pulse generation

3.2.9.1 Data transfer paths

The data transfer paths of DMA are as shown in Figure 3.6.

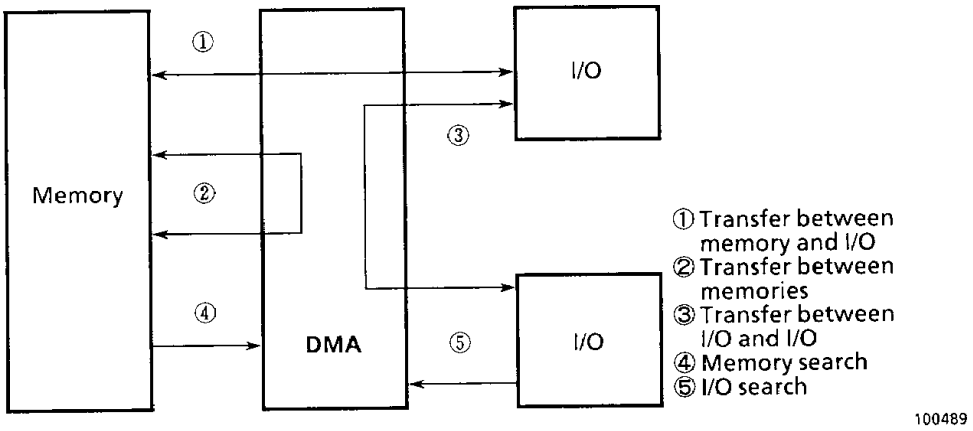


Figure 3.6 Transfer Paths of DMA

(1) Transfer between memory and I/O

This is the most ordinary method of data transfer and data transfer with the high speed serial interfaces (Z80SIO, etc.) is possible.

(2) Transfer between memories

This method of transfer is used for relocation of the memory content and high speed transfer of voluminous data between memories. In addition, this method is used to support memory mapped I/O. It is possible to program to make RDY conditions active for this type of data transfer.

The same function as that of LDIR command (block transfer command) of the Z80 MPU is provided. Number of clocks required by MPU for transfer of data of single byte is 21 clocks in case of the LDIR command while it can be processed in 4 clocks when DMA is used (in case of 2 cycle variable timing). Further, when DMA is used, approx. 420 clocks are required for initialization but in transfering data of 25 bytes or above, DMA becomes advantageous.

(3) Transfer between I/O and I/O

This method of transfer can be used in such applications as acquisition of real time data requiring temporary storage of input data. For instance, in transfering data from a diskette to a line printer, a program only starts the DMA operation and data is transferred from I/O to I/O. However, if I/O error occurred, its recovery becomes necessary.

Further, when there is a byte equality, it is possible to branch into various operations by the search function.

(4) Memory search

This memory search is used to search a large quantity of data at high spped. The same function as that of CPIR command (search command) of the Z80 MPU is provided. Number of clocks required by MPU for single byte memory search is 21 clocks when the CPTR command is used while the search is possible in 2 clocks ( in case of 2 cycle variable timing) when DMA is used. Further, approx. 376 clocks are required for initialization when DMA is used and therefore, DMA is advantageous for memory search of more than 19 bytes. In addition, the search of special bytes in the end of block and character check block is also possible.

(5) I/O search

This is used for search of special bytes in the end of block and character check block. For instance, this is used for search of a file mark showing a file delimiter on a magnetic tape.

3.2.9.2 Operating classes

There are 3 kinds of basic operation classes for DMA. 2 out of these 3 kinds are further devided into 2 classes. In addition, the ports referred to here denote the data source and destination.

(1) Data transfer between 2 ports

① Transfer

Data transfer path in the flow of readout cycle followed by write cycle. This is executed without external logic circuit between DMA and MPU.

② Simultaneous transfer

Data transfer path for simultaneous read and write of data transferred between ports by generating required control signal through use of an external logic circuit. 2 times of effeciency of the transfer only class is obtained.

(2) Search of special bit pattern in byte at one port

① Search

This is a method to search special bit pattern by comparing data read from the source port with a matched byte. The matched byte is masked by another byte and can be compared with a special bit pattern (a certain bit in bytes).

(3) Data transfer between 2 ports and search

① Transfer/search

Data transfer is performed in the same transfer method as that of the only transfer class and at the same time, the same search as that for the search only class is performed.

② Simultaneous transfer/search

Data transfer is performed in the same transfer method as that of the simultaneous transfer class and at the same time, the same search as that for the search only class is performed.

In this case, an external logic circuit is required.

### 3.2.9.3 Operation modes

In the transfer methods for various operation classes, DMA can select the following modes:

- Byte mode
- Burst mode
- Continuous mode

The single byte transfer/search is shown in Figure 3.7 (commonly applicable to all modes).

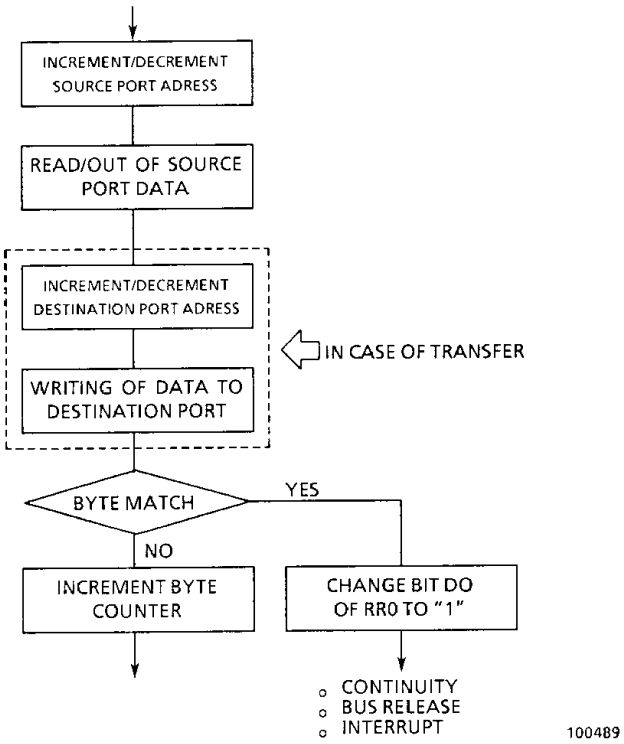


Figure 3.7 Single Byte Transfer/Search

The data transfer is started at the point of time when DMA is enabled. In the first single byte operation in any mode, RDY signal is first checked to determine if it is active.

Then, the bus request is made and single byte transfer/search is performed when DMA becomes the bus master. The same operation is continued until the end of block judgement is made. If it is not the end of block, however, a different operation is carried out after judgement of RDY signal. The operations in respective modes are as shown in Figure 3.8, 3.9 and 3.10.

(1) Byte mode

In the data transfer operation of DMA, the system bus control right is released whenever 1 byte is transferred at a time and the system bus control right is returned to MPU for at least one machine cycle period.

If RDY signal of DMA is active when one machine cycle passes after the system bus control right is returned to MPU, the bus request is made again to MPU and next one byte data transfer is performed. Further, when RDY signal is non-active, the system bus control right is retained by MPU. This operation is shown in Figure 3.8.

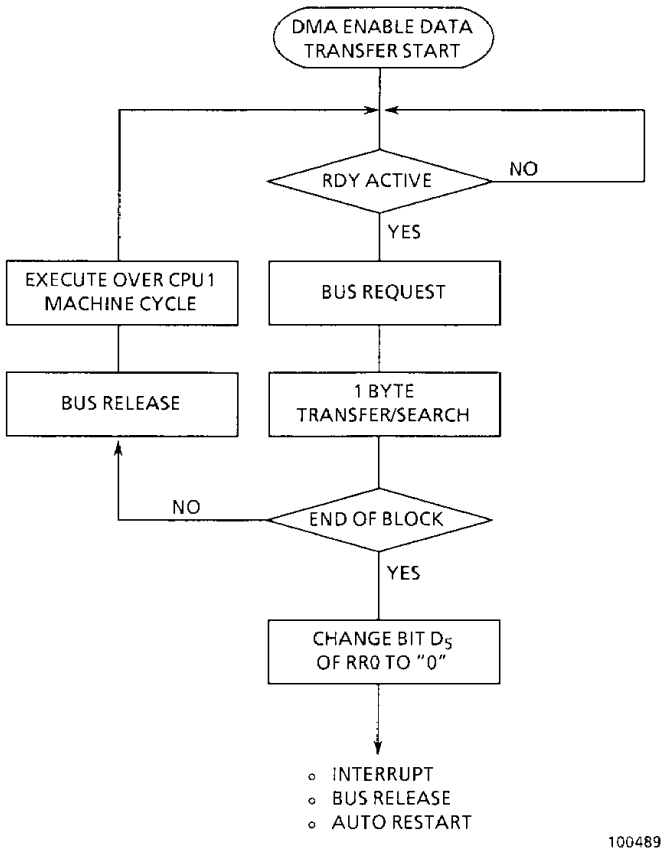


Figure 3.8 Byte Mode

(2) Burst mode

In the burst mode, after one byte data is transferred, RDY signal is checked to determine if it is active without releasing the system bus control right. If RDY signal is active, data transfer is continued until RDY signal becomes non-active and after the data transfer is completed, DMA stops to operate. Since MPU is ready to operate during the period in which I/O device does not transfer data (when RDY signal is non-active), data transfer rate and bus using efficiency are effective.

This operation is shown in Figure 3.9.

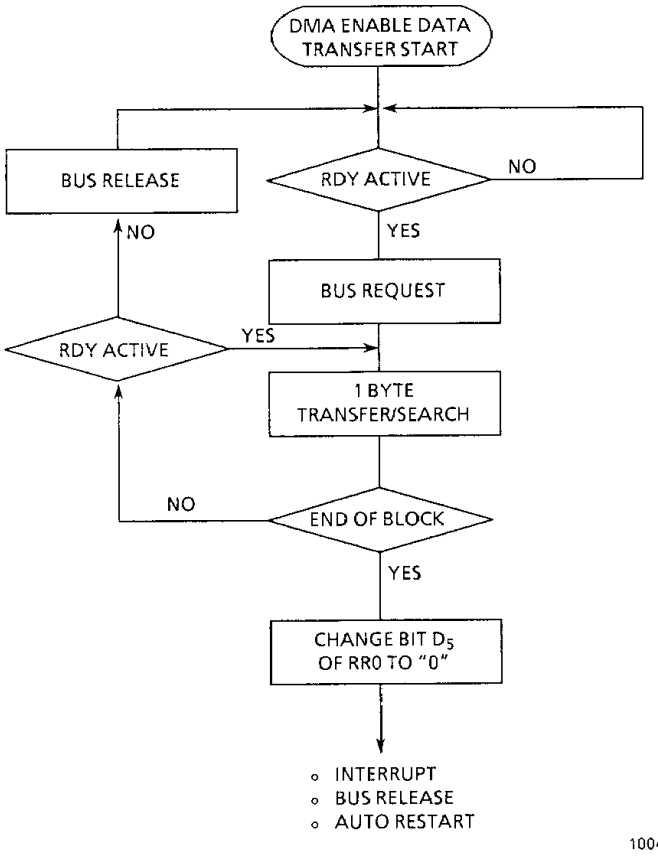


Figure 3.9 Burst Mode

(3) Continuous mode

When the data transfer is commenced, DMA retains the system bus control right until the transfer of last byte of a data block is completed or the stop condition of RDY signal becomes non-active during the operation, DMA is simply put in the idle state and still retains the system bus control right while waiting that RDY signal becomes active again. What must be taken care of is that if number of data bytes is smaller than that set in the byte counter, DMA cannot end the block transfer forever and the system is impeded to operate properly.

This operation is shown in Figure 3.10.

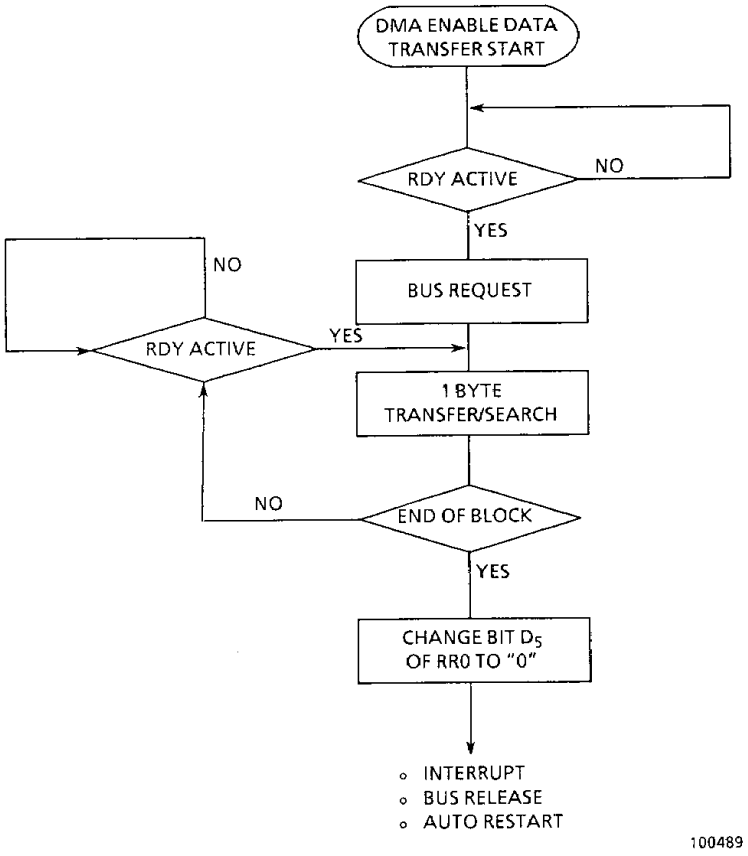


Figure 3.10 Continuous Mode

### 3.2.9.4 Transfer speed

Shown in Table 3.1 are the comparison of max. transfer rates in 5 transfer classes of DMA operation and that of max. transfer rates in block transfer command of MPU. The max. speed transfer rate is accomplished in the simultaneous transfer operation of DMA and at least one external logic circuit is required. DMA transfers shown in the table are based on the assumption that interruption is not involved in the burst or continuous mode, and that the read and write cycle is 2 cycles.

Table 3.1 Transfer and Search Max. Speed (Burst and continuous modes)

| Operation | Z – 80 (6.0MHz) |
|---|---|
| Simultaneous transfer of DMA<br>DMA search only<br>Simultaneous transfer/search | 3M byte/s |
| DMA transfer<br>DMA transfer/search | 1.5M byte/s |
| Block transfer command of MPU | 0.300M byte/s |

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Shown in Table 3.2 is the comparison of the Z80 throughput reduction rate (per transfer K baud) in the byte mode of data transfer by DMA with the throughput reduction rate in the byte transfer using the interrupt service routine by six commands (actual minimum) by MPU. The DMA transfer in this data is based on the assumption that read and write cycle timing is longer than 2 cycles (min.). Therefore, MPU throughput reduction rate in the 2 cycle simultaneous transfer is further reduced.

Table 3.2 Z-80 MPU Throughput Reduction Per DMA Transfer K Baud (Byte Mode)

| Operation | Z – 80 (6.0MHz) |
|---|---|
| DMA transfer<br>DMA transfer/search | 0.027% |
| MPU transfer by interrupt | 0.142% |

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### 3.2.9.5 Operating conditions

Programmable conditions to get DMA perform certain operations and these operations are shown in Table 3.3. The conditions referred to here are those conditions for the internal registers of DMA, signals from peripheral LSI's and commands to DMA on the data bus. For details refer to Table 3.3.

Table 3.3 Operating Conditions

| Conditions | Operations that can be caused under conditions at left hand |
|---|---|
| End of block | a. Bus release<br>b. MPU interruption<br>c. Auto restart |
| Coincidence of byte | a. Bus release<br>b. MPU interruption<br>c. Continuation |
| Pulse control byte coincided with low order byte of byte counter | a. Pulse generation |
| RDY signal is active | a. Bus request<br>b. MPU interruption |
| RDY signal is non-active | a. Bus release<br>b. Breaking<br>(in case of continuous mode) |
| RETI command (interruption return command from MPU) | a. Bus request |

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### 3.2.9.6 Auto restart

In DMA data transfer, it is possible to automatically clear the byte counter, load the content of the start address register on the address counter again and restart the data transfer at the end of block.

The automatic restart function can reduce a burden of software on MPU in the CRT refresh or repeating operation. In addition, it is possible to write different start address into the buffer register during the data transfer (when RDY signal is non-active and the bus is released during the data transfer in the byte mode or burst mode). At this time, it becomes possible to commence the automatic restart of data transfer from a new start address.

### 3.2.9.7 Variable Cycle

DMA is capable of changing readout and write cycle lengths through programming. This function is effective in increasing data transfer rate and reducing a burden on a software, and an external logic circuit may be omitted. Refer to 3.3.2 (2) (i) where this function is described.

### 3.2.9.8 Pulse generation

DMA generates pulse signal on the $\overline{INT}$ line for every 256 bytes for data transfer. This is described in detail in 3.3.2 (2) (k).

### 3.2.10 Interrupt

DMA is able to make an interrupt request to MPU under the following conditions:

- After DMA's RDY signal becomes active and before DMA makes a bus request ($\overline{BUSREQ}$="0")
- When the content of the byte counter coincides with that of the block length register and the end of block is detected.
- When the content of the coincided byte masked by the mask byte coincides with data in the transfer or search period when the byte coincidence is formed.

To make an interrupt request to MPU, it is necessary for DMA to release the bus. If DMA is the bus master, signal on the INT line generates periodic pulses to the peripheral LSI's, which are not sensed by MPU.
Therefore, at the end of block or after stop by byte coincidence, DMA releases the bus before interrupting MPU.

If interrupt at the enf of block and automatic restart at the end of block are set for DMA by programming, an interrupt is taken place at each end of block (at this point of time, it is acknowledged for the continuous operation). If the automatic restart is programmed in this case, the status flag at the end of block is not set. In this case, the interrupt vector cannot determine a factor for that interrupt.

On the Z80 system, interrupt is controlled through the daisy chain system. For the interrupt daisy chain, refer to 3.2.7 Interrupt/Priority Circuit. In addition, for the interrupt timing, refer to 3.3.2 (2) (j).

## 3.3 Status change flowchart and basic timing

The status change flowchart and the basic data transfer timing by DMA are shown here. The status change flowchart is shown in 3.3.1 and the basic timing in 3.3.2.

3.3.1 Status change flowchart

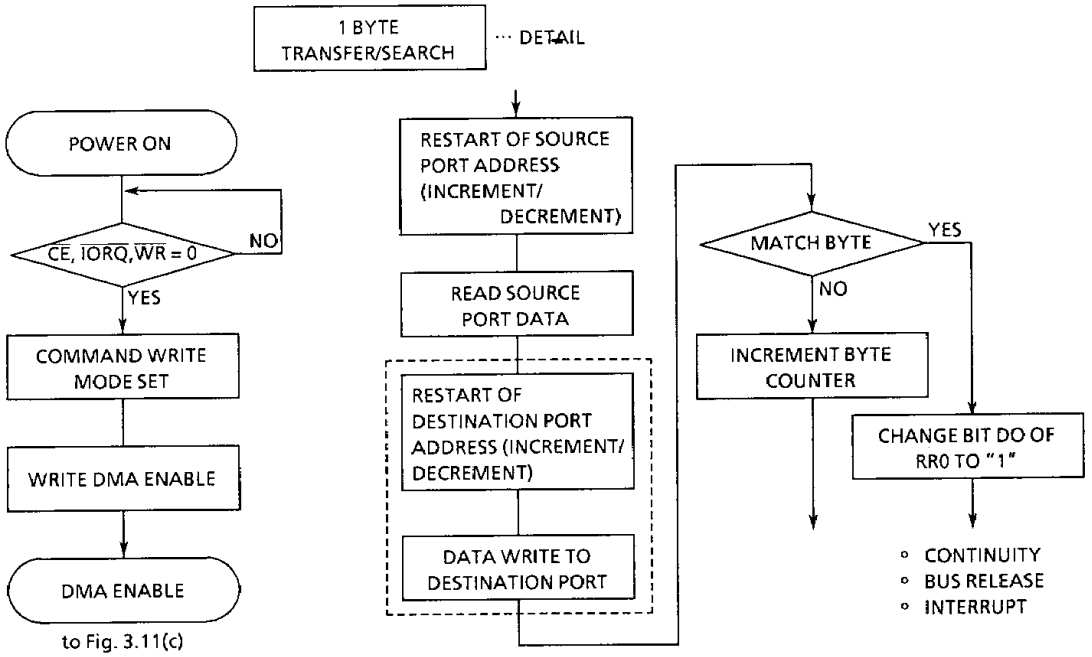
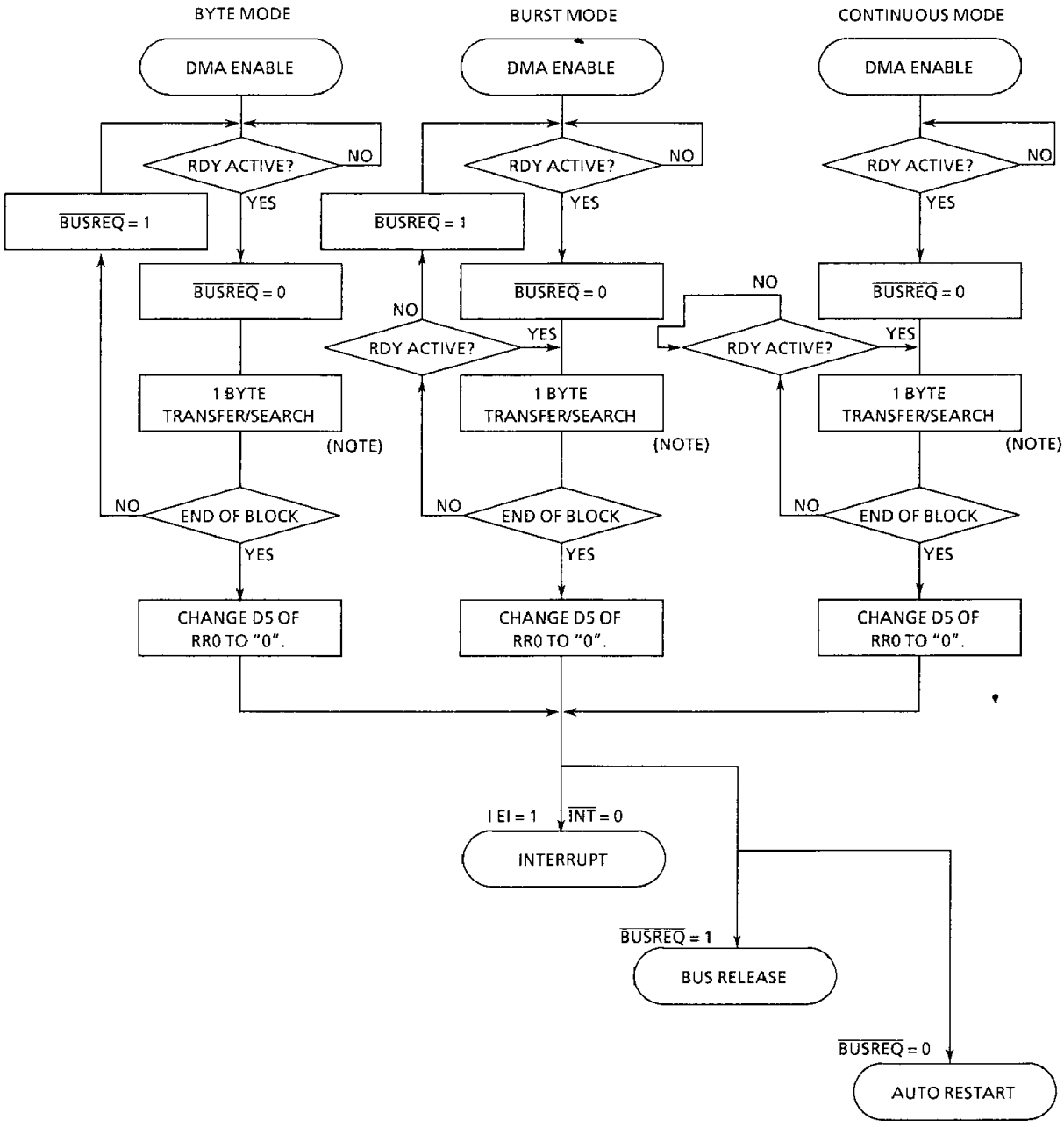



Figure 3.11 (a) Status Change Flowchart Figure 3.11 (b) Status Change Flowchart




Note : The details for signal byte transfer/search is shown in Figure 3.11 (b) Status Change Flowchart.

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Figure 3.11 (c) Status Change Flowchart

3.3.2 Basic timing

When DMA receives a command from MPU or reads the readout register, MPU has the system bus control right, $\overline{BUSACK}$="1", and MPU is called the bus master. When DMA operation is data transfer by DMA proper, $\overline{BUSACK}$="0", and DMA gets the system bus control right and becomes the bus master.

(1) When the bus master is MPU:

(a) Write timing into the write register

To write data into the write register, it is necessary for 3 signals of $\overline{CE}$, $\overline{IORQ}$ and $\overline{WR}$ to become "0" simultaneously at the rising edge of clock. At this leading edge, DMA latches these 3 signals. After latched, $\overline{CE}$, $\overline{IORQ}$ and $\overline{WR}$ signals may change to the invalid level after certain hold time. Further, DMA writes the status of the data bus (D0 to D7) into necessary write registers at the rising edge of next clock.

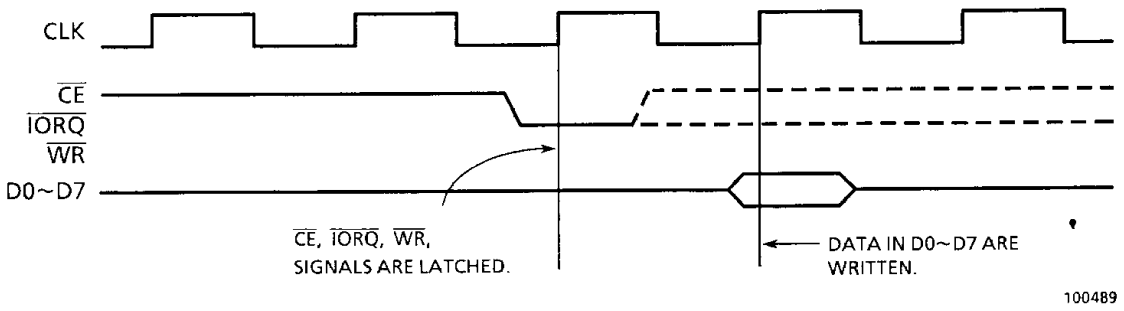



Figure 3.12 Write Timing into the Write Register of DMA

(b) Readout timing from the readout register

To readout the readout register it is necessary that 3 signals of $\overline{CE}$, $\overline{IORQ}$ and $\overline{RD}$ are at "0" and stable for more than 2 clocks. At the rising edges of 2 clocks, the status data is on the data bus and kept as long as $\overline{CE}$, $\overline{IORQ}$ and $\overline{WR}$ signals are active.

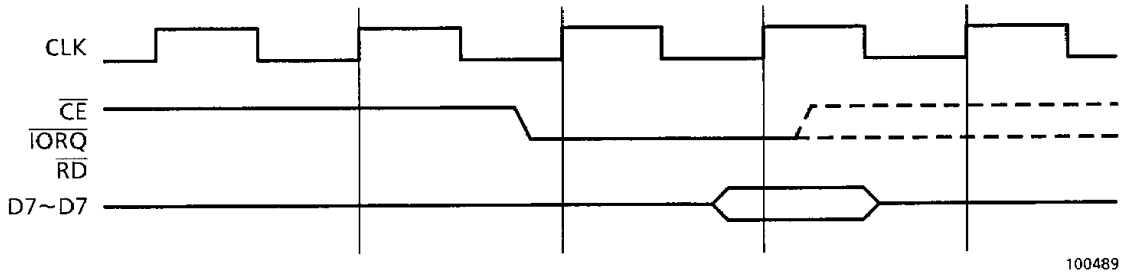



Figure 3.13 Readout Timing from the Readout Register of DMA

(2) When DMA is the bus master:

(a) Transfer

Transfer and transfer/search operations are performed at the same timing. Data is latched at the rising edge of $\overline{RD}$ signal (in case of the standard timing, the falling edge of T3 state) and held on the data bus during next write cycle. After $\overline{RD}$ signal becomes "1", the data bus buffer of DMA is enabled.

The standard timing is 3 clock cycles for the memory operation while it is 4 clock cycles for the I/O operation. In addition, in the I/O operation, the timing is 4 clock cycles including TW* which is automatically inserted between T2 and T3 state.

When $\overline{CE}/\overline{WAIT}$ signal is programmed as "Multiplex" in the write register WR5, DMA samples the status of this signal at the falling edge of T2 in case of the memory readout and at the falling edge of TW* in case of the I/O write. If $\overline{WAIT}$ signal is at "0" level at this time, DMA inserts one clock cycle (Tw) and if it is at "1" level, proceeds to next cycle. Further, when Tw is inserted, $\overline{WAIT}$ signal is sampled again during this period and the same processing is performed.

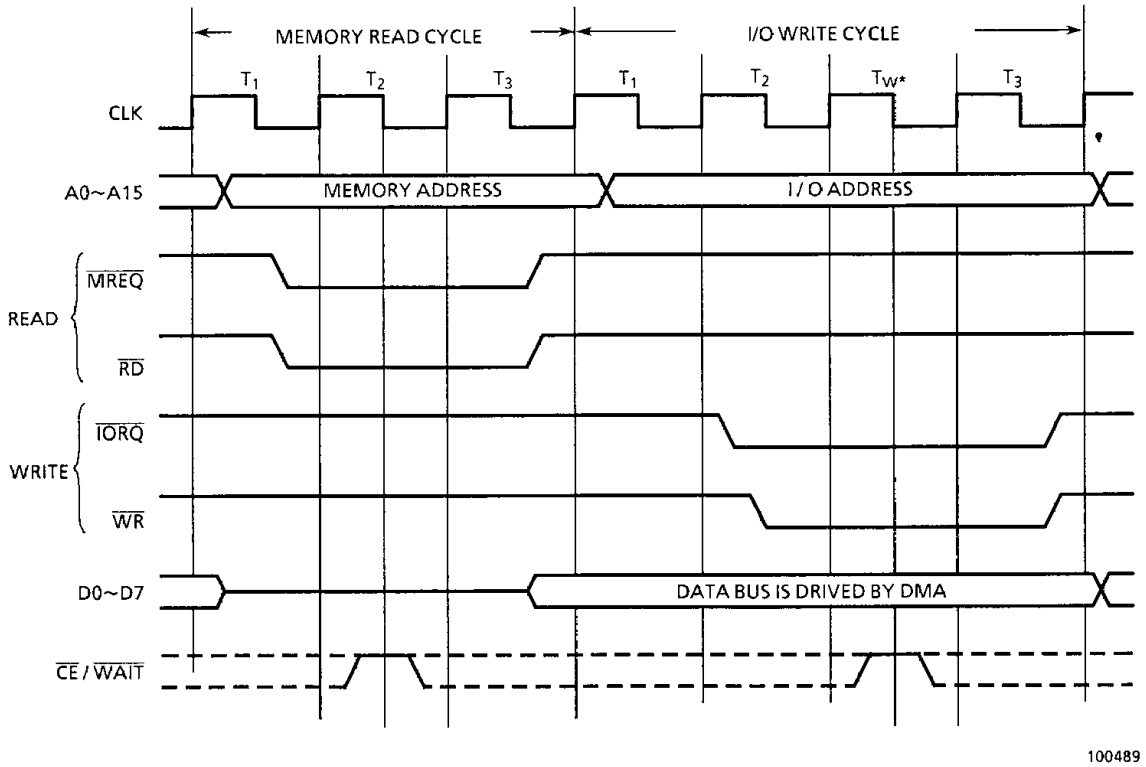



Figure 3.14 Transfer Standard Timing of Memory to I/O

- Memory to I/O

  In the memory readout, DMA put the memory address on the memory bus (A0 to A5) in the period of T1 rise and bring $\overline{MREQ}$ and $\overline{RD}$ signals to "0" level at the falling edge of T1 state. The memory data is read out at this point of time, put on the data bus (D0 to D7), latched by DMA at the falling edge of T3 immediately before the rise of $\overline{RD}$ signal, and when $\overline{RD}$ signal becomes "1" level, DMA data bus buffer is enabled and the latched data is output on the data bus.
  In the I/O write cycle, DMA put I/O address on the addresss bus in the T1 rise period, makes $\overline{IORQ}$ signal and $\overline{WR}$ signal to "0" level in the T2 rise period, and writes the data on the data bus (data readout from the memory) into I/O.

- I/O to memory

  In the I/O readout cycle, DMA put I/O address on the address bus in the T1 rise period and makes $\overline{IORQ}$ signal and $\overline{RD}$ signal to "0" in the T2 fall period. I/O data is read out and placed on the data bus at this time, and is latched by DMA at the trailing edge of T3 immediately before the rise of $\overline{RD}$ signal. When $\overline{RD}$ signal becomes "1" level, DMA data bus buffer is enabled and the latched data is output on the data bus.

  In the memory write cycle, DMA places memory address on the address bus in the T1 fall period, makes $\overline{MREQ}$ signal to "0" level at the falling edge of T1 and $\overline{WR}$ signal to "0" level in the T2 rise period, and write data on the data bus (data readout from I/O) into the memory.

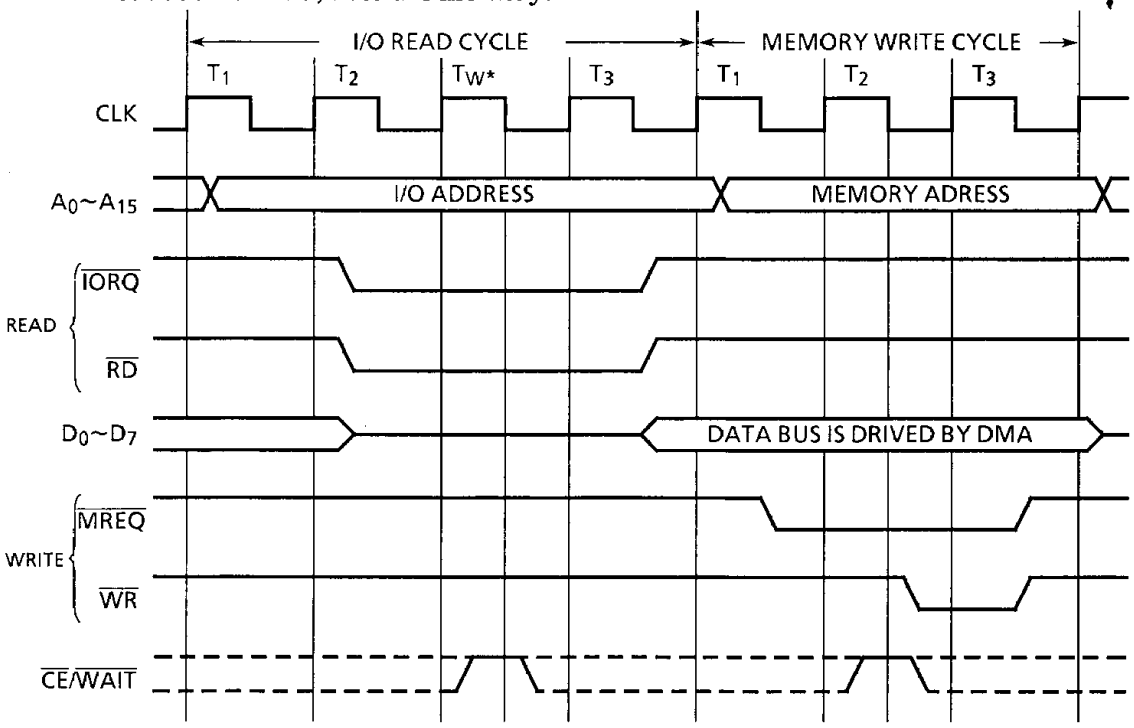



Figure 3.15 Transfer Standard Timing of I/O to Memory

- Memory to memory

  This operation is a combined operation of the memory read cycle and memory write cycle.

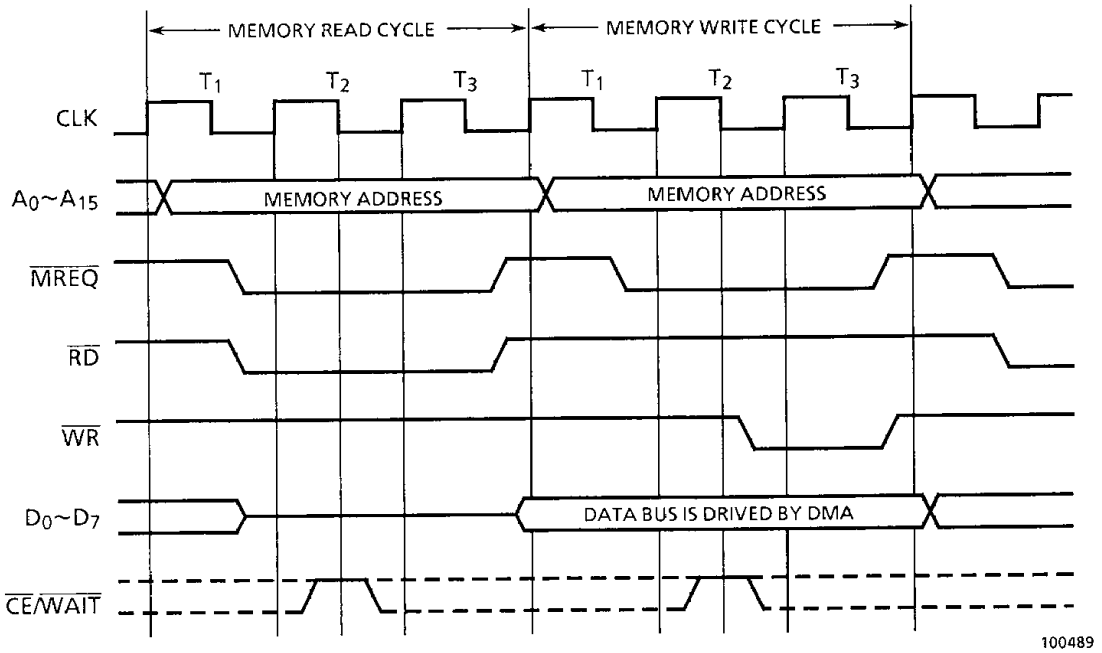



Figure 3.16 Transfer Timing of Memory to Memory

- I/O to I/O

  This operation is a combined operation of the I/O read cycle and I/O write cycle.

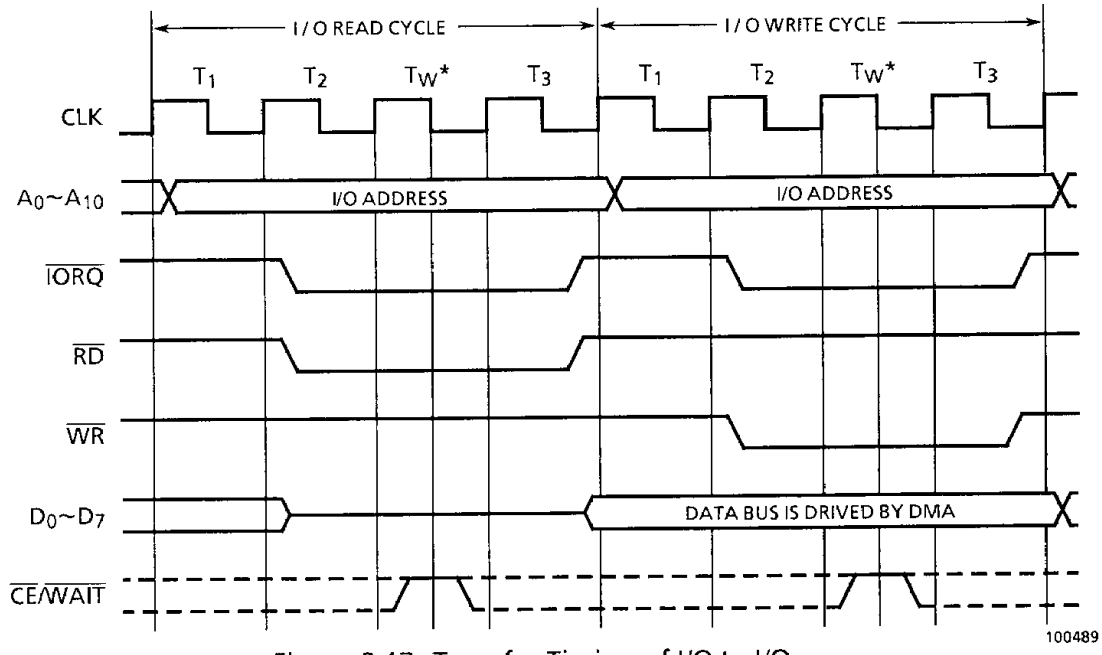



Figure 3.17 Transfer Timing of I/O to I/O

(b) Search timing

The search operation is identical to the readout only operation and data is only read into DMA register for comparison with coincided byte.

The timing of search operation is identical to that of memory to I/O transfer shown in Figure 3.14 and that of I/O to memory transfer in Figure 3.15.

(c) Simultaneous transfer

The simultaneous transfer operation and the simultaneous transfer/search operation are performed in the same timing.

When DMA is programmed in the search only mode, the read and write cycles are generated in one read cycle (source port readout period). Since only one address is generated on the address bus, the memory or I/O control signal is generated using an external logic circuit and DMA operation is performed according to this control signal. In addition, I/O ports are selected by hardware during the operation. Signals with (EXT) shown in Figure 3.18 through Figure 3.21 are those generated by an external logic circuit.

- Memory to I/O (Memory search cycle)

In this data transfer, the memory search mode is programmed and the memory readout and I/O write are performed in one read cycle by generating $\overline{\text{IORQ}}$ signal and $\overline{\text{WR}}$ signal in the memory readout cycle using an external logic circuit. The hardware performs the memory readout by $\overline{\text{MREQ}}$ signal and $\overline{\text{RD}}$ signal that are output by DMA and the I/O write by $\overline{\text{IORQ}}$ signal and $\overline{\text{WD}}$ signal that are generated using an external logic circuit.

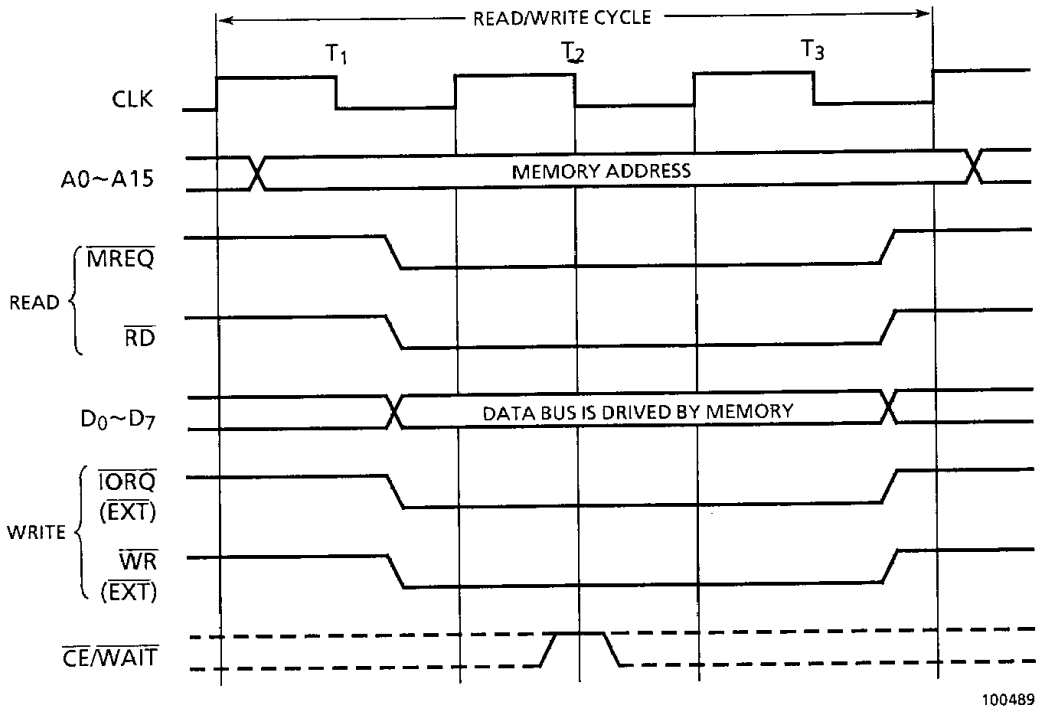



Figure 3.18 Simultaneous Transfer Timing of Memory to I/O (Memory search timing)

- I/O to memory (Memory search cycle)

  In this data transfer, the memory search mode is programmed and the I/O read and memory write operations are performed in one readout cycle by generating $\overline{IORQ}$ signal and $\overline{WR}$ signal in the memory readout cycle using an external logic circuit. The hardware performes the I/O readout using $\overline{RD}$ signal output by DMA and $\overline{IORQ}$ signal generated by an external logic circuit and the memory write using $\overline{MREQ}$ signal generated by DMA and WR signal produced by an external logic circuit.

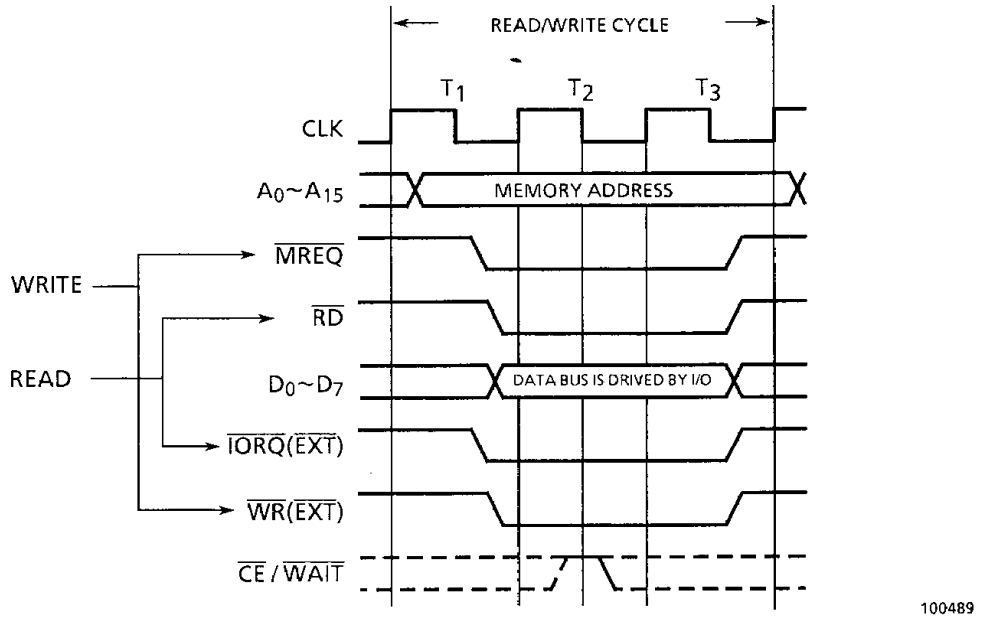


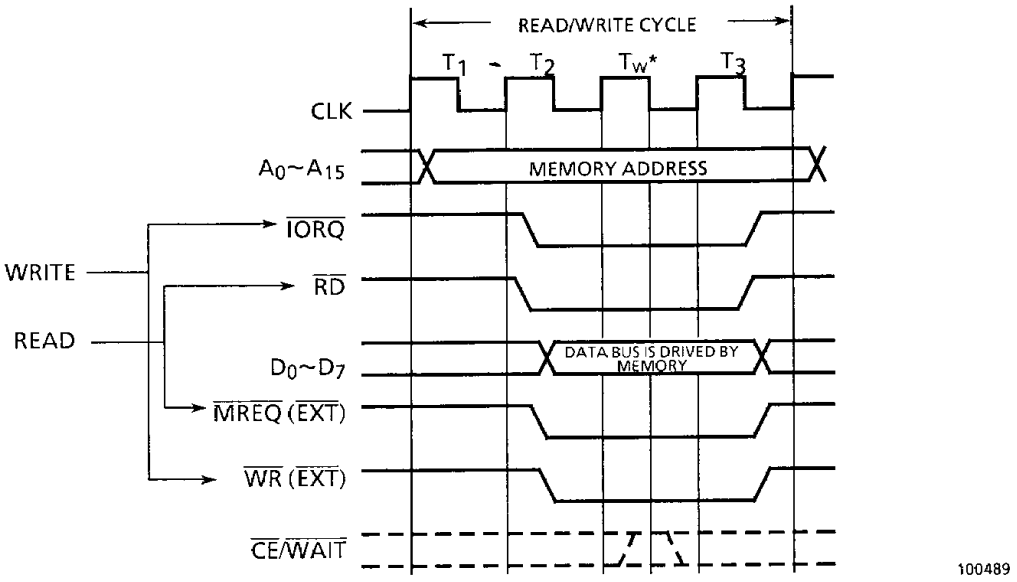

Figure 3.19 Simultaneous Transfer Timing of I/O to Memory (Memory search timing)

- Memory to I/O (I/O search cycle)

  In this data transfer, the I/O search mode is programmed and the memory read and I/O write operations are performed in one readout cycle by generating $\overline{\text{MREQ}}$ signal and $\overline{\text{WR}}$ signal in the I/O readout cycle using an external logic circuit. The hardware performs the memory readout using $\overline{\text{RD}}$ signal output by DMA and $\overline{\text{MREQ}}$ signal generated by an external logic circuit and the I/O write using $\overline{\text{IORQ}}$ signal generated by DMA and $\overline{\text{WR}}$ signal produced by an external logic circuit.

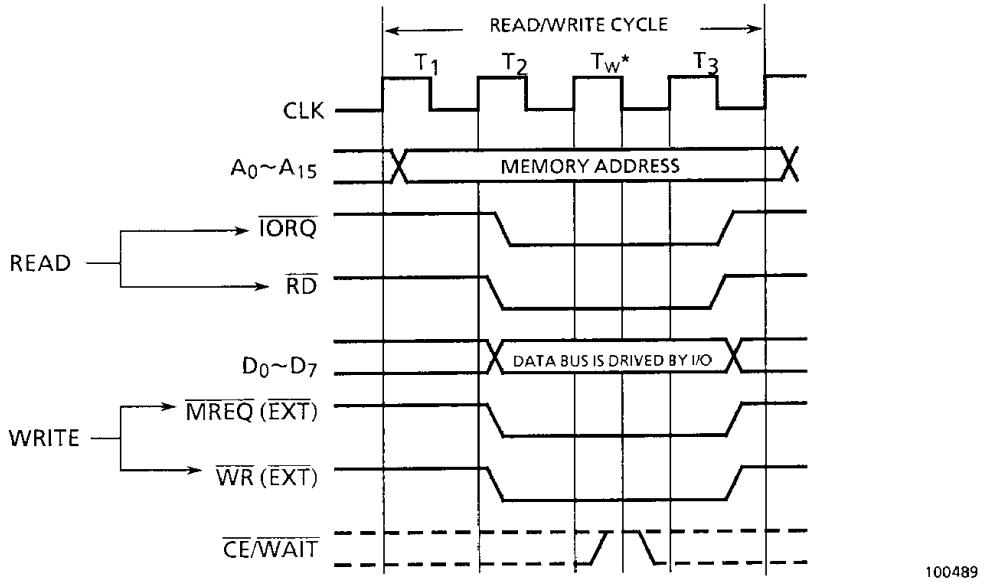
- I/O to memory (I/O search cycle)

  In this data transfer, the I/O search mode is programmed and the I/O read and memory write operations are performed in one readout cycle by generating $\overline{\text{MREQ}}$ signal and $\overline{\text{WR}}$ signal in the I/O readout cycle using an external logic circuit. The hardware performs the I/O readout using $\overline{\text{IORQ}}$ and $\overline{\text{RD}}$ signals output by DMA and the memory write using $\overline{\text{MREQ}}$ signal and $\overline{\text{WR}}$ signal produced by an external logic circuit.




Note : Althrough addresses on A0-A15 are originally I/O addresses, they are handled as memory addresses.

Figure 3.20 Simultaneous Transfer Timing of Memory to I/O (I/O search timing)




Note : Althrough addresses on A0-A15 are originally I/O addresses, they are handled as memory addresses.

Figure 3.21 Simultaneous Transfer Timing of I/O to Memory (I/O search timing)

(d) Bus request timing

When RDY signal becomes active, DMA samples RDY signal at the rising edge of the clock and if the bus is not full ($\overline{BUSREQ}$="1") DMA makes $\overline{BUSREQ}$ signal to "0" level at the rising edge of next clock and request MPU to hand over the system bus control right.

MPU samples $\overline{BUSREQ}$ signal at the rising edge of the last state clock of the machine cycle which MPU is executing at that point of time and if it is "0", makes $\overline{BUSACK}$ signal to "0" level at the rising edge of next clock.

Therefore, maximum value of a time required for MPU to hand over the bus control right to DMA ($\overline{BUSACK}$="0") after DMA detected that RDY signal becomes active is the sum of one machine cycle (valiable) and one clock period of MPU.

When detecting that $\overline{BAI}$ ($\overline{BUSACK}$) signal is at "0" level for 2 clock period, DMA start the DMA action. There is the delay time of max. One machine cycle +3 clock period after RDY signal becomes active till the DMA action is actually started.

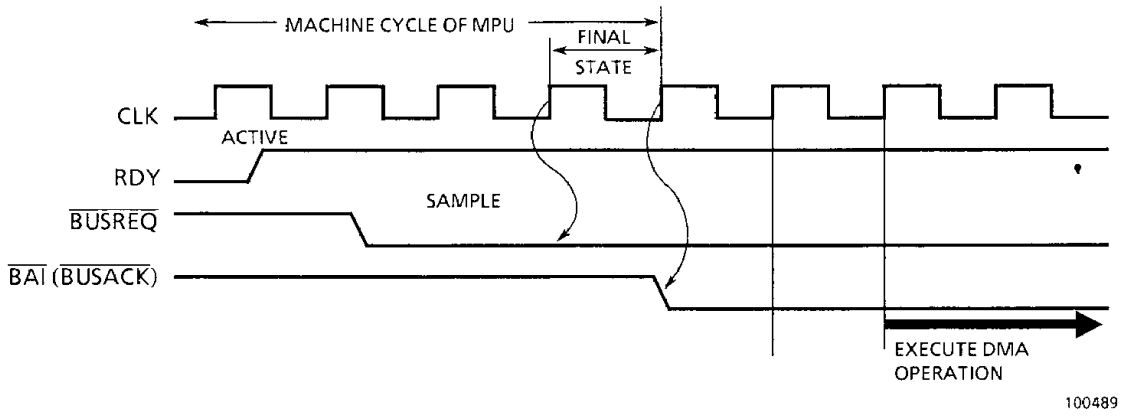



Figure 3.22 Bus Request Timing

(e) Bus release timing - byte mode

In the byte mode, DMA makes $\overline{BUSREQ}$ signal to "1" level at the rising edge of the clock immediately before end of each data transfer cycle (the end of readout cycle in the search operation and the end of write cycle in the transfer and trasfer/search operation.)

Although $\overline{BUSREQ}$ signal becomes "1" before the end of DMA cycle by one clock, MPU resumes the operation one clock after $\overline{BUSREQ}$ signal becomes "1" level and therefore, there will be no trouble.

After the bus is released, next bus request is made at the leading edge of the clock immediately after both $\overline{BUSREQ}$ signal and $\overline{BAI}$ signal becomes "1" level. RDY signal being active is the conditions for this.

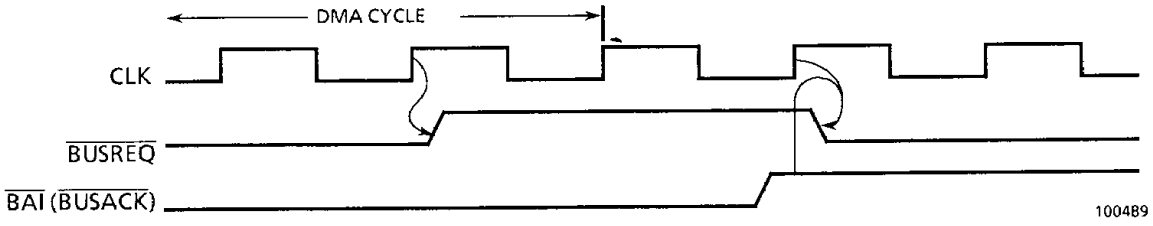



Figure 3.23 Bus Release Timing - Byte Mode

(f) Bus release at the end of block in the burst mode or continuous mode

When it is programmed to stop DMA at the end of block in the burst mode or continuous mode, $\overline{\text{BUSREQ}}$ signal is set to "1" level at the rising edge of the clock at the end of last data transfer. This last data is transferred even when RDY signal becomes non-active.

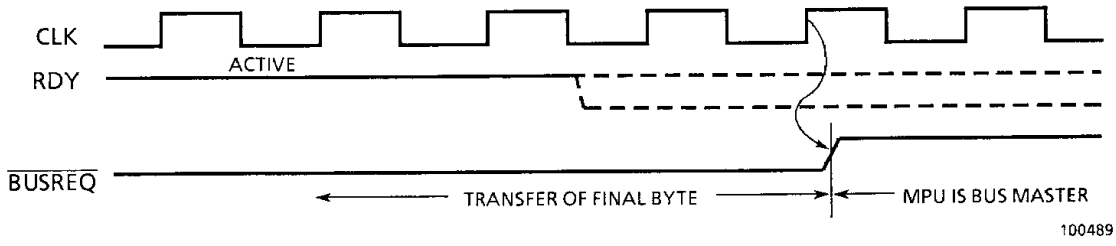



Figure 3.24 Bus Release Timing - at End of Block

(g) Bus release when coincidence is detected in the burst mode or continuous mode

When DMA is set in the burst mode or continuous mode and programmed to stop its operation at byte coincidence, DMA stops to operated when the byte coincidence is detected.

Since DMA operation is pipelined and the advance reading is performed, a check to determine if the n th data coincides with the coincidenced byte is carried out at the same time when the n + 1 st data is transferred. Therefore, data of N+1 byte is transferred and $\overline{\text{BUSREQ}}$ signal is set to "1" level at the leading edge of the clock when this transfer ended.

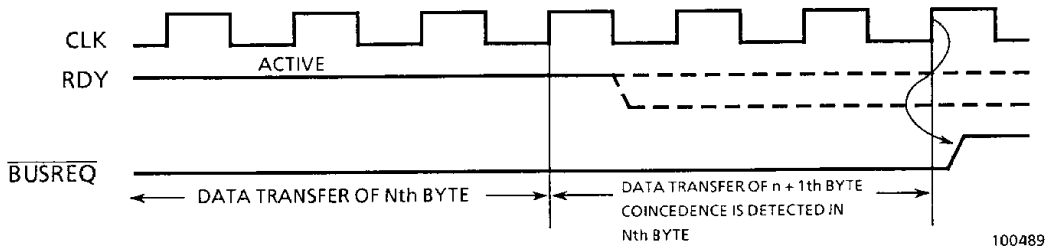



Figure 3.25 Bus Release Timing on Match - Byte Mode, Continuous Mode

(h) Bus release when RDY signal is non-active

If RDY signal becomes non-active in the burst mode, $\overline{BUSREQ}$ signal is set to "1" level at the rising edge of next clock after end of the byte operation that is under execution at the time. For instance, this is done when the read of the search only or simultaneous transfer/search operation ended or when the write of the trasfer/search operation ended. Therefore, the action for $\overline{BUSREQ}$ signal is slightly behind the action for RDY signal.

DMA always does not release the bus until the byte action at the time is completed.

In contrast with this, in the continuous mode $\overline{BUSREQ}$ signal is kept at "0" level even when RDY signal becomes non-active.

In addition, after the byte action at the time ended DMA is put in the idle state until RDY signal becomes active again.

This figure is shown in Figure 3.26.

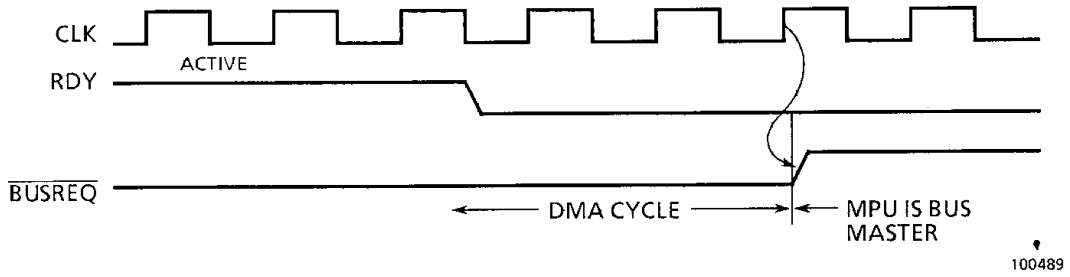



Figure 3.26 Bus Release Timing when RDY Signal becomes Non-active

Timing of RDY signal with other signals are shown in Figure 3.27, 3.28 and 3.29. In these figures the memory search only operation by the Z80 standard timing by mode is assumed. In each of the operation modes, RDY signal is sampled at the rising edge of the last clock of the read or write cycle to determine its level.

RDY signal can become non-active before completion of the last byte operation withour affecting its operation. In the byte or burst mode, $\overline{BUSREQ}$ signal and $\overline{BAI}$ signal are set to "1" at the end of byte operation of RDY signal. In the byte or burst mode, the bus control signals ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$) are also kept at "1" level as long as RDY signal is non-active. Further, the address bus and data bus are kept in 3 state.

The continuous mode differs from other modes in that the address bus holds an address which is incremented in advance against next byte during the period when RDY signal is non-active. This address can be used immediately after RDY signal becomes ative again.

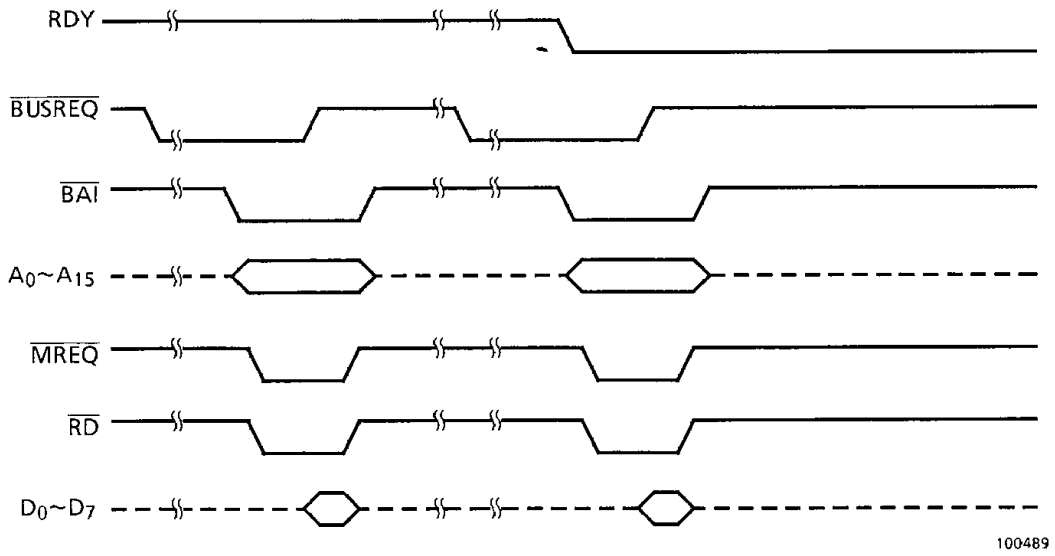



Figure 3.27 Timings of RDY Signal with Other Signals (Byte Mode)

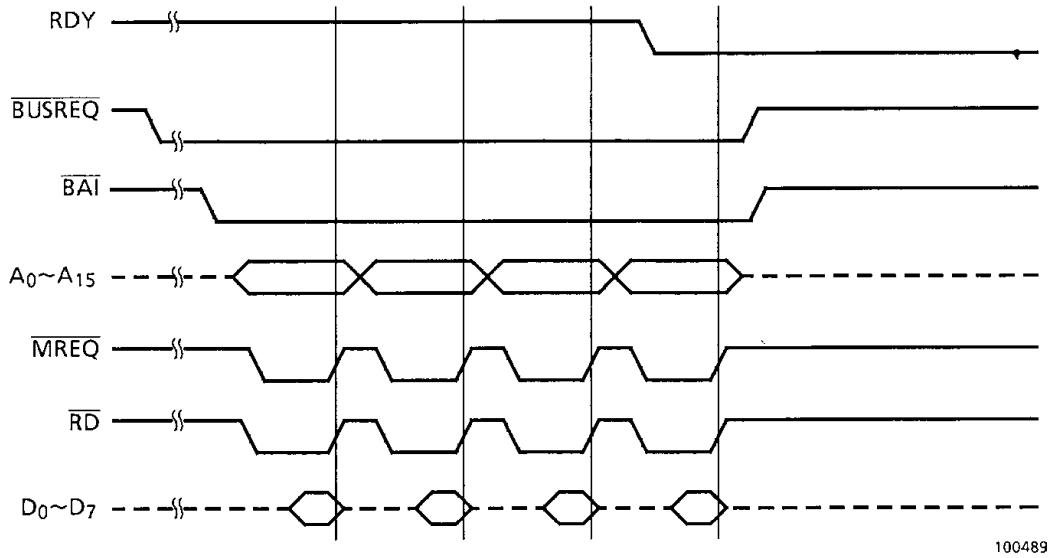



Figure 3.28 Timings of RDY Signal with Other Signals (Burst Mode)

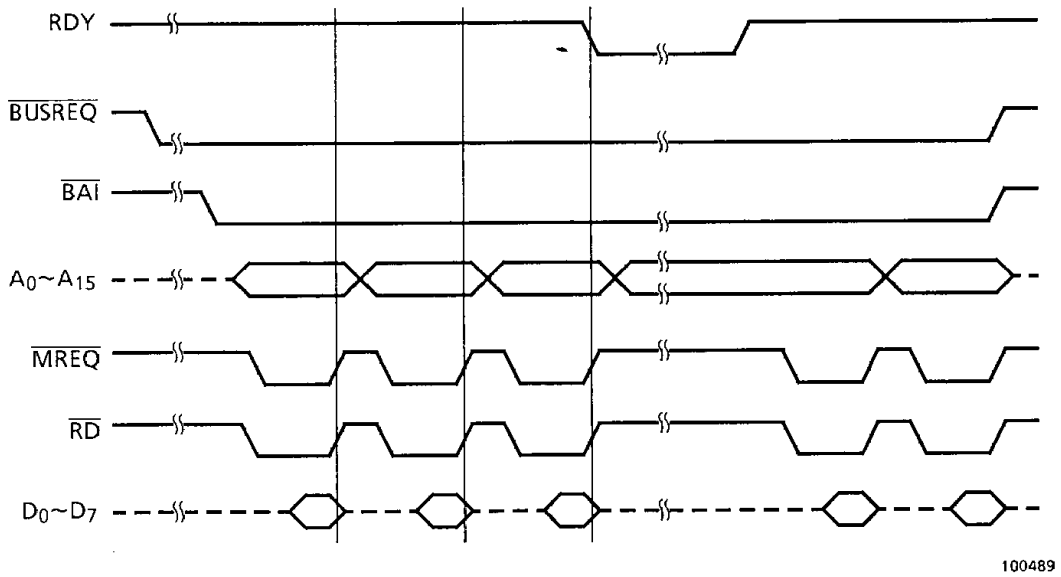



Figure 3.29 Timings of RDY Signal with Other Signals (Continuous mode)

(i) Variable cycle

When programmed, DMA is capable of changing read and write cycle lengths. Source and destination can be programmed independently by the write register WR1 (designation of Port A) and WR2 (designation of Port B). This variable cycle function allows the read or write in 2, 3 or 4 clock cycles (more clock cycles if Tw is inserted) and further, can increase or decrease pulse widths of all signals generated by DMA. Four signals relative to the data transfer; $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals have the function to end the rising edge timing earlier by 1/2 clock independently.

Differing from the standard timing, in the variable cycle mode $\overline{\text{IORQ}}$ signal becomes active earlier than $\overline{\text{MREQ}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals by 1/2 clock. Further, $\overline{\text{CE/WAIT}}$ signal can be used in the extension of 3 or 4 clock cycle variable memory cycle and 4 clock cycle variable I/O cycle only. In the 3 or 4 clock cycle memory operation, $\overline{\text{CE/WAIT}}$ signal is sampled at the T2 falling edge while it is sampled at the T3 falling edge in the 4 clock cycle I/O operation. In the 2 clock cycle operation it is not sampled. Use of this variable cycle effective in increasing data transfer rate and reducing software burden and further, can eliminate an external logic circuit. In addition, this function provides more faster memory read/write speed than normal speed.

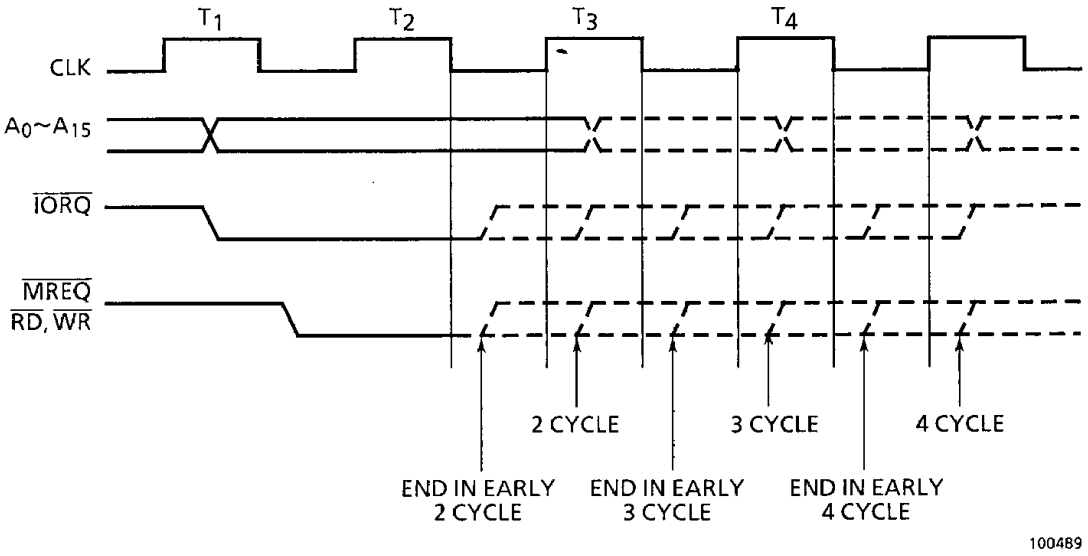



Figure 3.30 Variable Cycle

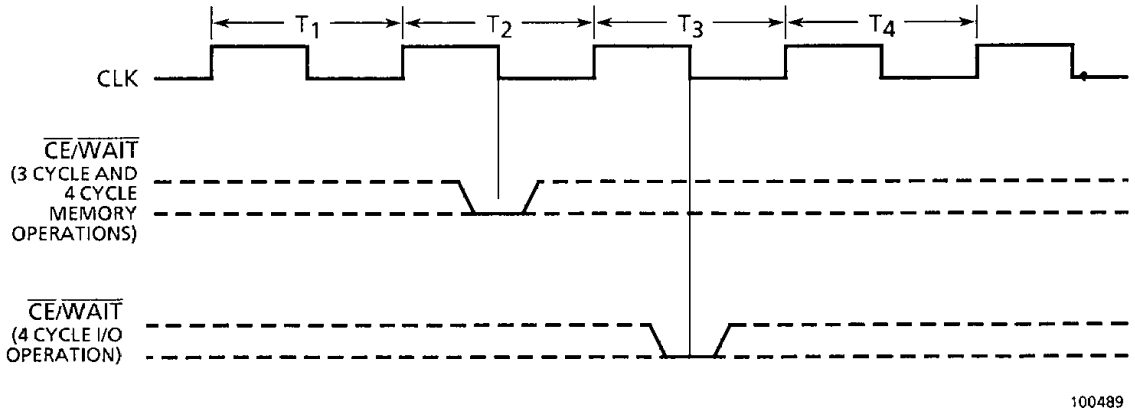



Figure 3.31 $\overline{\text{WAIT}}$ Sample in Variable Timing

(j) Interrupt

The timing for the interrupt acknowledge or return from interrupt is identical to that of other Z80 peripheral LSI's. $\overline{INT}$ signal is sampled by MPU at the rising edge of the last clock of all commands. If the interrupt enable is not set by the internal MPU software or when $\overline{BUSREQ}$ signal is active, this $\overline{INT}$ signal is not accepted. When $\overline{INT}$ signal is accepted, $\overline{IORQ}$ signal also becomes active at the same time (normally, $\overline{MREQ}$ signal) in the period of its M1 cycle, indicating that the interrupting LSI can load its 8-bit vector on the data bus. At the same time, two wait status are automatically inserted into this cycle. This is to facilitate execution of the priority interrupt mechanism and the wait status of 2T gives a stabilizing time to IE1 and IE0 signals and thus, it becomes possible to identify which peripheral LIS will react.

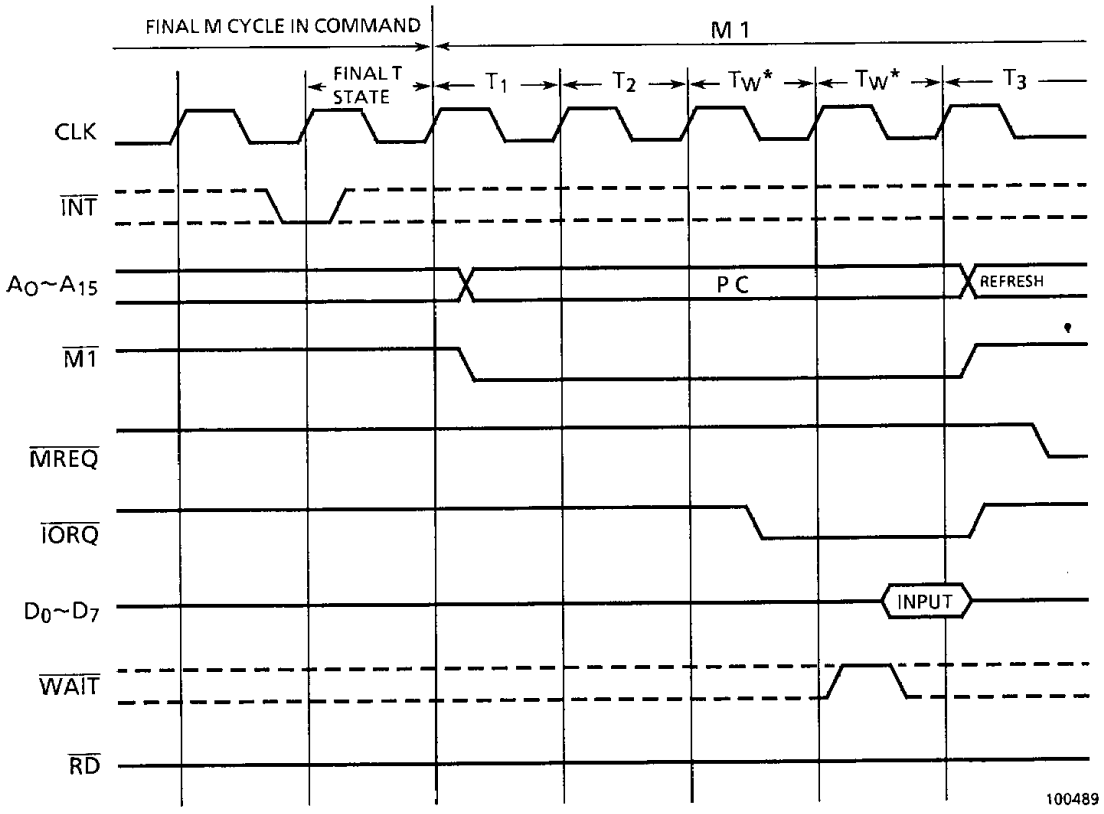



Figure 3.32 Interrupt Acknowledge

Interrupt on RDY signal (interrupt before the bus request) does not directly affect $\overline{BUSREQ}$ signal. The process in this case is carried out by giving following commands to the write register WR6 in the interrupt service routine.

- Enable after interrupt return (B7H)
- DMA enable (87H)

- Execution of REI instruction to reset IUS latch during the interrupt service in the Z80 DMA (ED4DH)

(k) Pulse generation

In the pulse generation, $\overline{INT}$ signal is set to "0" level (pulses are generated on the $\overline{INT}$ line) every 256 bytes after offset value is loaded to the write register WR4 by the program.

$\overline{INT}$ signal is put to "0" level during the DMA cycle in which pulse control bytes coincide with low order bytes of the byte counter and kept at "0" level in the full period of transfer cycle. Here, the transfer cycle means the read cycle (the search only or simultaneous transfer operation) or read/write cycle and lengths of the read and write cycles can be set independently by variable cycle.

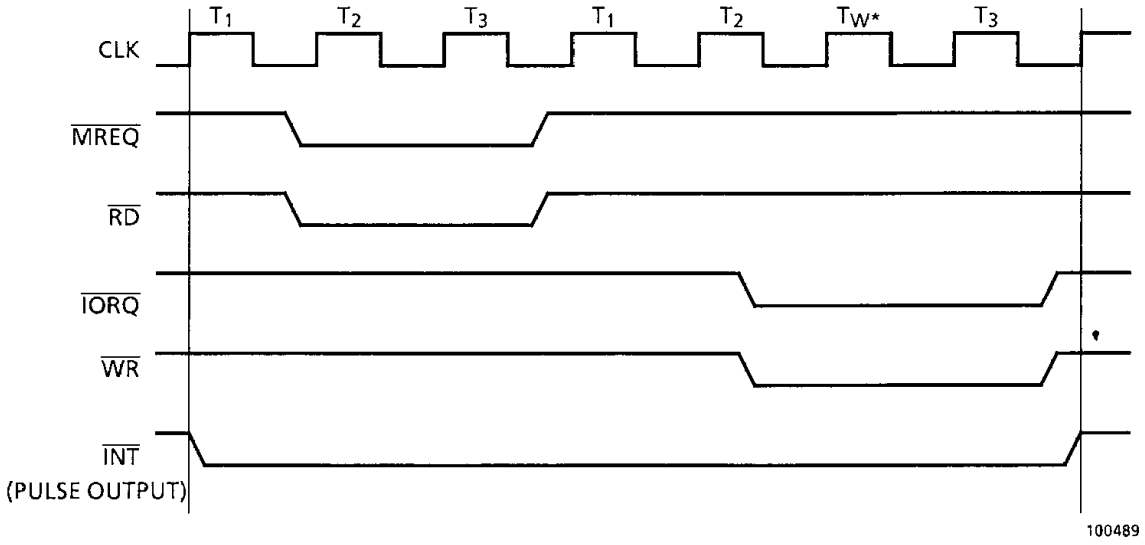



Figure 3.33 (a) Pulse Output (Standard timing at the time of transfer)

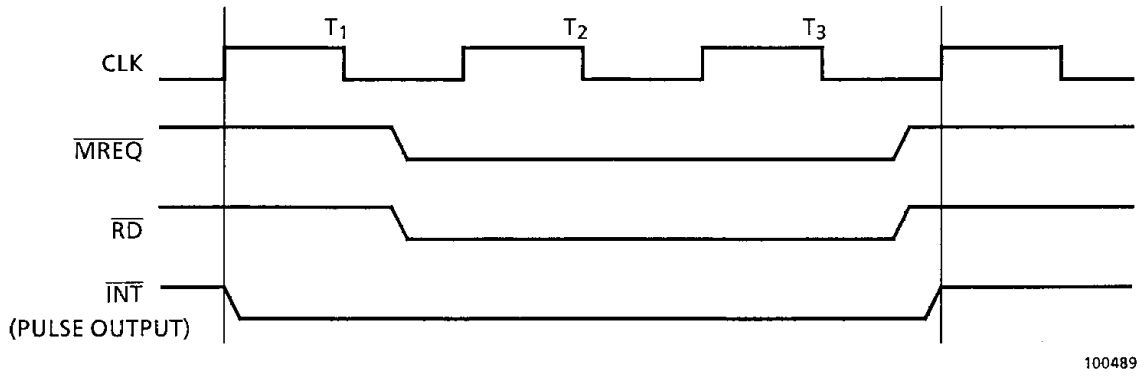



Figure 3.33 (b) Pulse Output (Standard timing at the time of memory search)

(I) Precautions

① Transfer timing

Although the DMA transfer timing is basically identical to the read/write timing of the Z80 MPU, care is required when variable cycle is used or in case of simultaneous transfer.

In the case of simultaneous transfer, all addresses which are output by DMA are interpreted to be memory addresses and I/O are selected by the hardware using an external logic circuit. It is normally programmed that I/O addresses are fixed and memory addresses are updated during the DMA operation. At this time, DMA controls memory addresses and outputs I/O select signal using an external logic circuit.

② Memory refresh

Since DMA has no refresh signal output function, the refresh of a dynamic RAM is performed normally using RFSH signal of MPU. If the transfer period becomes long in the DMA operation using the burst mode or continuous mode, another refresh method must be used.

③ Pulse generation

When the pulse generating function is used for transfer in the byte mode, pulse output is generated in two times. This is to avoid BAI signal from becoming non-active and MPU from being put in HALT state. Further, when offset value and low order 8 bits of the block length are equal other, pulse is once generated and after DMA operation is completed, pulse is generated during the read cycle of the 1st byte when the DMA operation is performed again without changing the offset value.

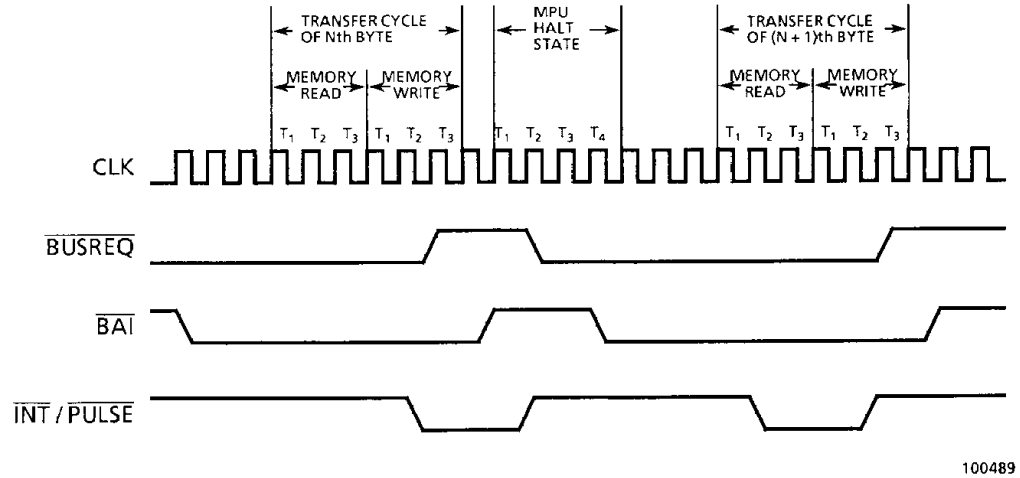



Figure 3.34 Pulse Generation Timing (Byte mode)

## 3.4 PERIPHERAL COMMANDS

To operate DMA, specify its operations by writing into the control register group through programming. In addition, the status of DMA can be known by reading the contents of the status register group.

To give effect to this on a program, write the operation into the write register by OTIR or OUT command to MPU and read out by INIR or IN command. In both cases, output of the I/O address decoder to DMA becomes "0" level. This output is connected to the $\overline{CE}/\overline{WAIT}$ pin.

The configurations of the control register group and status register group are as follows:

(1) Control register group

① Write register WR0
② Write register WR1
③ Write register WR2
④ Write register WR3
⑤ Write register WR4
⑥ Write register WR5
⑦ Write register WR6

(2) Status register group

① Readout register RR0
② Readout register RR1
③ Readout register RR2
④ Readout register RR3
⑤ Readout register RR4
⑥ Readout register RR5
⑦ Readout register RR6

### 3.4.1 Control register group

The control registers consist of 7 groups of WR0 to WR6, each of which consists of a basic register and related registers. If the pointer bit of the basic redister is "1", related redisters are accessed by turns.

The basic registers WR0 to WR6 are identified by the combination of bits 0, 1, 2, 6 and 7. There may be pointer bits for related registers. BBH (followed by the readout mask) command of WR6 has no pointer bit but data that follows this command is limited to the readout mask.

(1) Write register WR0

WR0 is identified by the condition that Bit 7 of the basic register is "0" and Bit 1, 0 are other than both "0".

WR0 has 4 pointer bits, each of which has related registers, respectively.

(a) Basic register bit 0, 1 (Designation of operating class)

Bit 0 and 1 designate the operating class; transfer, search only, and transfer/search operations. In addition, simultaneous transfer or transfer/search is obtained by selecting search and generating a proper bus control signal for complete transfer through external hardware.

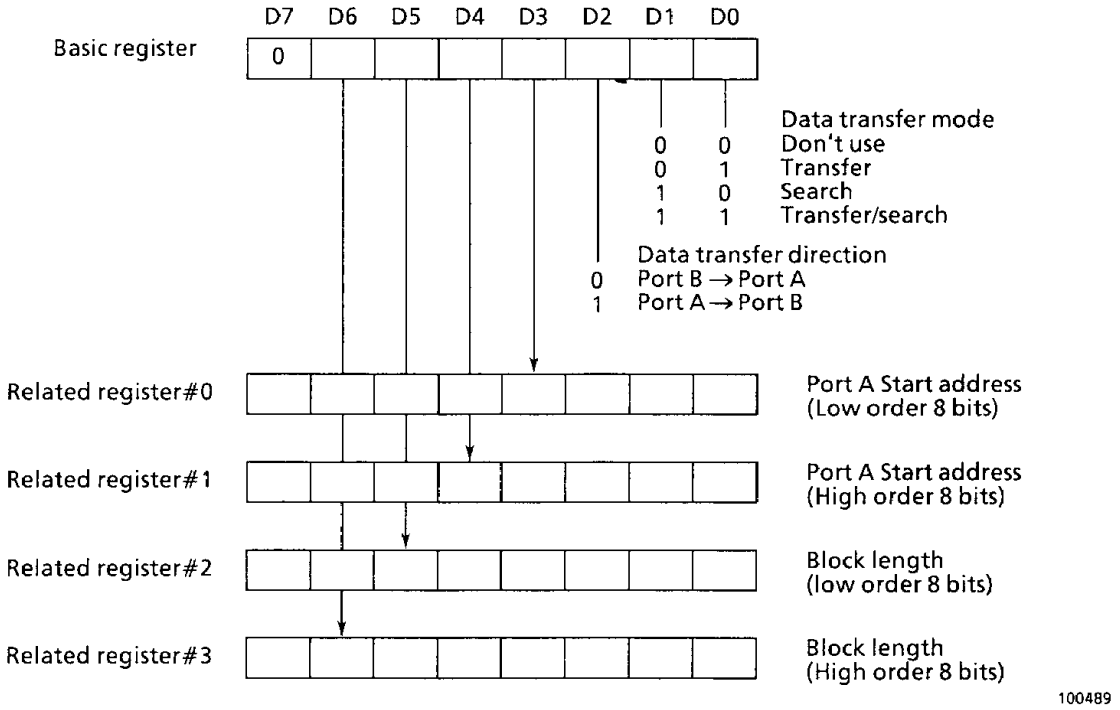



Figure 3.35 Write Register WR0

(b) Basic register bit 2 (Designation of data transfer direction)

Bit 2 declears the source port, and by implication, the destination port, if the operation is a sequential transfer. In the search only operation, the source port only is designated and in the simultaneous transfer or transfer/search operation, the destination port is decided by external wiring.

(c) Basic register bit 3-6 (Pointer bits)

Bit 3-6 are the pointer bits which are used to designate four related registers following respective bits.

(d) Related register #0, #1 (Port A start address)

These registers are accessed by Bit 3 and 4 of the basic register byte. When Port A is used as a source or destination, it is necessary to write the start address. Low order byts are written into #0 and high order bytes in #1.

(e) Related register #2, #3 (Block length)

These registers are designated by Bit 5 and 6 of the basic register.
Max. 64K bytes can be designated by writting low order bytes of block length into #2 and high order bytes into #3. However, as data read is pipe line type, number of bytes actually searched or transferred is more than that entered here by 1 or 2.

In addition, if "zero" is set for these registers, the transfer or search of $2^{16}+1$ bytes is carried out.

(2) Write register WR1

WR1 is identified by the condition that all of Bits 0, 1 and 7 of the basic register are "0" and Bit 2 is "1".

(a) Basic register bit 3 (Port A designation)

A memory is designated by Port A when "0" is written for Bit 3, while I/O is designated when "1" is written. This designation makes the control signal ($\overline{MREQ}$ or $\overline{IORQ}$) active against the cycle including this port.

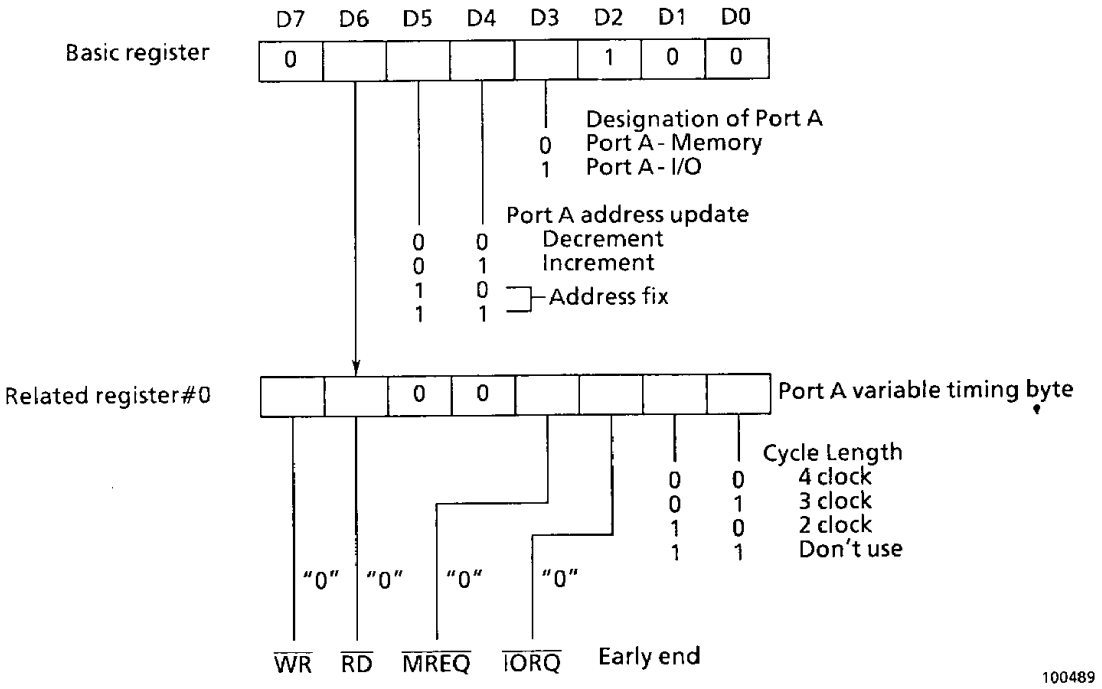



Figure 3.36 Write Register WR1

(b) Basic register Bit 4, 5 (Fixed or variable address designation)

Fixed or variable Port A address is designated by Bit 4 and Bit 5 for each transfer or search byte.

(c) Basic register Bit 6 (Pointer bit)

When Bit 6 is set to "1". next related register is accessed. In addition, when Bit 6 is set to "0", DMA's variable cycle is not used.

(d) Related register #0 (Port A variable timing byte)

By setting values for this register, Port A cycle length and control signal timing can be designated.

- Bit 0, 1 (Cycle length)

  Length of data transfer cycle (memory read/write, I/O read/write) relative to Port A is designated. Timing can be changed in a range of 2 - 4 clocks.

- Bit 2, 3, 6, 7 (Early end)

  The timing of the control signal $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$ and $\overline{WR}$ can be advanced by 1/2 clock.

(3) Write register WR2

WR2 is identified by the condition that all of Bits 0, 1, 2 and 7 of the basic register are "0".

(a) Basic register bit 3 (Port B designation)

A memory is designated by Port B when "0" is written for Bit 3, while I/O is designated when "1" is written. This designation makes the control signal ($\overline{MREQ}$ or $\overline{IORQ}$) active against the cycle including this port.

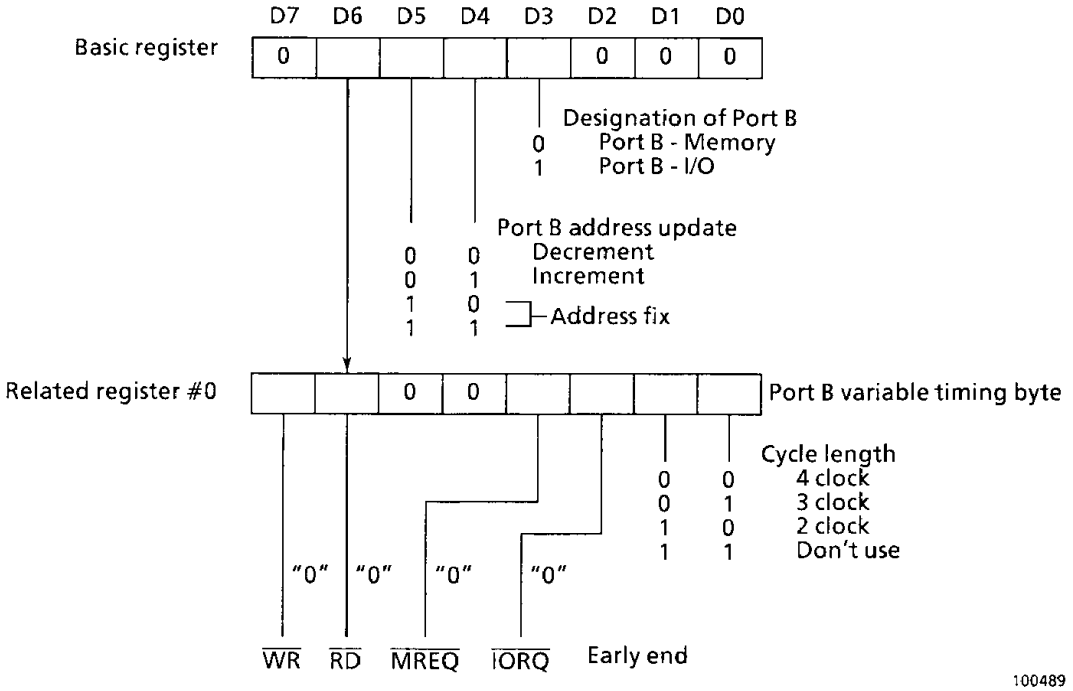



Figure 3.37 Write Register WR2

(b) Basic register Bit 4, 5 (Fixed or variable address designation)

Fixed or variable Port B address is designated by Bit 4 and Bit 5 for each transfer or search byte.

(c) Basic register Bit 6 (Pointer bit)

When Bit 6 is set to "1", next related register is accessed. In addtion, when Bit 6 is set to "0", DMA's variable cycle is not used.

(d) Related register #0 (Port B variable timing byte)

By setting values for this register, Port B cycle length and control signal timing can be designated.

- Bit 0, 1 (Cycle length)

  Length of data transfer cycle (memory read/write, I/O read/write) relative to Port B is designated. Timing can be changed in a range of 2 - 4 clocks.

- Bit 2, 3, 6, 7 (Early end)

  The timing of the control signal $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$ and $\overline{WR}$ can be advanced by 1/2 clock.

(4) Write register WR3

WR3 is identified by the condition that both Bit 0 and Bit 1 of the basic register are "0" and Bit 7 is "1".

(a) Basic register Bit 2 (Stop on match)

This bit is used for the search or transfer/search operation. When this bit is "1" and transferred data matches the match byte, the data transfer is stopped and the bus is released. When this bit is "0" and transferred data matches the match byte (if DMA is not stopped even when they matched), the status flag is set on the status byte to allow interrupt resulting from byte match.

(b) Basic register Bit 3 (Pointer bit)

When this bit is set at "1", the mask byte follows the basic register.

(c) Basic register Bit 4 (Pointer bit)

When this bit is set at "1", a match byte follows the basic register.
This bit designates a match byte used for comparison with all data to be searched.

(d) Basic register Bit 5 (Interrupt enabled)

When this bit is set at "1", DMA interrupt is enabled.

(e) Basic register Bit 6 (DMA enable)

When this bit is set at "1", DMA operation is enabled and a bus request can be made to MPU.

(f) Related register #0 (Mask byte)

This register is accesed by basic register Bit 3. It is possible to write a mask byte required for the search operation. The mask byte is capable of masking the match byte (data to be compared) during the search operation to extract bits to be compared.

When all bits of the mask byte are at "0", the comparison is made and when they are at "1", the masking is made. In addition, if no masking is required and all bits are compared, write 00H mask byte.

(g) Related register #1 (match byte)

This register is accessed by basic register Bit 4. The match byte is used as data to be compared when the data transfer mode is search or transfer/search. The match byte is masked by the mask byte of related register #0.

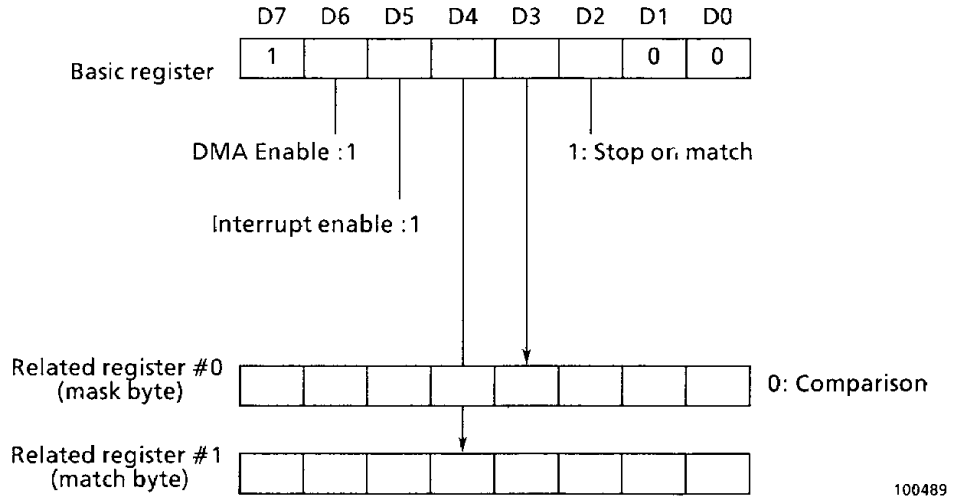



Figure 3.38 Write Register WR3

(5) Write register WR4

WR4 is identified by the condition that both Bit 0 and Bit 7 of the basic register are "1" and Bit 1 is "0".

(a) Basic register Bit 2 - 4 (Pointer bit)

When these bits are set at "1", the related registers #0 to #2 are accessed after the basic register.

(b) Basic register Bit 5, 6 (Operation mode designation)

Operation mode selected values can be set for Bit 5 and Bit 6. For values to be set, refer to Figure 3.39.

(c) Related register #0, #1 (Port B start address)

These registers are accessed by basic register Bit 2 and Bit 3. Related register #0 designates low order byte of Port B start address while related register #1 designated high order byte of Port B. Further, if low order 8 bits are sufficient for Port B start address, thr loading to related register #1 is not required.

(d) Related regiser #2 (Interrupt control byte)

This register control DMA interrupt or pulse generation. By setting Bit 3 and Bit 4, related registers #3 and #4 can be accessed.

- Bit 0 (Interrupt on match)

When Bit 0 is set at "1", DMA generates interrupt if transferred data matches the match byte in the search or transfer/search operation.

- Bit 1 (Interrupt on end of block)

When Bit 1 is set at "1", DMA generates interrupt if a value of the byte counter becomes "0" in DMA operation.

- Bit 2 (Pulse generation)

When Bit 2 is set at "1", pulse is generated on the $\overline{INT}$ line whenever data in number of bytes set on the pulse control byte is transferred.

- Bit 3, 4 (Pointer bits)

When Bit 3 is set at "1", pulse control byte is accessed after interrupt control byte. When Bit 4 is set at "1", the interrupt vector is accessed.

- Bit 5 (Vector value change by status)

When this bit is set at "1", interrupt vector value changes according to cause for generating interrupt. However, if the automatic restart or interrupt at the end of block was already set, this mode cannot be used.

- Bit 6 (Interrupt on RDY)

When this bit is set at "1", DMA generates interrupt prior to the bus request if it detects that RDY signal has become active. Therefore, the interrupt enable command becomes necessary and when RETI instruction is executed after the interrupt enable of WR6 (B7H) is sent out, the bus request is started.

(e) Related register #3 (Pulse control byte)

When Bit 3 of the interrupt control byte is set at "1", the pulse control byte is accessed after the interrupt control byte. The pulse control byte gives offset values to pulse that are first generated (Number of bytes shown by this control byte).

The pulse control byte compares low order 8 bits of the byte counter and if both coincide each other, pulses are output on the $\overline{INT}$ line.

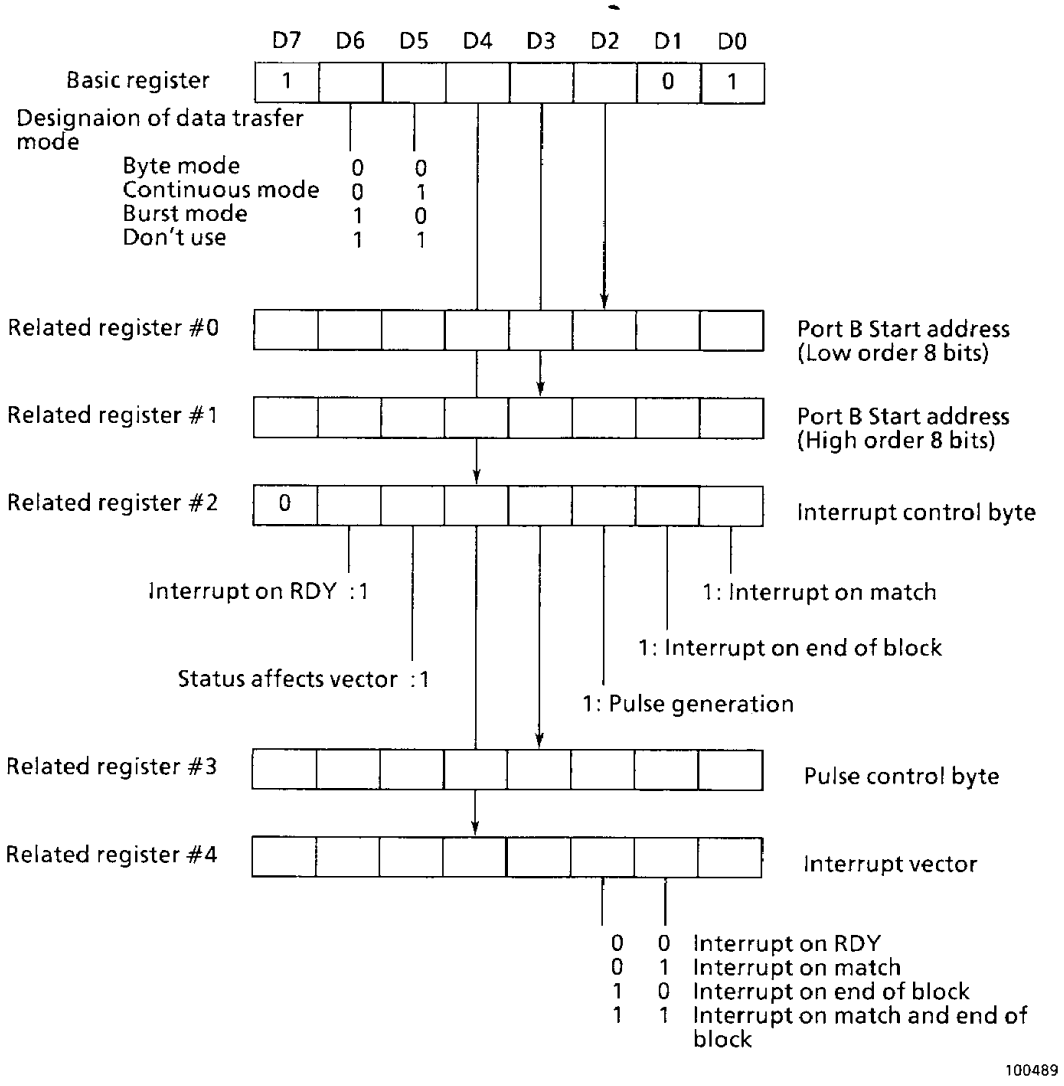



Figure 3.39 Write Register WR4

(f) Related register #4 (Interrupt vector)

When Bit 4 of the interrupt control byte is set at "1", the interrupt vector is accessed after the interrupt control byte. The interrupt vector is loaded on the data bus at time of the interrupt acknowledge by MPU ($\overline{IORQ}$="0", $\overline{M1}$="0"). If Bit 5 of the interrupt control byte is set at "1", Bit 1 and Bit 2 of the interrupt vector change according to the interrupt factor. However, when the automatic restart and interrupt on the end of block has been already programmed, the interrupt vector sent out at the end of block does not change and therefore, the mode for vector value change by status cannot be used.

(6) Write register WR5

WR5 is identified by the condition that Bit 1 and 7 of the basic register are "1" and Bit 0, 2 and 6 are "0". WR5 has no related register.

- Bit 3 (Effective polarity of RDY signal)

  When this bit is set at "0", RDY signal becomes "0" and active, and when it is set at "1", RDY signal becomes "1" and active.

- Bit 4 (Use of $\overline{CE}/\overline{WAIT}$ pin)

  When this bit is set at "0", $\overline{CE}$ function only is available. When it is set at "1", both $\overline{CE}$ and $\overline{WAIT}$ functions become available. When $\overline{BUSREQ}$ signal is at "1", CE function is available, while if $\overline{BUSREQ}$ signal is at "0" level, WAIT function is available.

- Bit 5 (Automatic register)

  When this bit is set at "0" level, DMA operation is stopped at time of the end of block (Byte counter = "Zero"). When it is at "1" level, the contents of the address register and byte counter are automatically loaded on the address counter and byte counter, and DMA operation is continued.

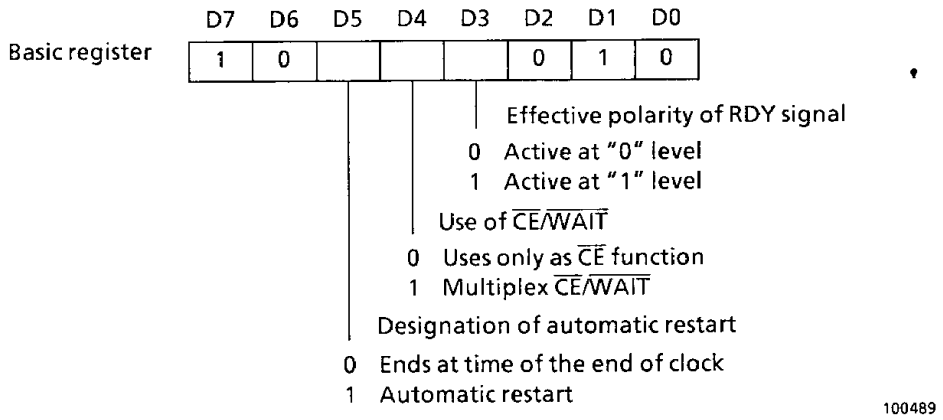



Figure 3.40 Write Register WR5

(7) Write register WR6

WR6 is identified by the condition that Bit 0, 1 and 7 of the basic register are at "1" level. In the case of WR6, the functions (commands) are divided by the combination of Bits 2 to 6.

(a) Reset (C3H)

This command is used to reset DMA. By executing this command, DMA performs the followings;

- Disables the interrupt control circuit and bus request control circuit.
- Releases the interrupt latch.
- Releases the forced RDY condition.
- Releases the automatic restart condition.
- Releases $\overline{CE}/\overline{WAIT}$ function (Bit 4 WR5) and retains $\overline{CE}$ function only.
- Returns the timings of both Port A and B to the Z80 standard timing.

After turning power to DMA ON, and performing the programming, it is necessary to execute the reset command once. In addition, if the DMA operation is interrupted during its execution, it is necessry to execute the reset command 6 times successively (this is because there are 5 related registers that are capable of directing in WR4).

Further, DMA is not always reset completely by this reset command. The read sequence is reset only by the read sequence reset command.

(b) Port A timing reset (C7H)

This command resets Port A variable timing byte and returns Port A timing to the Z80 standard timing.

(c) Port B timing reset (CBH)

This command resets Port B variable timing byte and returns Port B timing to the Z80 standard timing.

(d) Load (CFH)

When this command is executed, the content of the address register is loaded on the address counter and the byte counter is cleared. In addition, the internal forced RDY condition is also released.

Further, an address counter to which the loading can be made immediately is the source port address counter only. The loading to the destination port address counter is made when a value of this counter is initially updated (incremented/decremented) but if "address if fixed", the loading is not performed. However, the loading by the "fixed address destination port programming" technique is possible. If DMA becomes non-active when the load command is written, another DMA control byte is written before the load command.

(e) Continue (D3H)

Although this command clears the byte counter to "zero", both port address counters do not change. This command is used in transferring several data blocks to continued positions in the many buffer if it is desirable to know a break of every block, and continues DMA operation which has been interrupted by detection of match at the end of block or search.

In order to execute this command, interrupt at the end of each blocks is needed and new block length shall be entered in WR0 with the continue command.

In transferring data blocks, interrupt becomes necessary whenever transfer of each data block ended. In trasferring next data block after the interrupt, this continuity command is used inserted of the load command.

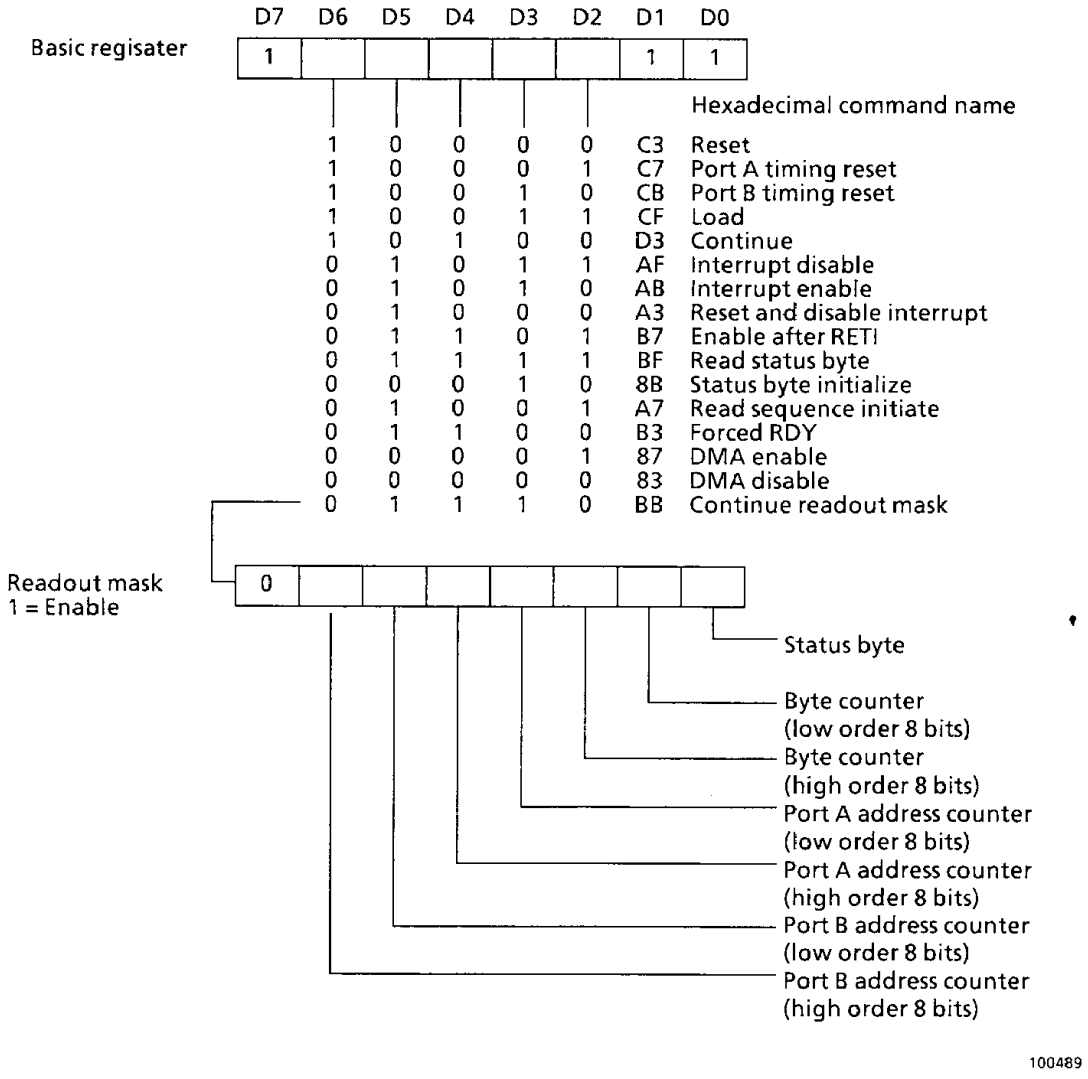



Figure 3.41 Write Register WR6

(f) Interrupts disable (AFH)

This command is used to simulate the Z80 MPU's interrupt acknowledge when DMA is operated in a system other than the Z80 MPU. When DMA sends the interrupt signal into any MPU other than the Z80 MPU, if the inerrupt disable command is written into the beginning of the service routine, $\overline{INT}$ signal returns to "1" level but next interrupt signal of DMA cannot be sent during the service routine is continuously carried out. Generation of next interrupt signal becomes possible when the interrupt enable command is written into the end of the service routine.

(g) Interrupts enable (ABH)

This is a command used on the Z80 system to enable the interrupt when the power source is ON. This command enables the interrupt control circuit of DMA. When the interrupt disable command is not used, if the interrupt enable command is once written, next interrupt is enabled automatically when RETI instruction is executed at the final stage of the interrupt service routine. However, if the interrupt disable command is used, it becomes necessary to write the interrupt enable command at the final stage of the interrupt service routine.

(h) Reset and interrupt disable (A3H)

This command is used on such systems as 8080 and 8085 to interface DMA and MPU which is provided with the interrupt acknowledge function but has no RETI instruction. This command, when executed, performs the followings:

- Reset of the in-interrupt service routine (IUS) latch
- Reset of the interrupt pending (IP) latch
- Release of the internal forced RDY signal conditions
- Succeesing interrupt disable by DMA (same as the interrupt disable command)

(i) Enable after RETI (B7H)

This command is used only when "interrupt on RDY signal" is programmed on WR4. DMA, when detecting that RDY signal becomes active, does not make the bus request but grenerates the interrupt signal. After the interrupt return, this command enables DMA to make the bus request again. This command is always used to make the bus request after the interrupt to RDY signal on the Z80 MPU system. This command also can be used on other MPU's, for instance, 8080.
The interrupt latch (IOR) to RDY signal is set during its interrupt cycle. This latch makes RDY signal active and DMA is not allowed to make the bus request until this latch is reset by Enable after RETI instruction.

The execution sequence of the Z80 MPU service routine is as follows and the bus request is mode after RETI instruction is executed:

```
    ⋮
Enable after RETI
DMA Enable
    ⋮
RETI Instruction
```

(j) Read status byte (BFH)

This command indicates that next read command is the status byte access.

(k) Status byte initialization (8BH)

This command indicates the reinitialization of bit 4 and 5 of the status byte. The reinitialization of the interrupt pending status (Bit 3) of the status byte can be effected by the interrupt acknowledge, interrupt process, interrupt reset and disable command writing. The reinitialization of DMA operation status (Bit 0) can be efected by the load command.

(l) Read mask continue (BBH)

This command denotes that next control byte which is to be written into DMA follows the read mask register. The read mask register is used for setting a new read sequence of RR0 to RR6 and is normally a part of the initial state setting when the power source for DMA is turned ON.

The read mask can be programmed by setting the related pointer bit of register to be read out "1" level. The read sequence start command is used for initialization.

(m) Read sequence initiate (A7H)

This command is used to initiate the read sequence pointer command as a measures to access the first (in low order) read register that is designated to be readable by the read mask for initialization of DMA by next MPU read command. Normally, this command is output to reset the read sequence immediately after loading of the read mask.

(n) Forced RDY (B3H)

In the burst mode or continuous mode, this command is used to make the internal RDY conditions active for the active RDY signal by an external logic circuit. This command is used for memory-to-memory transfer or memory search where RDY signals not required. It is not necessary to consider the effective polarity of RDY signal. Use of this command can eliminate an external logic circuit.

The forced RDY conditions are released by the following commands/conditions:

- Reset command
- Load command
- Interrurpt reset and disable command
- Ending by end-of-block
- Ending by byte match
- Bus release by DMA

(o) DMA enable (87H)

This command is used to enable the bus control circuit of DMA. The interrupt circuit is not affected nor the function and latch are reset. This bus request enable function is identical to that of Bit 6 of WR3. In the interrupt service routine, DMA enable command is the last command to DMA before MPU executes RETI instruction.

(p) DMA disable (83H)

This command inhibits the bus request by DMA. This command is used to stop DMA operation by external events, end-of-block or match by bytes and when reinitialization of the status byte is required.

3.4.2 Status register group

There are 7 read registers RR0 to RR6 available for DMA to know the operation execution or end status.

The readout of MPU is made according to the method to access DMA as the peripheral I/O using I/O command. Commands to be written into DMA are as follows:

① Read status byte (BFH)
② Read sequence initiate (A7H)
③ Status byte reinitialize (8BH)
④ Read mask continue (BBH)

The above commands are those which are shown for WR6.

(1) Read register PR0 - Status byte

(a) Bit 0 (DMA operation)

This bit indicates if DMA made the bus request after the last LOAD command. "1" indicates that DMA made the bus request while "0" indicates no bus request made.

(b) Bit 1 (RDY signal active)

"0" of this bit indicates that RDY signal is active. "1" indicates RDY signal being non-active.

(c) Bit 2 (Don't Care)

(d) Bit 3 (Interrupt pending)

This bit indicates the interrupt pending (IP) latch status. "0" indicates the interrupt pending.

(e) Bit 4 (Match detection)

When this bit is "0", it indicates the match after the last status byte reset or reintialization command.

(f) Bit 5 (End-of-block detection)

When this bit is "0", it indicates the end-of-block reached after the last status byte reset, load, continuity or reinitialization.

(g) Bit 6, 7 (Don't Care)

(2) Read register RR1, RR2 - Byte counter

The 16-bit counter consisting of two register RR1 or RR2 are cleared to zero by the load, continuity or resest command.

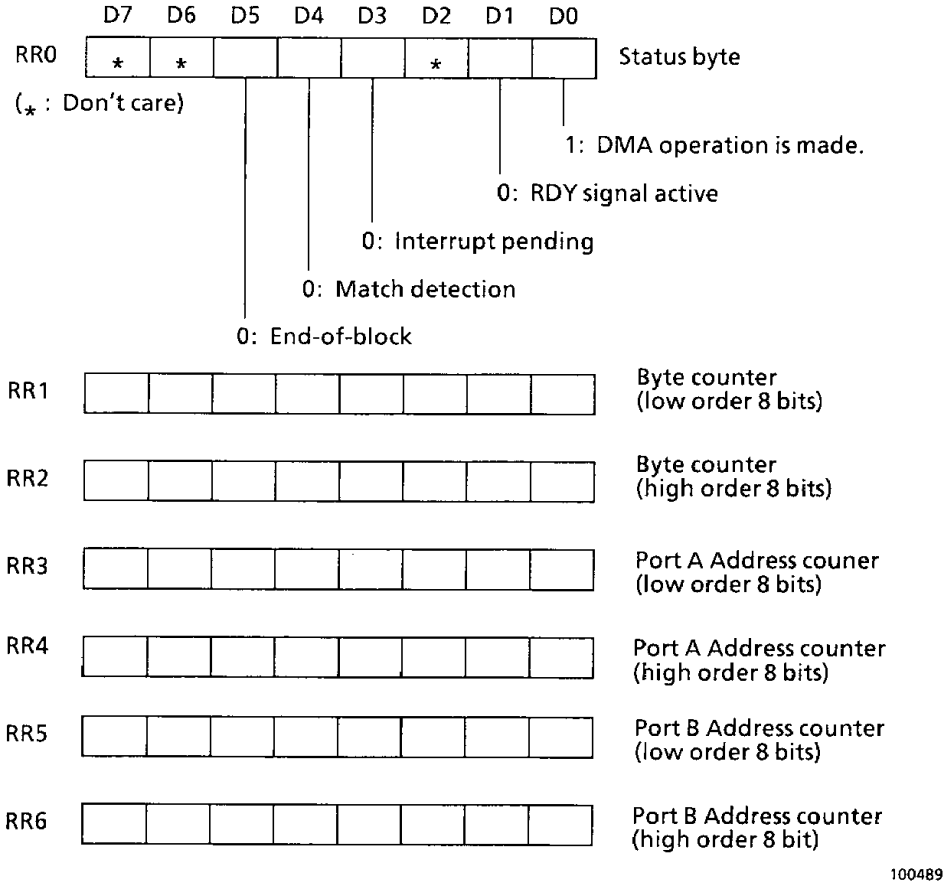



Figure 3.42 Read Register

When DMA starts the transfer or search, the byte counter is incremented by one at the end of each read cycle and judges the end-of-block by comparing with the program content of the block length register (WR0), when match is detected, DMA operation is stopped. If the pulse generation is used at this time, the content of the WR4 pulse control byte is, after transferred, compared with low order 4 byte (RR1) of the byte counter.

(3) Read register RR3, RR4 - Port A address counter

Write into the 16-bit counter consisting of two read registers RR3 and RR4 is made from WR0 port A start address register by the load command. Whenever one byte of DMA operation is carried out according to the designated content of WR0, this counter is updated (incremented or decremented) by one.

(4) Read register RR5, RR6 - Port B address counter

The 16-bit counter consisting of two read registers RR5 and RR6 indicates Port B address when DMA operation ended. Values in the port B address register (WR4) are loaded into this counter by the load command and the counter is updated by one every time when DMA operation is carried out by one byte. However, if address fix (Bit 4 and 5 of WR2) is programmed, the counter does not change. If port A or Port B is a fixed address destination port, in order to properly function the port it is necessary to program as described for the fixed address destination port.

### 3.4.3 Address counter and byte counter values when DMA operation ended.

Values of these counters when DMA operation ended are shown in Table 3.4 (a) and Table 3.4 (b).

Table 3.4 (a) Values of Those Counters when DMA Operation Ended

| Data format | Data transfer mode | Value of block length register | Number of byte to be transferred | Value of byte counter | Address counter value of source port | Address counter value of destinaion port |
|---|---|---|---|---|---|---|
| Transfer | Byte | N | N + 1 | N | As ± (N + 1) | As ± (N) |
| | Burst | N | N + 1 | N | As ± (N + 1) | As ± (N) |
| | Continuity | N | N + 1 | N | As ± (N + 1) | As ± (N) |
| Search | Byte | N | N + 1 | N | As ± (N + 1) | |
| | Burst | N | N + 1 | N | As ± (N + 1) | |
| | | | N + 2* | N + 1* | As ± (N + 2)* | |
| | Continuity | N | N + 1 | N | As ± (N + 1) | |
| | | | N + 2* | N + 1* | As ± (N + 2)* | |

As: Start address *: The values when N + 1 byte data is trasferred and RDY signal is active using 2-cycle valiable timing.

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Table 3.4 (b) Values of Those Counters when DMA Operation Ended

| Data format | Data transfer mode | Byte no. to be detected | Number of byte to be transferred | Value of byte counter | Address counter value of source port | Address counter value of destination port |
|---|---|---|---|---|---|---|
| Transfer | Byte | M | M | M-1 | As ± (M) | As ± (M-1) |
| | Burst | M | M | M-1 | As ± (M) | As ± (M-1) |
| | Continuity | M | M | M-1 | As ± (M) | As ± (M-1) |
| Search | Byte | M | M | M-1 | As ± (M) | |
| | Burst | M | M + 1 | M | As ± (M + 1) | |
| | | | M* | M-1* | As ± (M)* | |
| | Continuity | M | M + 1 | M | As ± (M + 1) | |
| | | | M* | M-1* | As ± (M)* | |

As : Start address * : The values when match is detected and RDY signal is active.

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## 3.4.4 List of command (1/3)

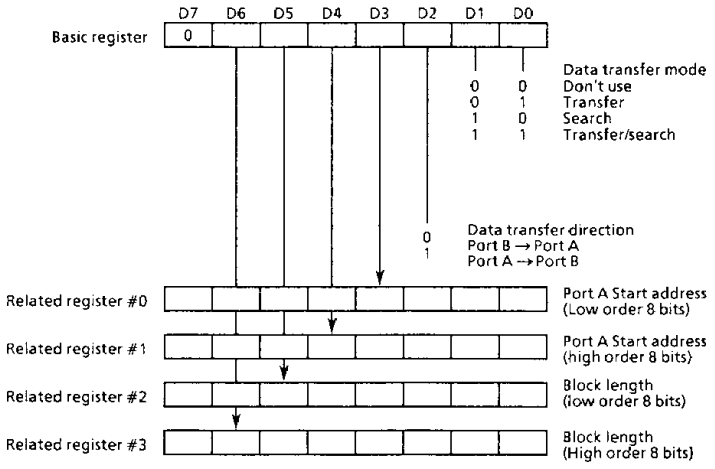


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Figure 3.35 Write Register WR0

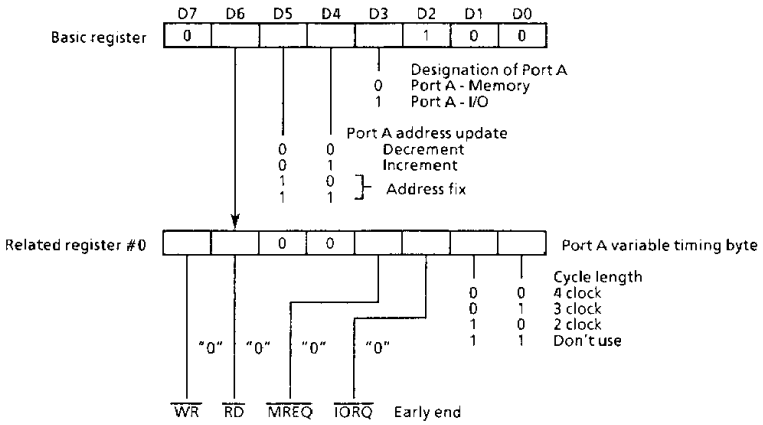


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Figure 3.36 Write Register WR1

List of command (2/3)

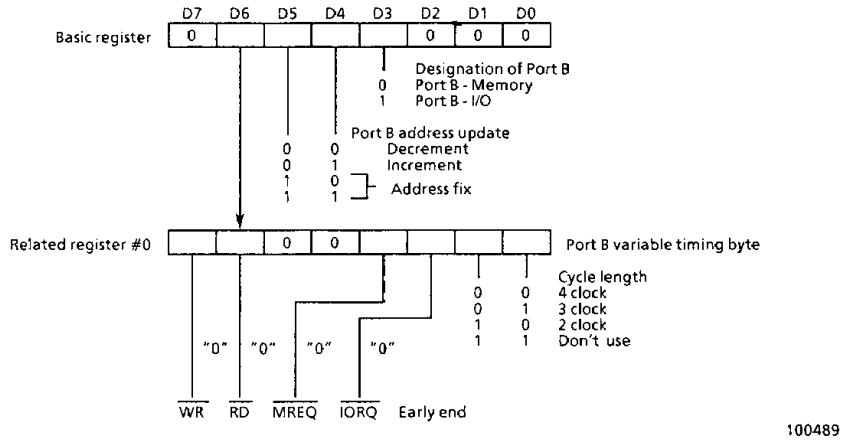


Figure 3.37 Write Register WR2

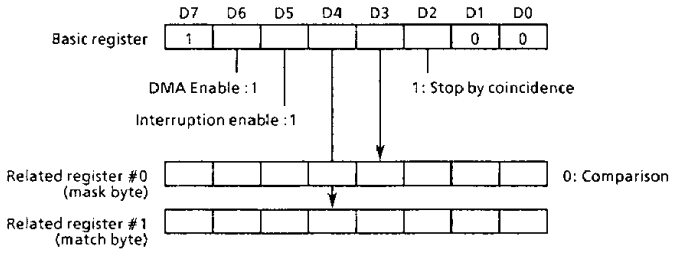


Figure 3.38 Write Register WR3

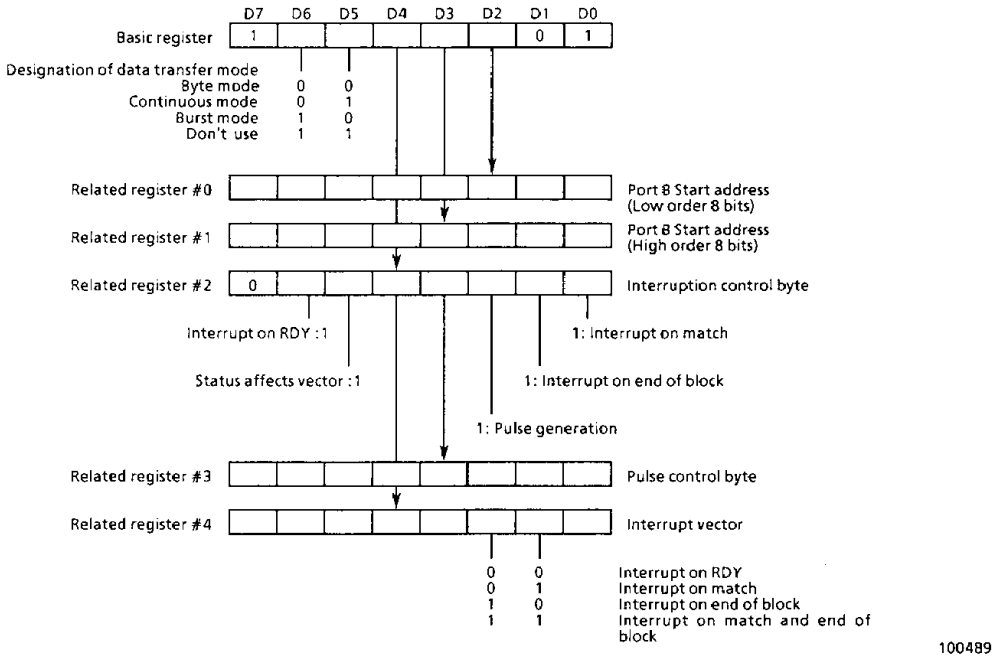


Figure 3.39 Write Register WR4

List of command (3/3)

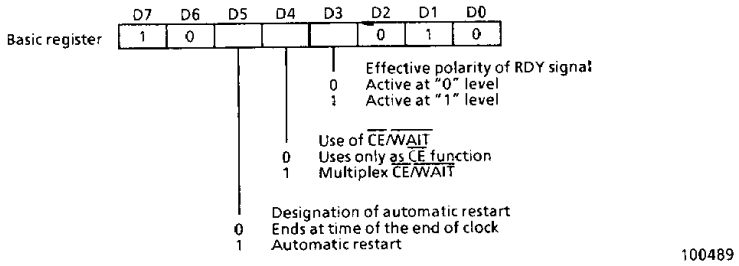


Figure 3.40 Write Register WR5

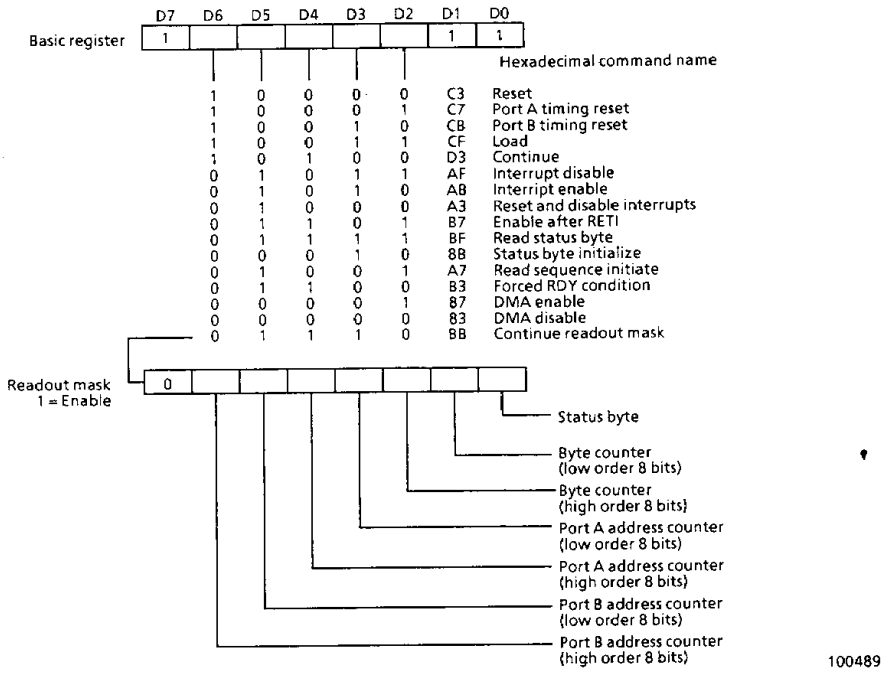


Figure 3.41 Write Register WR6

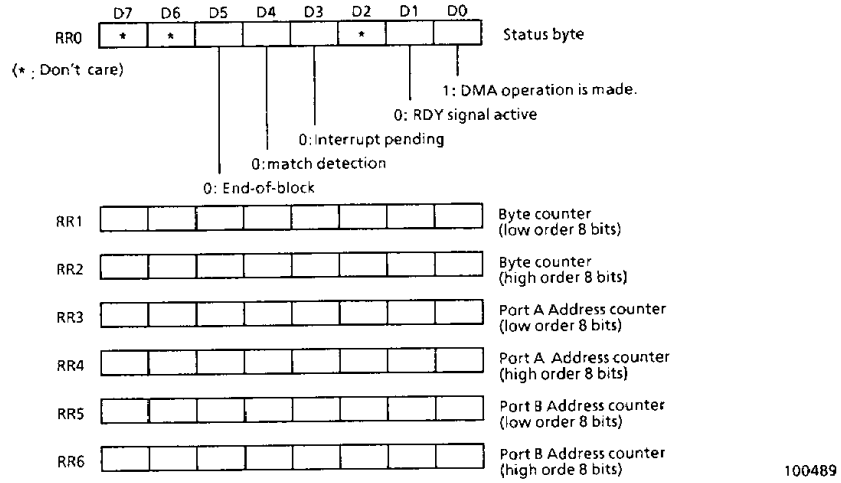


Figure 3.42 Read Register

3.5 METHOD OF USE

(1) Example of interface

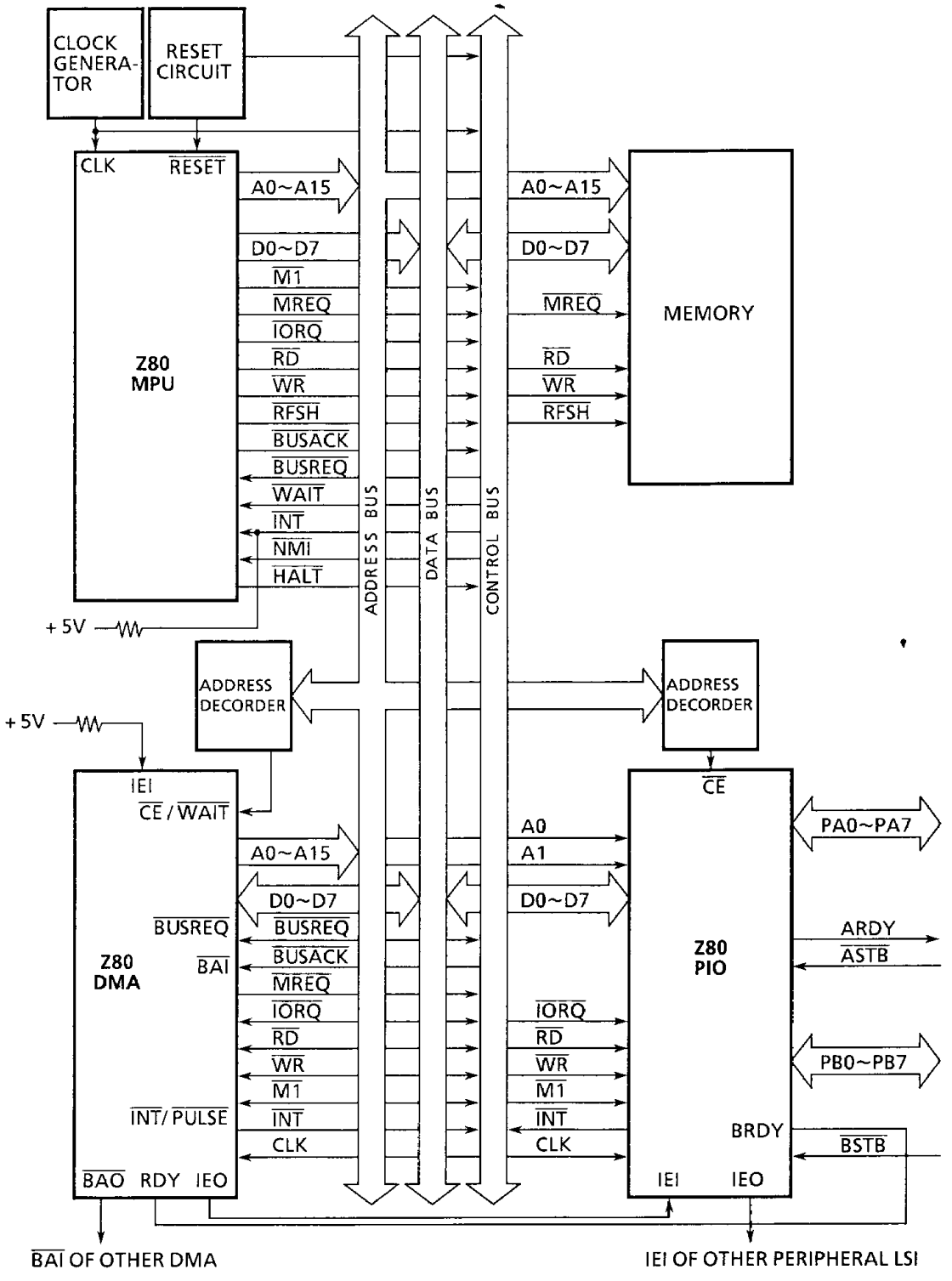


Figure 3.43 Example of Z80 System Interface

As the method of use of DMA using the Z80 family, a simple example of the Z80 system interface is shown below. Figure 3.43 shows the connection employing the Z80MPU, Z80DMA, Z80PIO, and MEMORY.

On the Z80 sistem, signal lines of MPU and peripheral devices are connected almost directly. In Figure 3.43, priority is in the order of DMA and PIO. This is because the connection is made according to the daisy chanin method which is peculiar to the Z80 system. In the case of DMA, espescially, in order to operate as a bus controller, $\overline{\text{BUSACK}}$ signal, which is the output of MPU, is input to BAI of DMA by the bus request daisy chain. When several units of DMA are used, BAO is connect to BAI of DMA which has the next higher priority. Hardware can be easily connected as shown in Figure 3.43. In addtion, memory mapped I/O also can be connected to DMA.

(2) Program example

As a program example of DMA operation, an example of transfer from I/O to memory using PIO is shown.

```
                        .Z80
                ;       Z80 DMA DATA TRANSFER
                ;       I/O TO MEMORY
                ;       (PIO PORT B)
                ;
0020            DPIOB   EQU   20H           ;DATA PIO CHANNEL B
0021            DPIOB   EQU   DPIOB+1       ;CONTROL PIO CHANNEL B
0030            DMA     EQU   30H           ;DMA ADDRESS
2000            DSTN    EQU   2000H         ;DESTINATION
0100            LENGTH  EQU   256           ;BLOCK LENGTH
                ;
                        ORG   1000H
1000' F3        STRT:   DI
1001' 3E 10             LD    A,10H
1003' ED 47             LD    I,A
1005' ED 5E             IM    2             ;INTERRUPT MODE 2
                ;
                ;   PIO B INITIALIZATION
1007' 3E 4F             LD    A,4FH         ;MODE 1
1009' D3 21             OUT   (CPIOB),A
100B' 3E 07             LD    A,07H
100D' D3 21             OUT   (CPIOB),A
                ;
                ;   DMA RESET
100F' 3E C3             LD    A,0C3H
1011' 06 06             LD    B,06H
1013' D3 30     DMRT:   OUT   (DMA),A
1015' 10 FC             DJNZ  DMRT
                ;
                ;   DMA INITIALIZATION
1017' 06 12             LD    B,DMAFIN-DMACTA
1019' 0E 30             LD    C,DMA
101B' 21 104E'          LD    HL,DMACTA
101E' ED B3             OTIR
```

```
1020'  FB                EI
1021'  C9                RET
                  ;
                  ;    INTERRUPT ON READY
1022'  76         IOR:   HALT
                  ;
                  ;    INTERRUPT ON MATCH
1023'  76         IOM:   HALT
                  ;
                  ;    INTERRUPT ON END OF BLOCK
1024'  CD 1037'   IOE:   CALL  SAV
1027'  3E 8B             LD    A,8BH
1029'  32 0030           LD    (DMA),A
102C'  06 04             LD    B,DMAFIN-DMACTB
102E'  0E 30             LD    C,DMA
1030'  21 105C'          LD    HL,DMACTB
1033'  ED B3             OTIR
1035'  C9                RET
                  ;
                  ;    INTERRUPT ON MATCH,END OF BLOCK
1036'  76         IME:   HALT
                  ;
                  ;    REGISTER SAVE
1037'  E3         SAV:   EX    (SP),HL
1038'  D5                PUSH  DE
1039'  C5                PUSH  BC
103A'  F5                PUSH  AF
103B'  DD E5             PUSH  IX
103D'  FD E5             PUSH  IY
103F'  CD 104D'          CALL  RUN
1042'  FD E1             POP   IY
1044'  DD E1             POP   IX
1046'  F1                POP   AF
1047'  C1                POP   BC
1048'  D1                POP   DE
1049'  E1                POP   HL
104A'  FB                EI
104B'  ED 4D             RETI
                  ;
104D'  E9         RUN:   JP    (HL)
                  ;
                  ;    DMA COMMAND TABLE
                  ;      PORT A - MEMORY
                  ;      PORT B - PIO CHANNEL B
104E'             DMACTA EQU   $
104E'  C3                DEFB  0C3H          ;WR6   RESET COMMAND
104F'  7D                DEFB  7DH           ;WR0   PORT A TO PORT B (TEMP)
1050'  2000              DEFW  DSTN          ;      DESTINATION ADDRESS
1052'  00FF              DEFW  LNGTH-1       ;      BLOCK LENGTH
1054'  14                DEFB  14H           ;WR1   PORT A - "INCREMENT" ADDRESS
1055'  28                DEFB  28H           ;WR2   PORT B - "FIXED" ADDRESS
1056'  A0                DEFB  0A0H          ;WR3   ENABLE INTERRUPT
1057'  95                DEFB  95H           ;WR4   BYTE MODE TRANSFER
1058'  20                DEFB  DPIOB         ;      PORT B ADDRESS (L)
```

```
1059'  32              DEFB  32H           ;       IOE,STATUS AFFECTS VECTOR
105A'  FF              DEFB  INTV-STRT     ;INTV   INTERRUPT VECTOR
105B'  82              DEFB  82H           ;WR5    RDY ACTIVE 'LOW',CE/ ONLY
105C'          DMACTB  EQU   $
105C'  CF              DEFB  0CFH          ;WR6    LOAD ADDRESS TO PORT A

105D'  01              DEFB  01H           ;WR0    PORT B TO PORT A
105E'  CF              DEFB  0CFH          ;WR6    LOAD ADDRESS TO PORT B
105F'  87              DEFB  87H           ;WR6    ENABLE DMA
1060'          DMAFIN  EQU   $
               ;
                       ORG   STRT+0FFH
10FF'  1022'   INTV:   DEFW  IOR
1101'  1023'           DEFW  IOM
1103'  1024'           DEFW  IOE
1105'  1036'           DEFW  IME
                       END
```

# 4. ELECTRICAL CHARACTERISTICS

## 4.1 ABSOLUTE MAXIMUM RATINGS

| Symbol | Item | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | − 0.5 to + 7 | V |
| $V_{IN}$ | Input Voltage | − 0.5 to VCC + 0.5 | V |
| $P_D$ | Power Diddipation (TA = 85°C) | 250 | mW |
| $T_{SOLDER}$ | Soldering Temperature (10 sec) | 260 | °C |
| $T_{STG}$ | Storage Temperature | − 65 to 150 | °C |
| $T_{OPR}$ | Operating Temperature | − 40 to 85 | °C |

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## 4.2 DC ELECTRICAL CHARACTERISTICS

$T_A = -40°C$ to $85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

| SYMBOL | PARAMETER | TEST CONDITION | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| VILC | Low Clock Input Voltage | | | − 0.3 | — | 0.6 | V |
| VIHC | High Clock Input Voltage | | | $V_{CC}$ − 0.6 | — | $V_{CC}$ + 0.3 | V |
| VIL | Low Inpur Voltage (Except CLK) | | | − 0.5 | — | 0.8 | V |
| VIH | High Input Voltage (Except CLK) | | | 2.2 | — | $V_{CC}$ | V |
| VOL | Output Low Voltage | IOL = 2.0mA<br>$\overline{BUSREQ}$ only 3.2mA | | — | — | 0.4 | V |
| VOH1 | Output High Voltage ( I ) | IOH = − 1.6mA | | 2.4 | — | — | V |
| VOH2 | Output High Voltage (II) | IOH = − 250μA | | $V_{CC}$ − 0.8 | — | — | V |
| ILI | Input Leak Current | $V_{SS} \leqq V_{IN} \leqq V_{CC}$ | | — | — | ± 10 | μA |
| ILO | Output Leak Current | $V_{SS} + 0.4 \leqq V_{IN} \leqq V_{CC}$ | | — | — | ± 10 | μA |
| ICC1 | Power Supply Current | $V_{CC}$ = 5V<br>$f_{CLK}$ = (1)<br>$V_{IHC} = V_{IH}$<br>$= V_{CC}$-0.2V<br>$V_{ILC} = V_{IL}$<br>= 0.2V | AP-6/AM-6<br>/AT-6 | — | 6 | 10 | mA |
| ICC2 | Standby Supply Current | $V_{CC}$ = 5V<br>$V_{IHC} = V_{IH} = V_{CC}$-0.2V<br>$V_{ILC} = V_{IL}$ = 0.2V | | — | 0.5 | 10 | μA |

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Note 1 : fCLK = 1/TcC (MIN.)

## 4.3 AC ELECTRICAL CHARACTERISTICS

### 4.3.1 AC characteritics ( I )

When operate as peripheral devices (inactive state)

TA = −40℃ to 85℃, VCC = 5V ± 10%, VSS = 0V

| NO. | SYMBOL | PARAMETER | AP-6/AM-6/AT-6 (6MHz) | | UNIT |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| 1 | $T_CC$ | CLock cycle time | 165 | DC | ns |
| 2 | TwCh | High clock pulse width | 65 | DC | ns |
| 3 | TwCl | Low clock pulse width | 65 | DC | ns |
| 4 | TrC | Clock rise time | — | 20 | ns |
| 5 | TfC | Clock fall time | — | 20 | ns |
| 6 | Th | Hold time | 0 | — | ns |
| 7 | TsC (Cr) | $\overline{IORQ}$, $\overline{WR}$ and $\overline{CE}$ signals set-up time for clock rise | 60 | — | ns |
| 8 | TdD0 (RDf) | Delay from $\overline{RD}$ rise to data output | — | 300 | ns |
| 9 | TsWM (Cr) | Data input set-up time for clock rise (write and $\overline{M1}$ cycle) | 30 | — | ns |
| 10 | TdCf (D0) | Delay from $\overline{IORQ}$ fall to data output (INTA cycle) | — | 100 | ns |
| 11 | TsRD (Dz) | Delay from $\overline{RD}$ rise to data bus float state | — | 70 | ns |
| 12 | TsIEI (IORQ) | IEI set-up time for $\overline{IORQ}$ fall (INTA cycle) | 100 | — | ns |
| 13 | TdIEOr (IEIr) | Delay from IEI rise to IEO rise | — | 70 | ns |
| 14 | TdIEOf (IEIf) | Delay from IEI fall to IEO fall | — | 70 | ns |
| 15 | TdM1 (IEO) | Delay from $\overline{M1}$ fall to IEO fall (When interrupt is generated immediately before $\overline{M1}$ cycle.) | — | 100 | ns |
| 16 | TsM1f (Cr) | $\overline{M1}$ signal set-up time for clock rise | 70 | — | ns |
| 17 | TsM1r (Cf) | $\overline{M1}$ signal set-up time for clock fall | −10 | — | ns |
| 18 | TsRD (Cr) | $\overline{RD}$ signal set-up time for clock rise ($\overline{M1}$ cycle) | 60 | — | ns |
| 19 | TdI ($\overline{INT}$) | Delay from interruption generation to $\overline{INT}$ fall (at inactive state) | — | 450 | ns |
| 20 | TdBAIr (BAOr) | Delay from $\overline{BAI}$ rise to $\overline{BAO}$ rise | — | 100 | ns |
| 21 | TdBAIf (BAOf) | Delay from $\overline{BAI}$ fall to $\overline{BAO}$ fall | — | 100 | ns |
| 22 | TsRDY (Cr) | RDY signal set-up time for clock rise | 50 | — | ns |

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4.3.2 AC charateristics (II) (1/2)

When operate as bus controller (active state)

TA = −40℃ to 85℃, VCC = 5V ± 10%, VSS = 0V

| NO. | SUMBOL | PARAMETER | AP-6/AM-6/AT-6 (6MHz) | | UNIT |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| 1 | $T_CC$ | Clock cycle time | 165 | DC | ns |
| 2 | TwCh | High clock pulse width | 65 | DC | ns |
| 3 | TwCl | Low clock pulse width | 65 | DC | ns |
| 4 | TrC | Clock rise time | — | 20 | ns |
| 5 | TfC | Clock fall time | — | 20 | ns |
| 6 | TdA | Delay of address output | — | 90 | ns |
| 7 | TdC (Az) | Delay from clock rise to address bus float state | — | 80 | ns |
| 8 | TsA (MREQ) | Address set-up time for $\overline{MREQ}$ fall (memory cycle) | 35 | — | ns |
| 9 | TsA (IRW) | Address set-up time for $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$ fall (I/O cycle) | 110 | — | ns |
| 10 | TdRW (A) | Address hold time from $\overline{RD}$, $\overline{WR}$ rise | 35 | — | ns |
| 11 | TdRW (Az) | Address hold time from $\overline{RD}$, $\overline{WR}$ rise (at float state) | 65 | — | ns |
| 12 | TdCf (D0) | Delay from clock fall to data output | — | 130 | ns |
| 13 | TdCr (Dz) | Delay from clock rise to data bus float state (write cycle) | — | 70 | ns |
| 14 | TsDI (Cr) | Data input set-up time up to clock rise (read cycle in which $\overline{RD}$ ended at clock rise) | 30 | — | ns |
| 15 | TsDI (Cf) | Data input set-up time up to clock fall (read cycle in which RD ended at clock fall) | 40 | — | ns |
| 16 | TsDO (WfM) | Data output set-up time up to $\overline{WR}$ fall (memory cycle) | 25 | — | ns |
| 17 | TsDO (WfI) | Data output set-up time up to $\overline{WR}$ fall (I/O cycle) | -55 | — | ns |
| 18 | TdWr (D0) | Data hold time from WR rise | 30 | — | ns |
| 19 | Th | Hold time | 0 | — | ns |
| 20 | TdCr (Mf) | Delay from clock rise to $\overline{MREQ}$ fall | — | 70 | ns |
| 21 | TdCf (Mf) | Delay from clock fall to $\overline{MREQ}$ fall | — | 70 | ns |
| 22 | TdCr (Mr) | Delay from clock rise to $\overline{MREQ}$ rise | — | 70 | ns |
| 23 | TdCf (Mr) | Delay from clock fall to $\overline{MREQ}$ rise | — | 70 | ns |

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AC characteristics (II) (2/2)

| NO. | SYMBOL | PARAMETER | AP-6/AM-6/AT-6 (6MHz) | | UNIT |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| 24 | TwMl | Low $\overline{MREQ}$ pulse width | 135 | — | ns |
| 25 | TwMh | High $\overline{MREQ}$ pulse width | 65 | — | ns |
| 26 | TdCf (If) | Delay from clock fall to $\overline{IORQ}$ fall | — | 70 | ns |
| 27 | TdCr (If) | Delay from clock rise to $\overline{IORQ}$ fall | — | 65 | ns |
| 28 | TdCr (Ir) | Delay from clock rise to $\overline{IORQ}$ rise | — | 70 | ns |
| 29 | TdCf (Ir) | Delay from clock fall to $\overline{IORQ}$ rise | — | 70 | ns |
| 30 | TdCr (Rf) | Delay from clock rise to $\overline{RD}$ fall | — | 70 | ns |
| 31 | TdCf (Rf) | Delay from clock fall to $\overline{RD}$ fall | — | 80 | ns |
| 32 | TdCr (Rr) | Delay from clock rise to $\overline{RD}$ rise | — | 70 | ns |
| 33 | TdCf (Rr) | Delay from clock fall to $\overline{RD}$ rise | — | 70 | ns |
| 34 | TdCr (Wf) | Delay from clock rise to $\overline{WR}$ fall | — | 60 | ns |
| 35 | TdCf (Wf) | Delay from clock fall to $\overline{WR}$ fall | — | 60 | ns |
| 36 | TdCr (Wr) | Delay from clock rise to $\overline{WR}$ rise | — | 70 | ns |
| 37 | TdCf (Wr) | Delay from clock fall to $\overline{WR}$ rise | — | 70 | ns |
| 38 | TwWl | Low $\overline{WR}$ pulse width | 135 | — | ns |
| 39 | TsWA (Cf) | $\overline{WAIT}$ signal set-up time for clock fall | 60 | — | ns |
| 40 | TdCr (B) | Delay from clock rise up to $\overline{BUSREQ}$ signal | — | 90 | ns |
| 41 | TdCr (Iz) | Delay from clock rise to $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$ signal float state | — | 70 | ns |

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VIH = 2.4V, VIL = 0.4V, VIHC = VCC − 0.6V, VILC = 0.6V
VOH = 2.2V, VOL = 0.8V, CL = 100pF

## 4.4 CAPACITANCE

TA = 25°C

| SYNBOL | ITEM | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| CCLOCK | Clock Input Capacitance | f = 1MHz<br>All terminals except that to be measured should be earthed. | — | — | 5 | pF |
| CIN | Input Capacitance | | — | — | 5 | pF |
| COUT | Output Capacitance | | | | 10 | pF |

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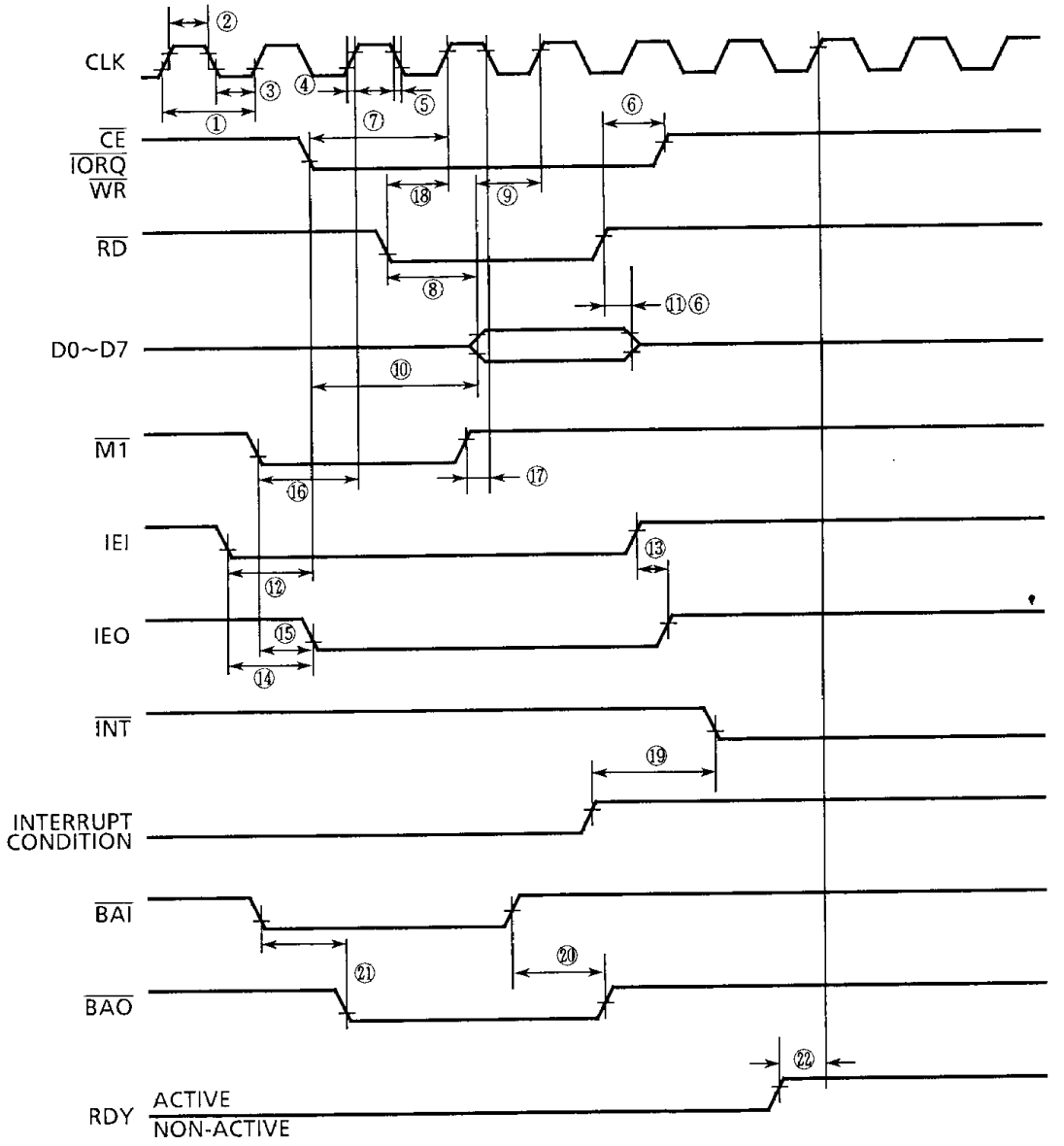
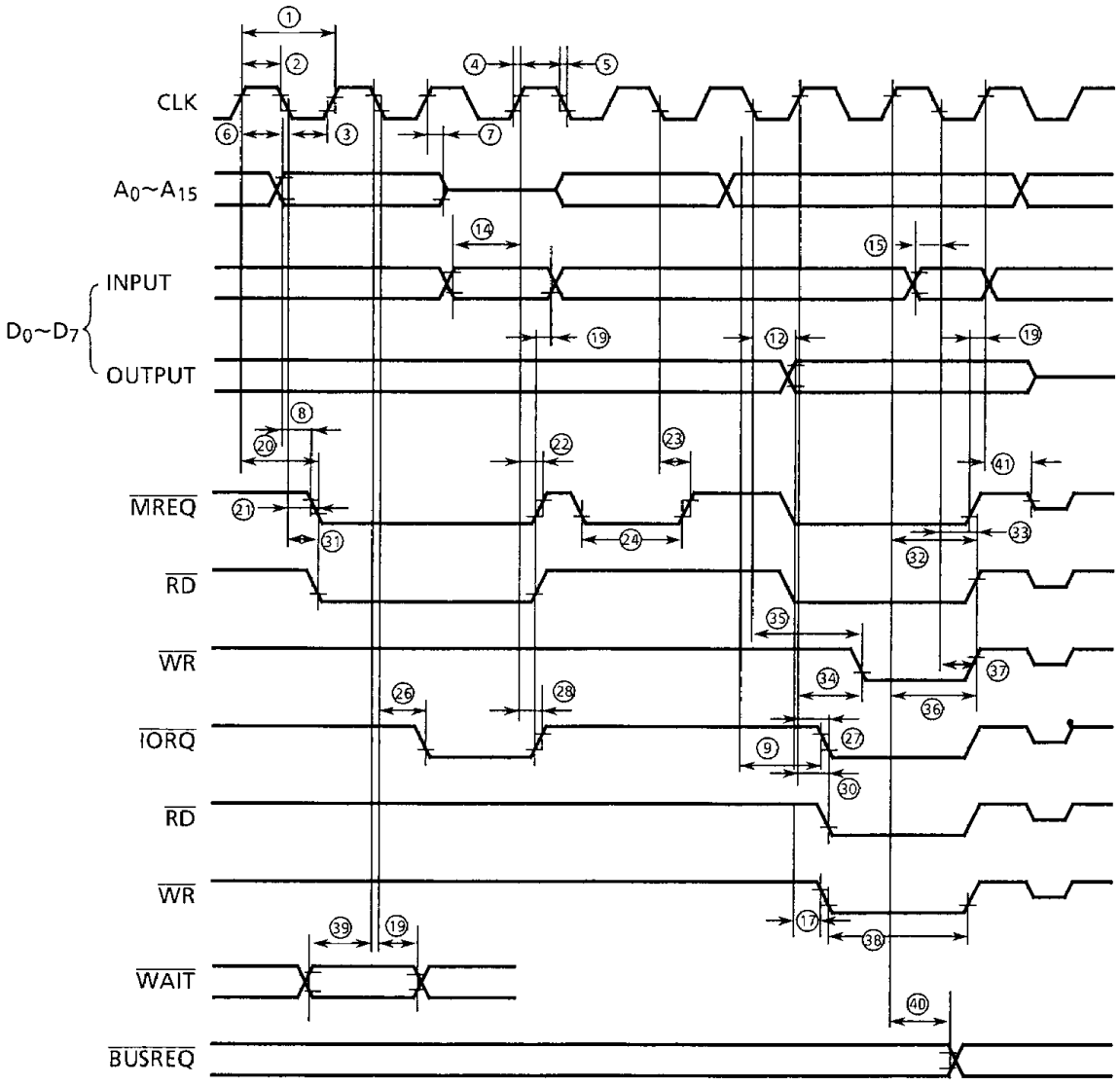
## 4.5 TIMING DIAGRAM

Numbers shown in the following figures correspond with those in the 4.3 A.C. Electrical Characteristics Table.

(1) When operate as peripheral devices (inactive state)



(2) When operate as bus controller (active state)

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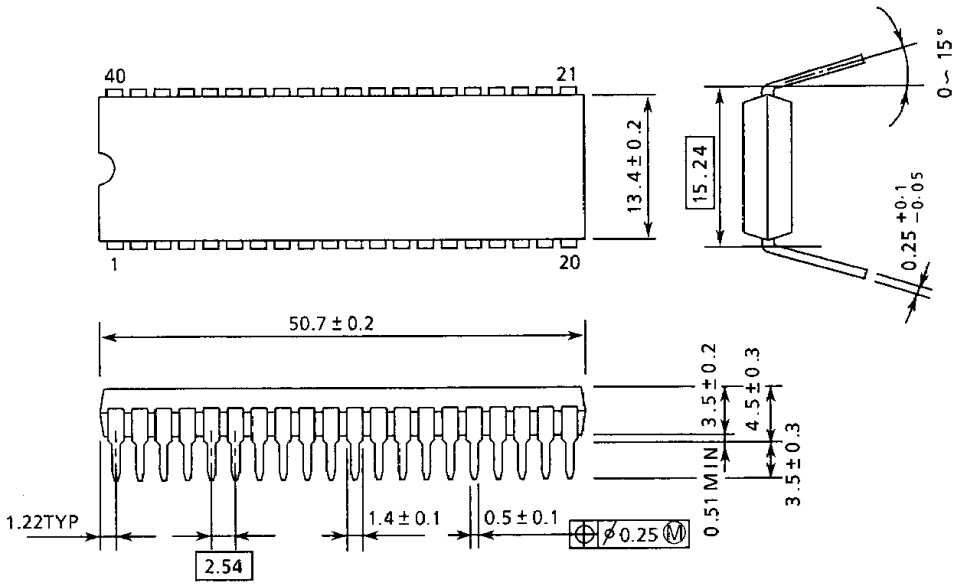
# 5. EXTERNAL DIMENSION VIEW

## 5.1 DIP PACKAGE

DIP40-P-600

Unit : mm

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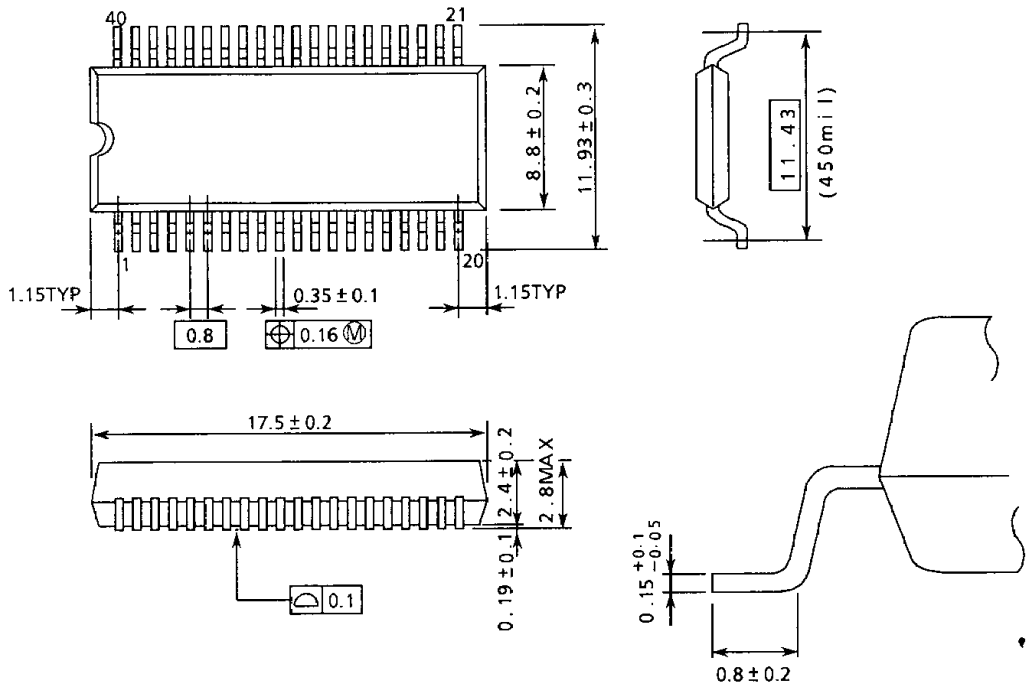
Note 1 : This dimension is measured at the center of bending point of leads.

Note 2 : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.40 leads.

## 5.2 SOP PACKAGE

SSOP40-P-450

Unit : mm

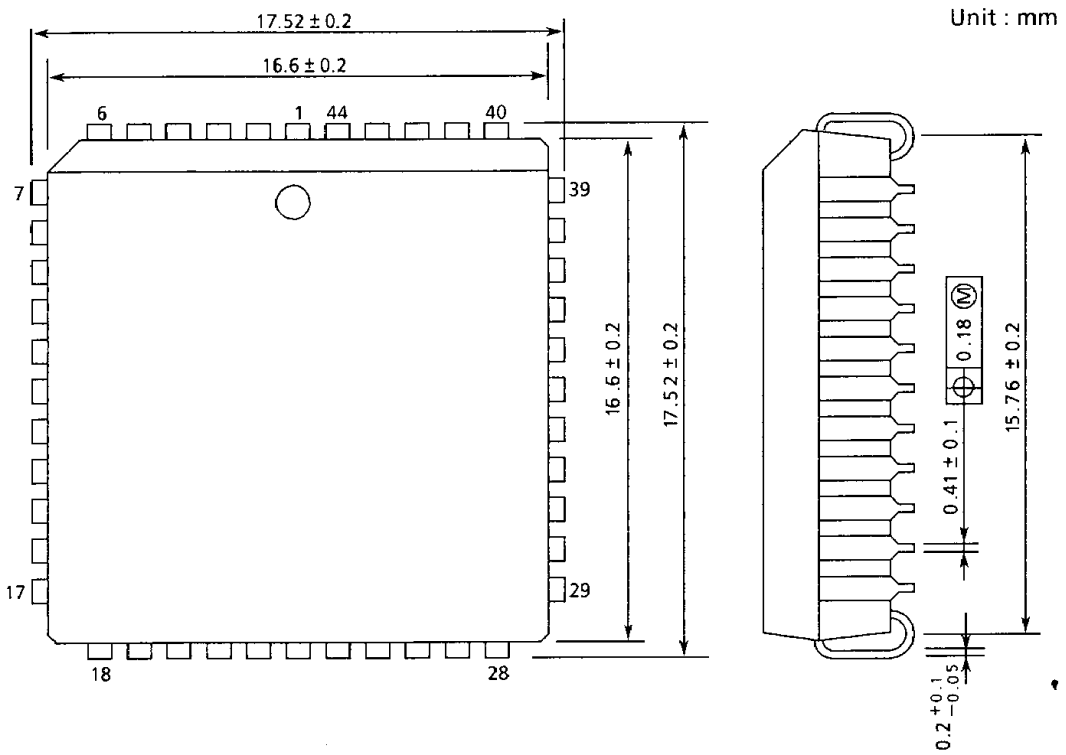


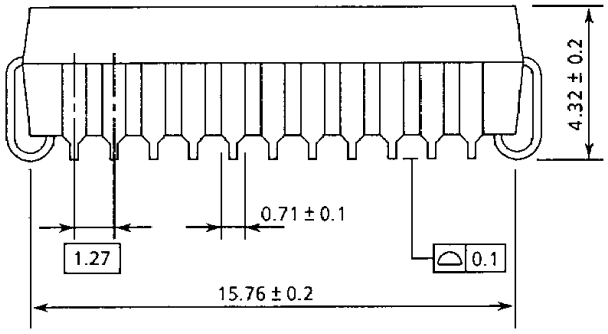

Note : Package Width and length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.

5.3 44-PIN PLCC PACKAGE

QFJ44-P-S650

Unit : mm

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# 6. PRECAUTIONS

No special care is required in the Z80 system designing employing DMA but it is necessary to fully understand the basic timings and commands shown in 3. Operational Description.

For the basic timings, please refer to the precautions in 3.3.2 (1).

For the commands, care shall be taken to the programming as there are many registers and setup is considerably complictated.

As the precaution for the programming, the "fixed address destinaion port programming" is briefly described. When Port A is assumed to be the "fixed address destination port", address can be loaded in the following stepe:

(1) Write Port A address into WR0.

(2) Designate Port A as the source port. (Set up temporarily)

(3) Load Port A address on the address counter. (Load command CFH)

(4) Write Port B start address into WR4.

(5) Convert Port A into the destination port.

(6) Load Port B start address on the address counter. (source port address)