TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT STATIC RAM

DESCRIPTION

The TC554161FTI is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5 V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10 mA/MHz (typ) and a minimum cycle time of 85 ns. It is automatically placed in low-power mode at 200 μA standby current (max) when chip enable ($\overline{CE}$) is asserted high. There are two control inputs. $\overline{CE}$ is used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. Data byte control pin ($\overline{LB}$, $\overline{UB}$) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of − 40° to 85°C, the TC554161FTI can be used in environments exhibiting extreme temperature conditions. The TC554161FTI is available in a plastic 54-pin thin-small-outline package (TSOP).

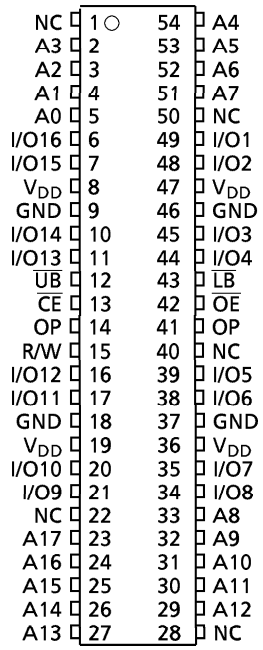
FEATURES

- Low-power dissipation
  Operating: 55 mW/MHz(typical)
- Standby current of 200 μA (maximum)
- Single power supply voltage of 5 V ± 10%
- Power down features using $\overline{CE}$.
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of − 40° to 85°C
- Access Times (maximum):

	TC554161FTI	
	-85	-10
Access Time	85 ns	100 ns
$\overline{CE}$ Access Time	85 ns	100 ns
$\overline{OE}$ Access Time	45 ns	50 ns

- Package:
  TSOP II 54-P-400-0.80 (FTI) (Weight: 0.55 g typ)

PIN ASSIGNMENT (TOP VIEW)



(Normal pinout)

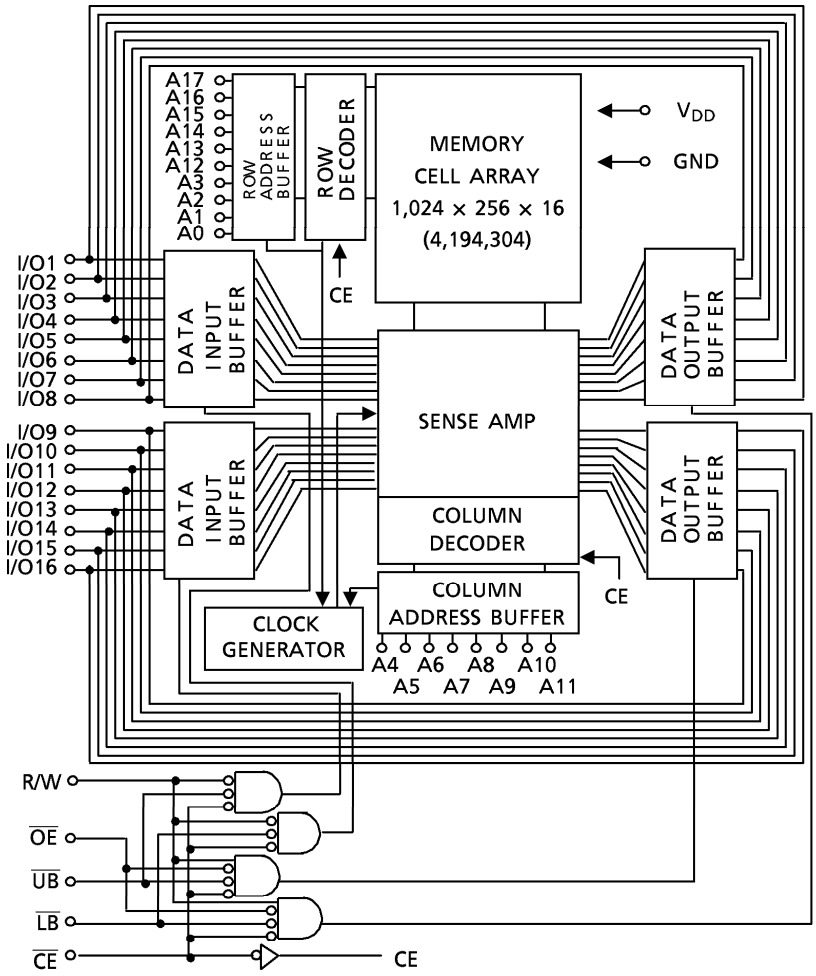
PIN NAMES

A0 to A17	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control Input
V_{DD}	Power (+ 5 V)
GND	Ground
NC	No Connection
OP*	Option

*: OP pin must be open or connected to GND.

961001EBA1

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 0.3 to 7.0	V
V_{IN}	Input Voltage	− 0.3 * to 7.0	V
$V_{I/O}$	Input/Output Voltage	− 0.5 to V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	− 55 to 150	°C
T_{opr}	Operating Temperature	− 40 to 85	°C

* − 3.0 V when measured at a pulse width of 30 ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = − 40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	− 0.3 *	−	0.6	V
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	V

* − 3.0 V when measured at a pulse width of 30 ns

DC CHARACTERISTICS (Ta = − 40° to 85°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}			−	−	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 V to VDD			−	−	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4 V			− 1.0	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V			2.1	−	−	mA
$I_{DDO\,1}$	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH}, I_{OUT} = 0 mA Other Inputs = V_{IH}/V_{IL}	Tcycle	min	−	−	100	mA
				1 μs	−	15	−	
$I_{DDO\,2}$		$\overline{CE}$ = 0.2 V R/W = V_{DD} − 0.2 V, I_{OUT} = 0 mA Other Inputs = V_{DD} − 0.2 V/0.2 V	Tcycle	min	−	−	90	mA
				1 μs	−	10	−	
$I_{DDS\,1}$	Standby Current	$\overline{CE}$ = V_{IH}			−	−	3	mA
$I_{DDS\,2}$		$\overline{CE}$ = V_{DD} − 0.2 V, Ta = − 40° to 85°C V_{DD} = 2.0 to 5.5 V			−	−	200	μA

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High-Z	Output	I_{DDO}
				L	H	Output	High-Z	I_{DDO}
Write	L	×	L	L	L	Input	Input	I_{DDO}
				H	L	High-Z	Input	I_{DDO}
				L	H	Input	High-Z	I_{DDO}
Outputs Disable	L	H	H	×	×	High-Z	High-Z	I_{DDO}
	L	×	×	H	H			
Standby	H	×	×	×	×	High-Z	High-Z	I_{DDS}

× = don't care
H = logic high
L = logic low

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = − 40° to 85°C, V_{DD} = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85		-10		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	Chip Enable Access Time	–	85	–	100	
t_{OE}	Output Enable Access Time	–	45	–	50	
t_{BA}	Data Byte Control Access Time	–	45	–	50	
t_{OH}	Output Data Hold Time	10	–	10	–	
t_{COE}	Chip Enable Low to Output Active	5	–	5	–	
t_{OEE}	Output Enable Low to Output Active	0	–	0	–	
t_{BE}	Data Byte Control Low to Output Active	0	–	0	–	
t_{OD}	Chip Enable High to Output High-Z	–	35	–	40	
t_{ODO}	Output Enable High to Output High-Z	–	35	–	40	
t_{BD}	Data Byte Control High to Output High-Z	–	35	–	40	

WRITE CYCLE

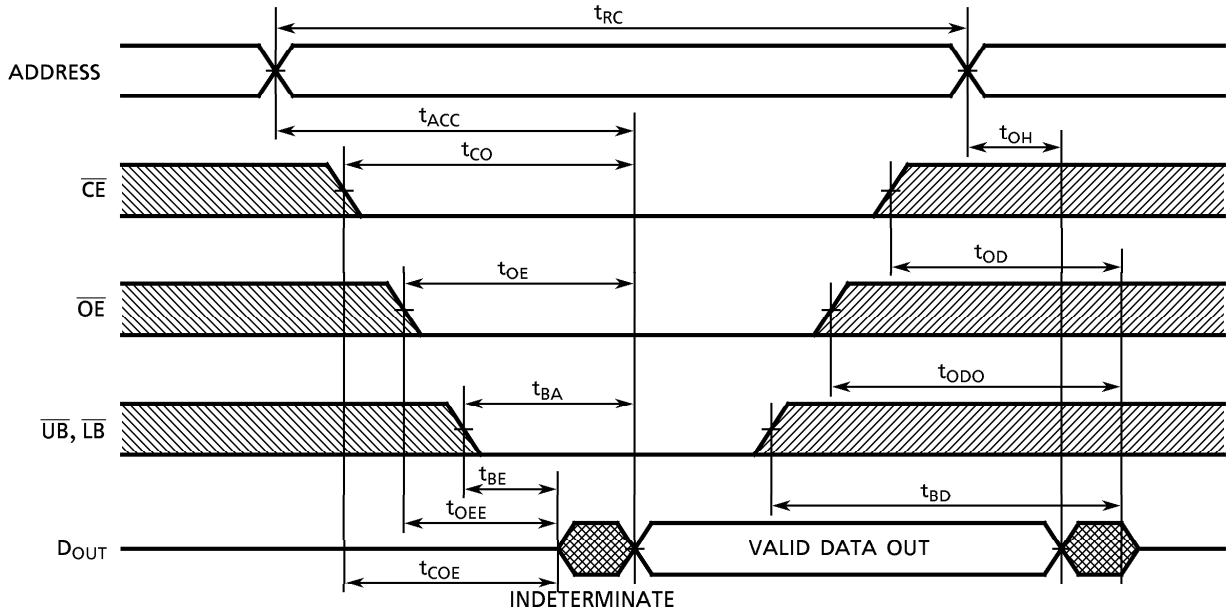
SYMBOL	PARAMETER	TC554161FTI				UNIT
		-85		-10		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	55	–	60	–	
t_{CW}	Chip Enable to End of Write	70	–	80	–	
t_{BW}	Data Byte Control to End of Write	55	–	60	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	35	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	R/W High to Output Active	0	–	0	–	
t_{ODW}	R/W Low to Output High-Z	–	35	–	40	

AC TEST CONDITIONS

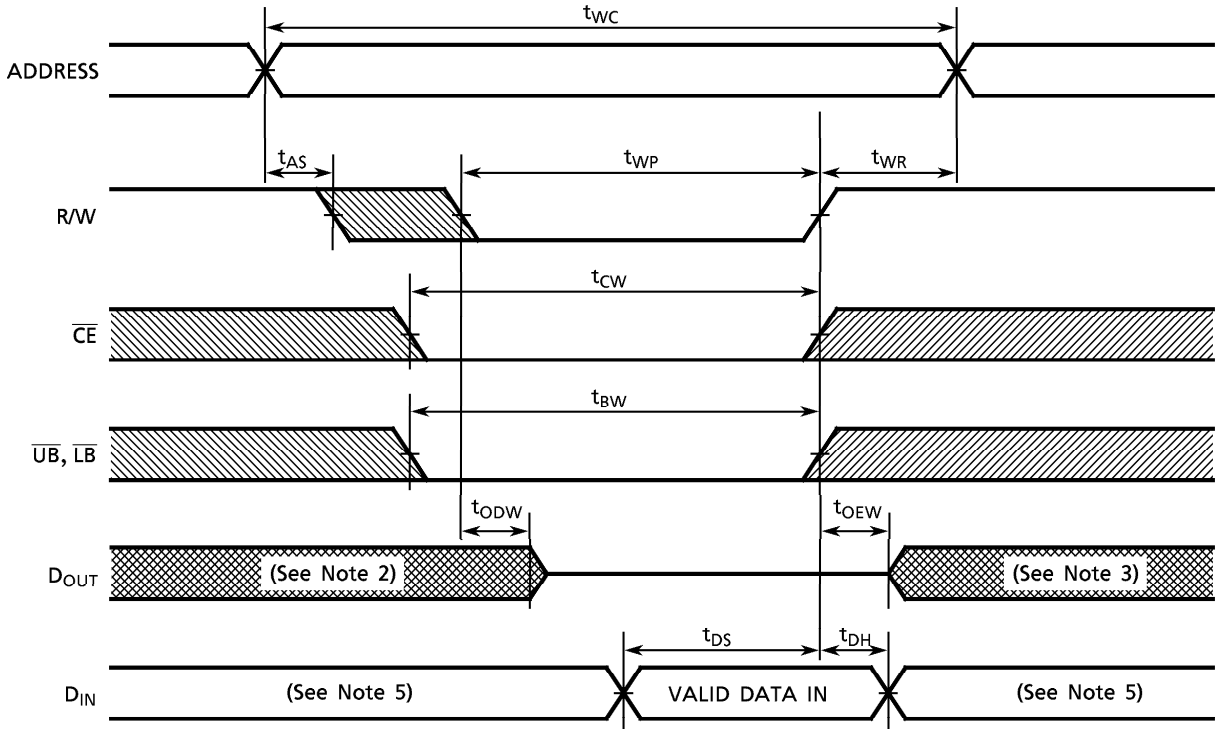
Output load: 100 pF + one TTL gate
Input pulse level: 0.4 V, 2.6 V
Timing measurements: 1.5 V
Reference level: 1.5 V
t_R, t_F: 5 ns

TIMING DIAGRAMS

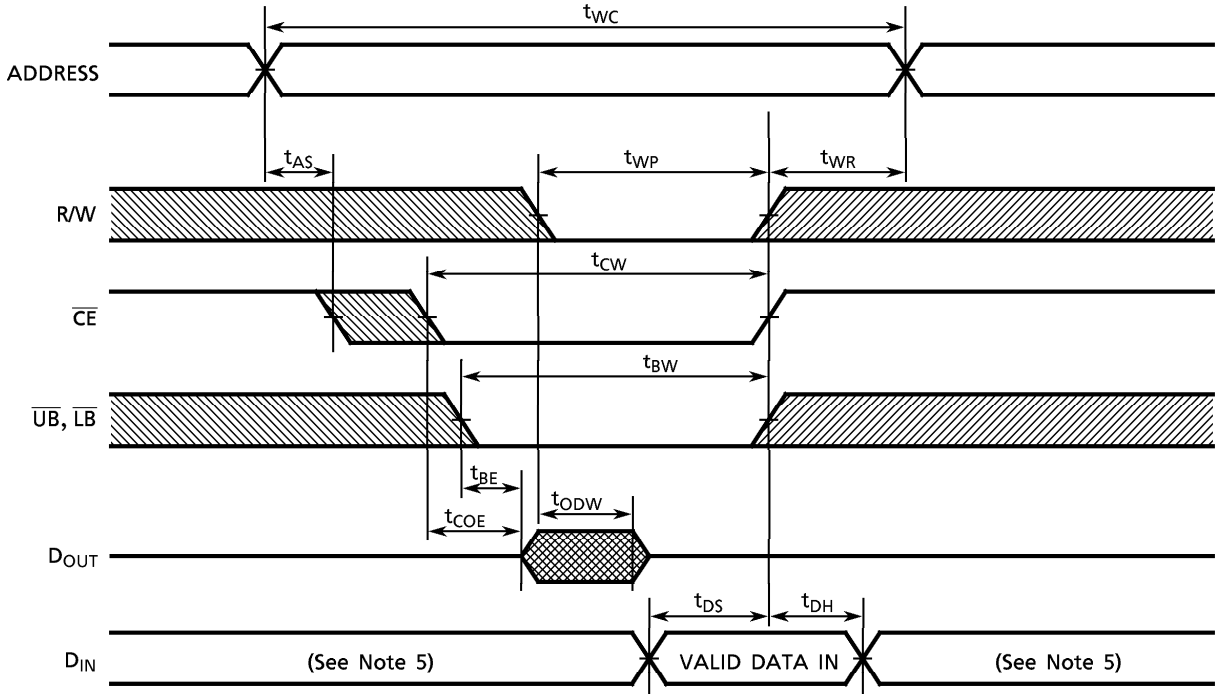
READ CYCLE (See Note 1)



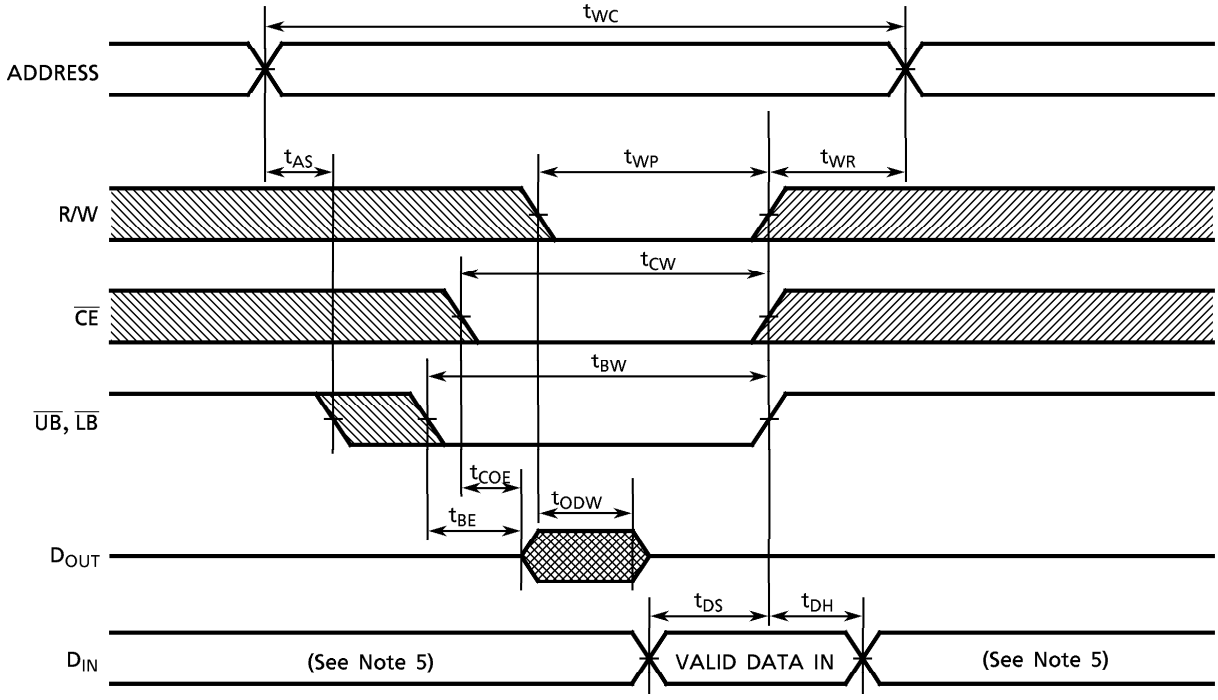
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 ($\overline{UB}$, $\overline{LB}$ CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE}$ goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE}$ goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

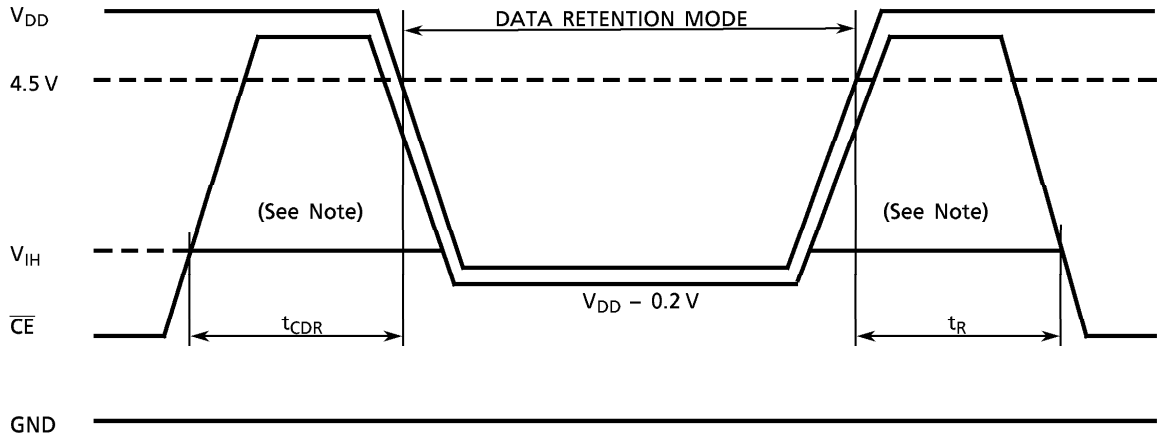
(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = – 40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DH} = 3.0 V	–	–	100	μA
		V_{DH} = 5.5 V	–	–	200	
t_{CDR}	Chip Deselect to Data Retention Mode Time		0	–	–	nS
t_R	Recovery Time		5	–	–	mS

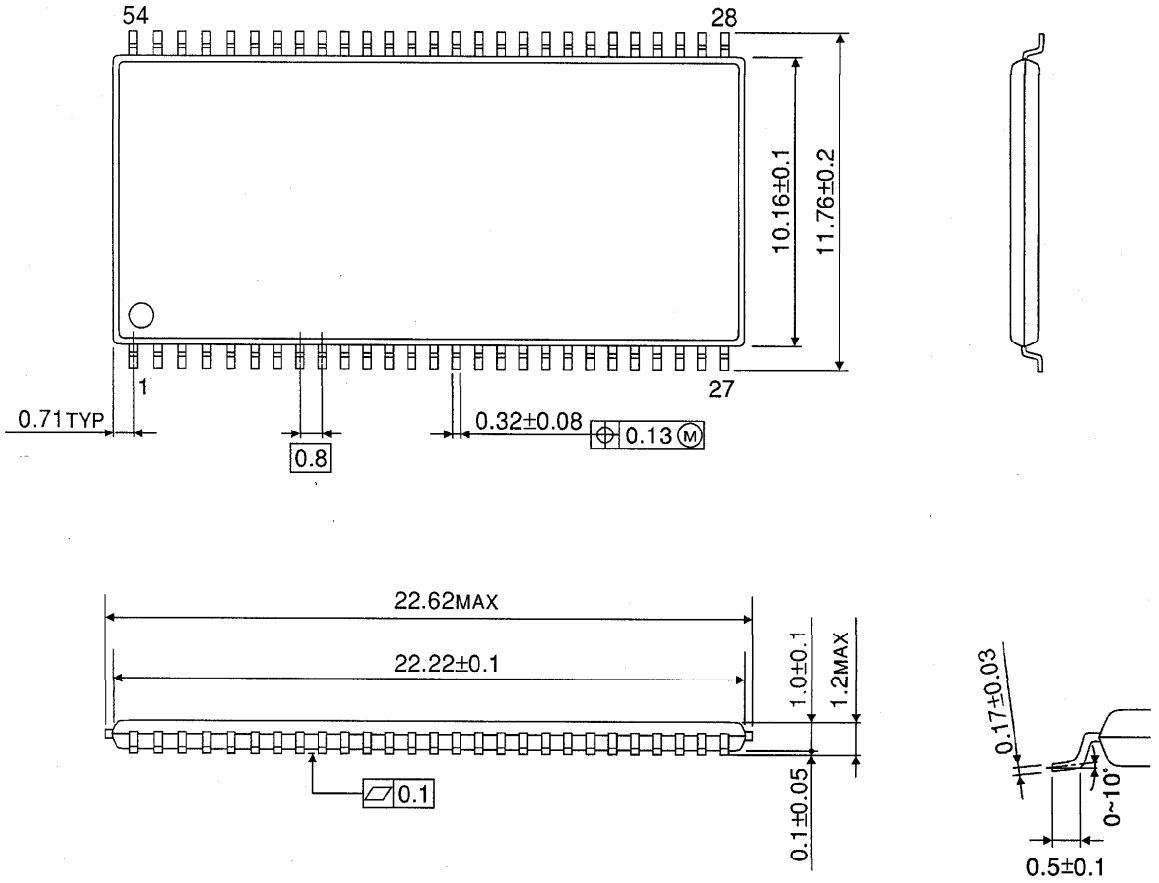
$\overline{CE}$ CONTROLLED DATA RETENTION MODE



Note: When $\overline{CE}$ is operating at the V_{IH} level (2.4 V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.6 V.

PACKAGE DIMENSIONS (TSOPII 54-P-400-0.80)

Units in mm



Weight: 0.55 g (typ)