Self-Contained Audio Preamplifier

SSM2017

FEATURES

Excellent Noise Performance: 950 pV/√Hz or 1.5 dB Noise Figure
Ultralow THD: < 0.01% @ G = 100 Over the Full Audio Band
Wide Bandwidth: 1 MHz @ G = 100
High Slew Rate: 17 V/μs typ
Unity Gain Stable
True Differential Inputs
Subaudio 1/f Noise Corner
8-Pin Mini-DIP with Only One External Component Required
Very Low Cost
Extended Temperature Range: –40°C to +85°C

APPLICATIONS

Audio Mix Consoles
Intercom/Paging Systems
Two-Way Radio
Sonar
Digital Audio Systems

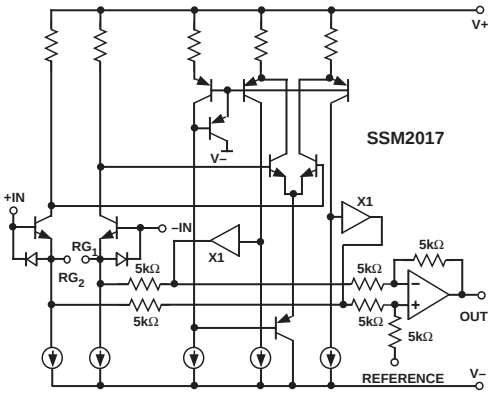
GENERAL DESCRIPTION

The SSM2017 is a latest generation audio preamplifier, combining SSM preamplifier design expertise with advanced processing. The result is excellent audio performance from a self-contained 8-pin mini-DIP device, requiring only one external gain set resistor or potentiometer. The SSM2017 is further enhanced by its unity gain stability.

Key specifications include ultralow noise (1.5 dB noise figure) and THD (<0.01% at G = 100), complemented by wide bandwidth and high slew rate.

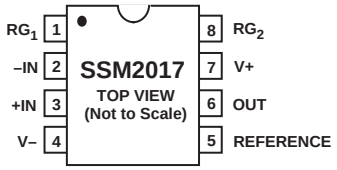
Applications for this low cost device include microphone preamplifiers and bus summing amplifiers in professional and consumer audio equipment, sonar, and other applications requiring a low noise instrumentation amplifier with high gain capability.

FUNCTIONAL BLOCK DIAGRAM

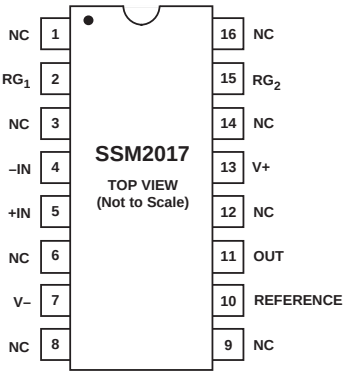


PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)



16-Pin Wide Body SOL (S Suffix)



NC = NO CONNECT

REV. C

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SSM2017–SPECIFICATIONS

(V_S = ±15 V and –40°C ≤ T_A ≤ +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DISTORTION PERFORMANCE		T_A = +25°C V_O = 7 V rms R_L = 5 kΩ				
Total Harmonic Distortion Plus Noise	THD+N	G = 1000, f = 1 kHz		0.012		%
		G = 100, f = 1 kHz		0.005		%
		G = 10, f = 1 kHz		0.004		%
		G = 1, f = 1 kHz		0.008		%
NOISE PERFORMANCE						
Input Referred Voltage Noise Density	e_n	f = 1 kHz, G = 1000		0.95		nV/√Hz
		f = 1 kHz; G = 100		1.95		nV/√Hz
		f = 1 kHz; G = 10		11.83		nV/√Hz
		f = 1 kHz; G = 1		107.14		nV/√Hz
Input Current Noise Density	i_n	f = 1 kHz, G = 1000		2		pA/√Hz
DYNAMIC RESPONSE						
Slew Rate	SR	G = 10 R_L = 4.7 kΩ C_L = 50 pF T_A = +25°C	10	17		V/µs
Small Signal Bandwidth	$BW_{-3\ dB}$	G = 1000		200		kHz
		G = 100		1000		kHz
		G = 10		2000		kHz
		G = 1		4000		kHz
INPUT						
Input Offset Voltage	V_{IOS}			0.1	1.2	mV
Input Bias Current	I_B	V_{CM} = 0 V		6	25	µA
Input Offset Current	Ios	V_{CM} = 0 V		±0.002	±2.5	µA
Common-Mode Rejection	CMR	V_{CM} = ±8 V				
		G = 1000	80	112		dB
		G = 100	60	92		dB
		G = 10	40	74		dB
		G = 1, T_A = +25°C	26	54		dB
		G = 1, T_A = – 40°C to +85°C	20	54		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V				
		G = 1000	80	124		dB
		G = 100	60	118		dB
		G = 10	40	101		dB
		G = 1	26	82		dB
Input Voltage Range	IVR		±8			V
Input Resistance	R_{IN}	Differential, G = 1000		1		MΩ
		G = 1		30		MΩ
		Common Mode, G = 1000		5.3		MΩ
		G = 1		7.1		MΩ
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ; T_A = +25°C	±11.0	±12.3		V
Output Offset Voltage	V_{OOS}			–40	500	mV
Minimum Resistive Load Drive		T_A = +25°C		2		kΩ
		T_A = –40°C to +85°C		4.7		kΩ
Maximum Capacitive Load Drive				50		pF
Short Circuit Current Limit	I_{SC}	Output-to-Ground Short		±50		mA
Output Short Circuit Duration					10	sec
GAIN						
Gain Accuracy	$R_G = \frac{10\ k\Omega}{G-1}$	T_A = +25°C				
		R_G = 10 Ω, G = 1000		0.25	1	dB
		R_G = 101 Ω, G = 100		0.20	1	dB
		R_G = 1.1 kΩ, G = 10		0.20	1	dB
		R_G = ∞, G = 1		0.05	0.5	dB
Maximum Gain	G			70		dB
REFERENCE INPUT						
Input Resistance				10		kΩ
Voltage Range				±8		V
Gain to Output				1		V/V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±22	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±10.6	±14.0	mA

Specifications subject to change without notice.

Typical Performance Characteristics

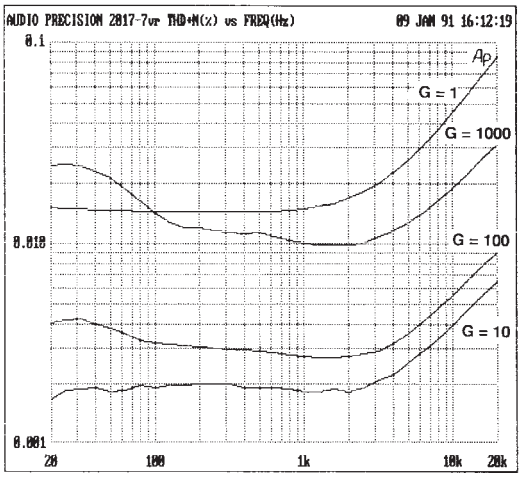


Figure 1. Typical THD+Noise at G = 1, 10, 100, 1000; V_O = 7 V rms, V_S = ±15 V, R_L = 5 kΩ; T_A = +25°C*

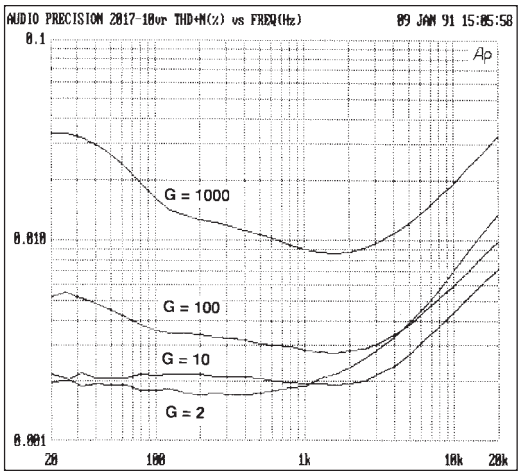


*Figure 2. Typical THD+ Noise * at G = 2, 10, 100, 1000; V_O = 10 V rms, V_S = ±18 V, R_L = 5 kΩ; T_A = +25°C*

*80 kHz low-pass filter used for Figures 1-2.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±22 V
Input Voltage . . . . . Supply Voltage
Output Short Circuit Duration . . . . . 10 sec
Storage Temperature Range (P, Z Packages) –65°C to +150°C
Junction Temperature (T_J) . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
Operating Temperature Range . . . . . –40°C to +85°C
Thermal Resistance*
8-Pin Hermetic DIP (Z): θ_{JA} = 134; θ_{JC} = 12 . . . . . °C/W
8-Pin Plastic DIP (P): θ_{JA} = 96; θ_{JC} = 37 . . . . . °C/W
16-Pin SOIC (S): θ_{JA} = 92; θ_{JC} = 27 . . . . . °C/W

*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ORDERING GUIDE

Model	Temperature Range*	Package Description	Package Option
SSM2017P	–40°C to +85°C	8-Pin Plastic DIP	N-8
SSM2017S	–40°C to +85°C	16-Lead SOL	R-16
SSM2017S-REEL	–40°C to +85°C	16-Lead SOL	R-16

*XIND = –40°C to +85°C.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2017 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

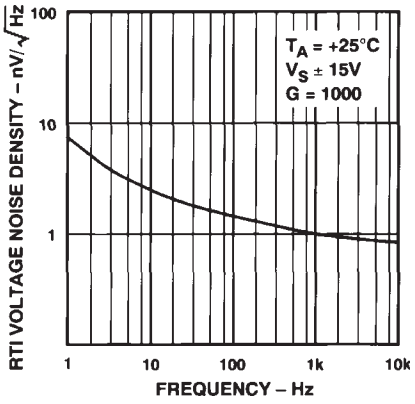


Figure 3. Voltage Noise Density vs. Frequency

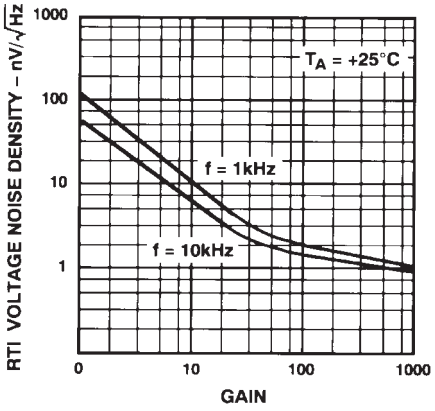


Figure 4. RTI Voltage Noise Density vs. Gain

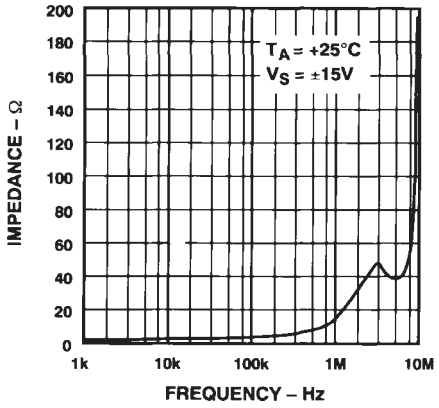


Figure 5. Output Impedance vs. Frequency

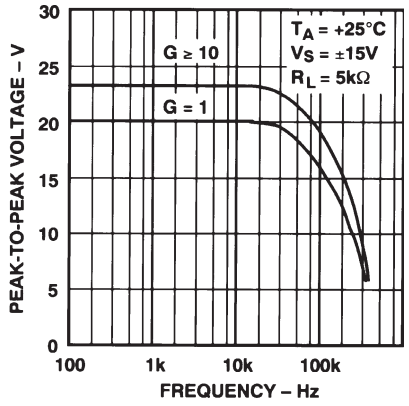


Figure 6. Maximum Output Swing vs. Frequency

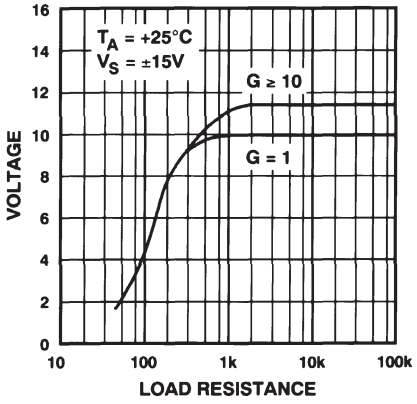


Figure 7. Maximum Output Voltage vs. Load Resistance

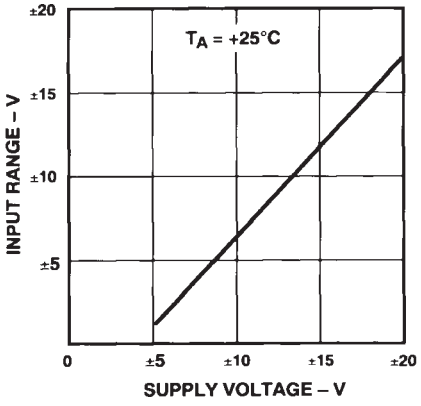


Figure 8. Input Voltage Range vs. Supply Voltage

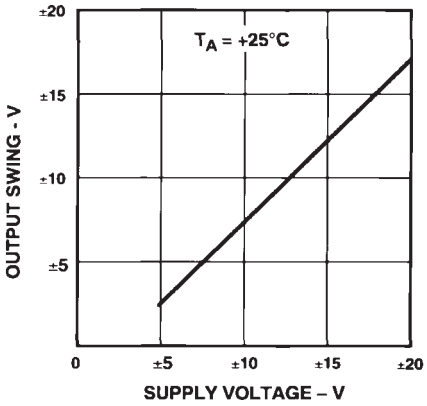


Figure 9. Output Voltage Range vs. Supply Voltage

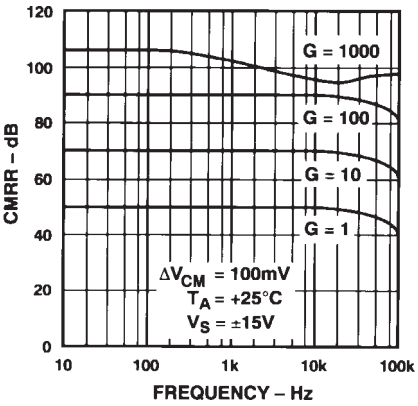


Figure 10. CMRR vs. Frequency

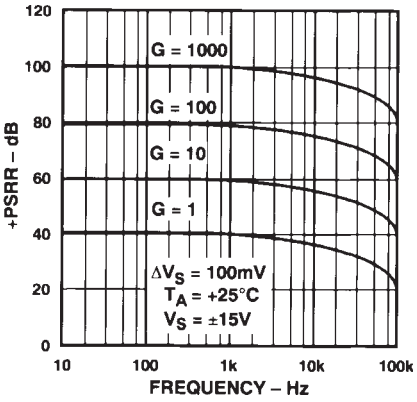


Figure 11. +PSRR vs. Frequency

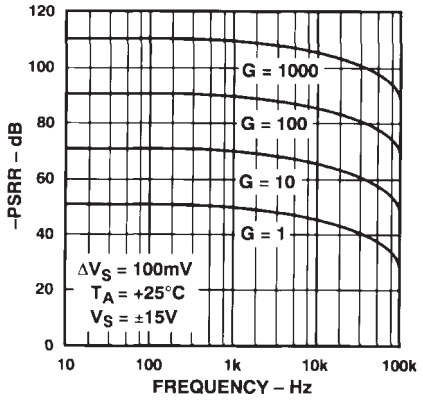


Figure 12. –PSRR vs. Frequency

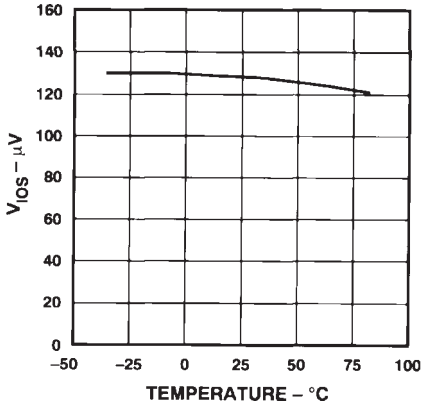


Figure 13. V_{IOS} vs. Temperature

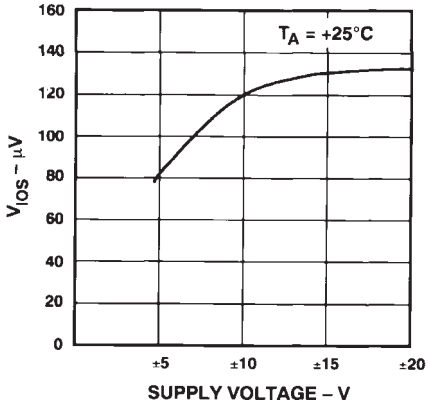


Figure 14. V_{IOS} vs. Supply Voltage

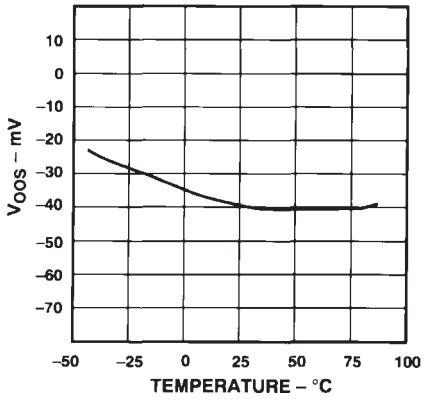


Figure 15. V_{OOS} vs. Temperature

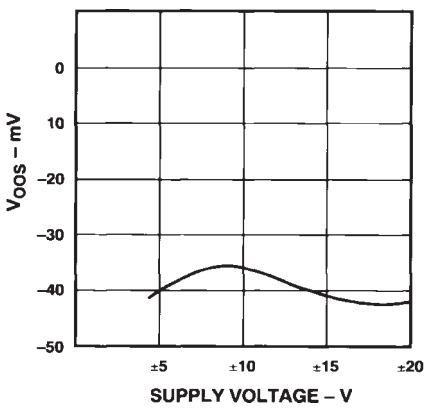


Figure 16. V_{OOS} vs. Supply Voltage

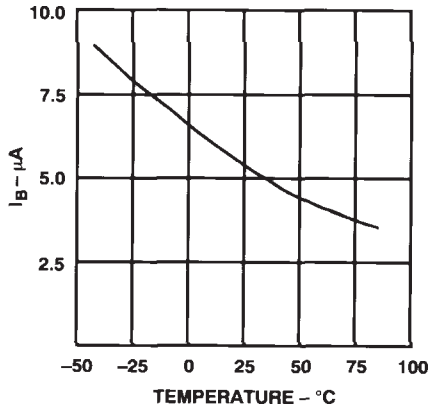


Figure 17. I_B vs. Temperature

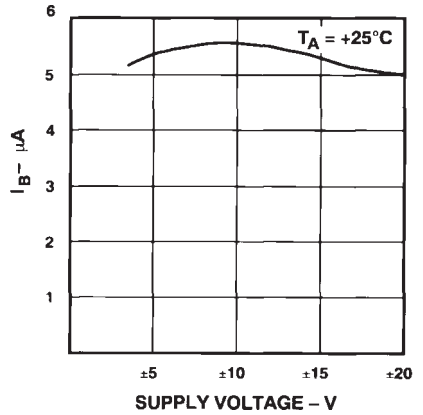


Figure 18. I_B vs. Supply Voltage

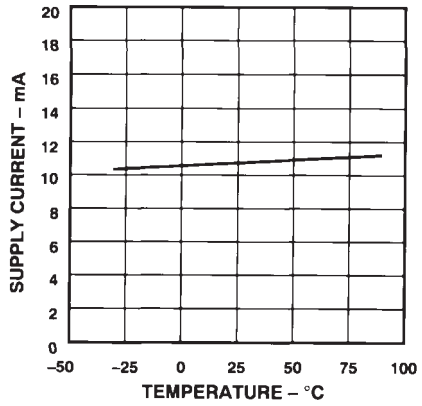


Figure 19. I_{SY} vs. Temperature

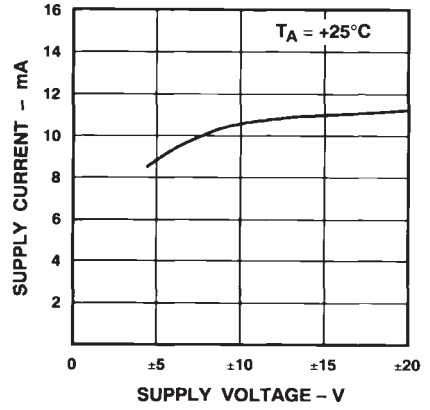
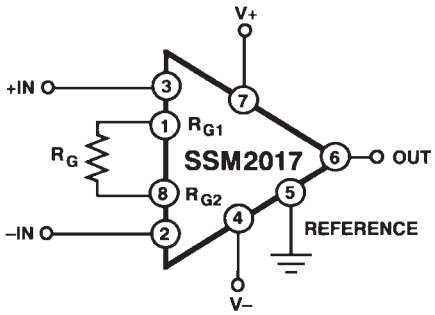


Figure 20. I_{SY} vs. Supply Voltage



$$G = \frac{V_{OUT}}{(+In) - (In)} = \left(\frac{10\,k\Omega}{R_G}\right) + 1$$

Basic Circuit Connections

GAIN

The SSM2017 only requires a single external resistor to set the voltage gain. The voltage gain, *G*, is:

$$G = \frac{10\,k\Omega}{R_G} + 1$$

and

$$R_G = \frac{10\,k\Omega}{G - 1}$$

For convenience, Table I lists various values of R_G for common gain levels.

Table I. Values of R_G for Various Gain Levels

A_V	dB	R_G
1	0	NC
3.2	10	4.7k
10	20	1.1k
31.3	30	330
100	40	100
314	50	32
1000	60	10

The voltage gain can range from 1 to 3500. A gain set resistor is not required for unity gain applications. Metal-film or wire-wound resistors are recommended for best results.

The total gain accuracy of the SSM2017 is determined by the tolerance of the external gain set resistor, R_G, combined with the gain equation accuracy of the SSM2017. Total gain drift combines the mismatch of the external gain set resistor drift with that of the internal resistors (20 ppm/°C typ).

Bandwidth of the SSM2017 is relatively independent of gain as shown in Figure 21. For a voltage gain of 1000, the SSM2017 has a small-signal bandwidth of 200 kHz. At unity gain, the bandwidth of the SSM2017 exceeds 4 MHz.

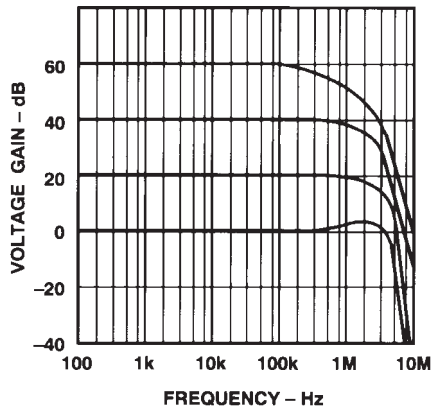


Figure 21. Bandwidth of the SSM2017 for Various Values of Gain

NOISE PERFORMANCE

The SSM2017 is a very low noise audio preamplifier exhibiting a typical voltage noise density of only 1 nV/√Hz at 1 kHz. The exceptionally low noise characteristics of the SSM2017 are in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the SSM2017 is obtained at the expense of current noise performance. At low preamplifier gains, the effect of the SSM2017's voltage and current noise is insignificant.

The total noise of an audio preamplifier channel can be calculate by:

$$E_n = \sqrt{e_n^2 + (i_n R_S)^2 + e_t^2}$$

where:

E_n = total input referred noise

e_n = amplifier voltage noise

i_n = amplifier current noise

R_S = source resistance

e_t = source resistance thermal noise.

For a microphone preamplifier, using a typical microphone impedance of 150 Ω the total input referred noise is:

e_n = 1 nV/√Hz @ 1 kHz, SSM2017 e_n

i_n = 2 pA/√Hz @ 1 kHz, SSM2017 i_n

R_S = 150 Ω, microphone source impedance

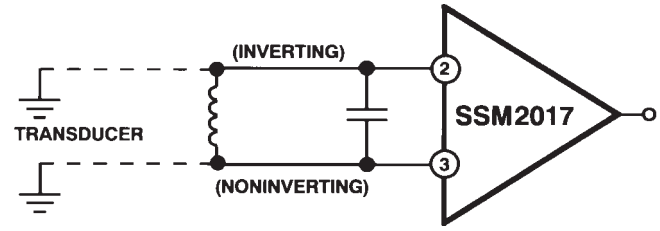
e_t = 1.6 nV/√Hz @ 1 kHz, microphone thermal noise

$$E_n = \sqrt{(1\ nV\sqrt{Hz})^2 + 2\ (pA/\sqrt{Hz} \times 150\ \Omega)^2 + (1.6\ nV/\sqrt{Hz})^2}$$
$$= 1.93\ nV/\sqrt{Hz}\ @\ 1\ kHz.$$

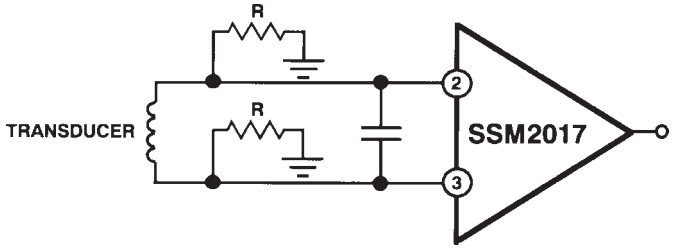
This total noise is extremely low and makes the SSM2017 virtually transparent to the user.

INPUTS

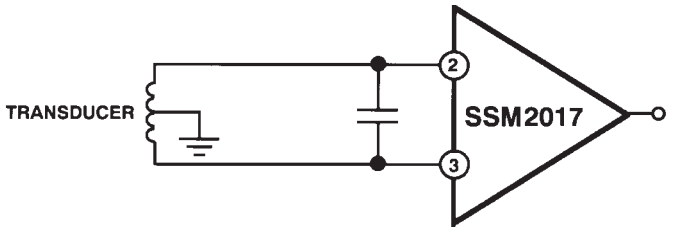
The SSM2017 has protection diodes across the base emitter junctions of the input transistors. These prevent accidental avalanche breakdown, which could seriously degrade noise performance. Additional clamp diodes are also provided to prevent the inputs from being forced too far beyond the supplies.



a. Single Ended



b. Pseudo Differential



c. True Differential

Figure 22. Three Ways of Interfacing Transducers for High Noise Immunity

Although the SSM2017's inputs are fully floating, care must be exercised to ensure that both inputs have a dc bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 22a, but an alternative way is to float the transducer and use two resistors to set the bias point as in Figure 22b. The value of these resistors can be up to 10 kΩ, but they should be kept as small as possible to limit common-mode pickup. Noise contribution by resistors themselves is negligible since it is attenuated by the transducer's impedance. Balanced transducers give the best noise immunity and interface directly as in Figure 22c.

REFERENCE TERMINAL

The output signal is specified with respect to the reference terminal, which is normally connected to analog ground. The reference may also be used for offset correction or level shifting. A reference source resistance will reduce the common-mode rejection by the ratio of 5 kΩ/R_{REF}. If the reference source resistance is 1 Ω, then the CMR will be reduced to 74 dB (5 kΩ/1 Ω = 74 dB).

COMMON-MODE REJECTION

Ideally, a microphone preamplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB.

PHANTOM POWERING

A typical phantom microphone powering circuit is shown in Figure 23. Z_1 through Z_4 provide transient overvoltage protection for the SSM2017 whenever microphones are plugged in or unplugged.

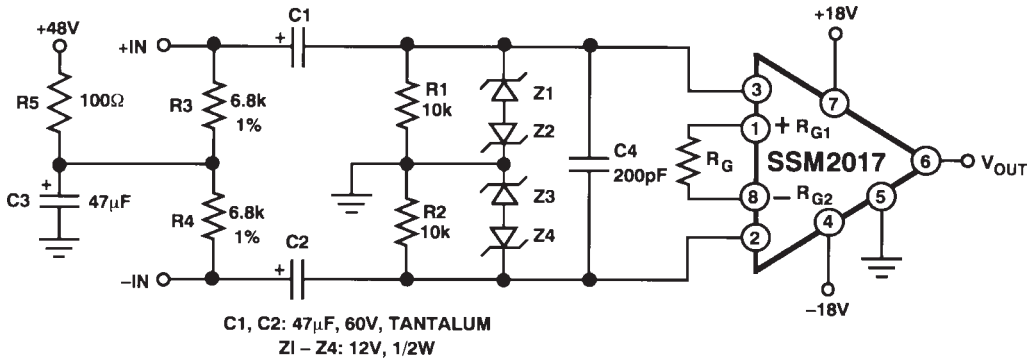


Figure 23. SSM2017 in Phantom Powered Microphone Circuit

BUS SUMMING AMPLIFIER

In addition to is use as a microphone preamplifier, the SSM2017 can be used as a very low noise summing amplifier. Such a circuit is particularly useful when many medium impedance outputs are summed together to produce a high effective noise gain.

The principle of the summing amplifier is to ground the SSM2017 inputs. Under these conditions, Pins 1 and 8 are ac virtual grounds sitting about 0.55 V below ground.

To remove the 0.55 V offset, the circuit of Figure 24 is recommended.

A_2 forms a "servo" amplifier feeding the SSM2017's inputs. This places Pins l and 8 at a true dc virtual ground. R4 in conjunction with C2 remove the voltage noise of A_2, and in fact just about any operational amplifier will work well here since it is removed from the signal path. If the dc offset at Pins l and 8 is not too critical, then the servo loop can be replaced by the diode biasing scheme of Figure 24. If ac coupling is used throughout, then Pins 2 and 3 may be directly grounded.

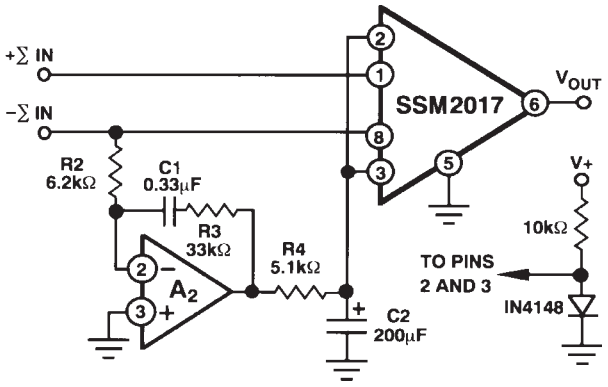


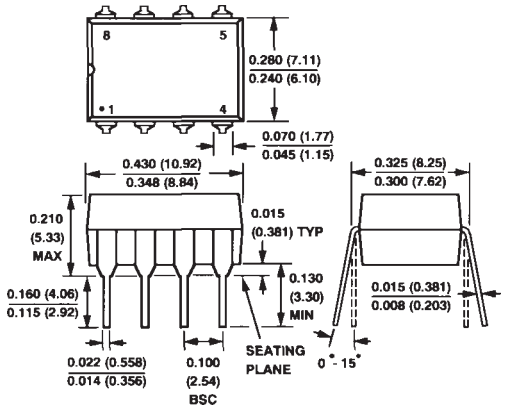
Figure 24. Bus Summing Amplifier

C1534–24–4/91

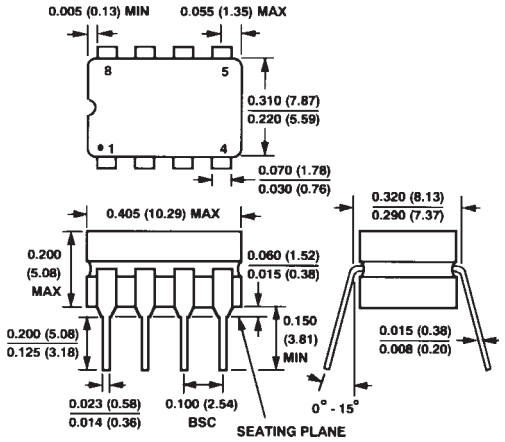
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

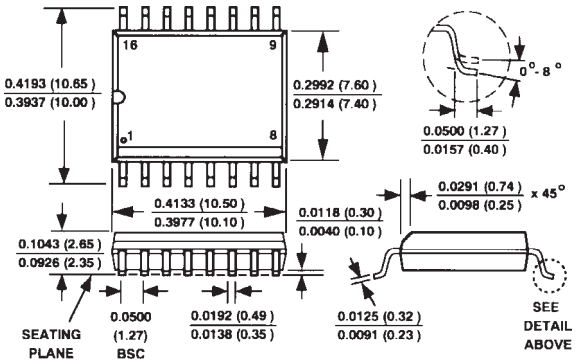
8-Pin Plastic DIP (P) Package



8-Pin Hermetic DIP (Z) Package



16-Pin SOIC (S) Package



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