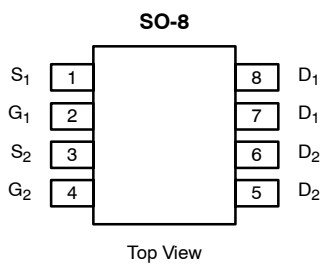


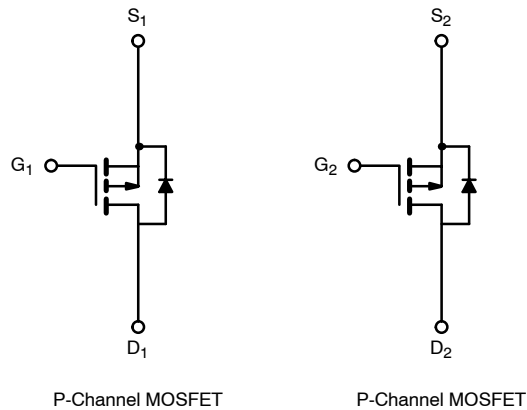


## Dual P-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-20	0.06 @ $V_{GS} = -4.5$ V	-4.7
	0.10 @ $V_{GS} = -2.5$ V	-3.7



Ordering Information: Si9933BDY—E3 (Lead Free)  
Si9933BDY-T1—E3 (Lead Free with Tape and Reel)



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	-20		V	
Gate-Source Voltage	$V_{GS}$	$\pm 12$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	-4.7	-3.6	A
		$T_A = 70^\circ\text{C}$	-3.8	-2.8	
Pulsed Drain Current	$I_{DM}$	-20			
continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-1.7	-0.9		
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2.0	1.1	W
		$T_A = 70^\circ\text{C}$	1.3	0.7	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec	$R_{thJA}$	55	62.5	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	33	40	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

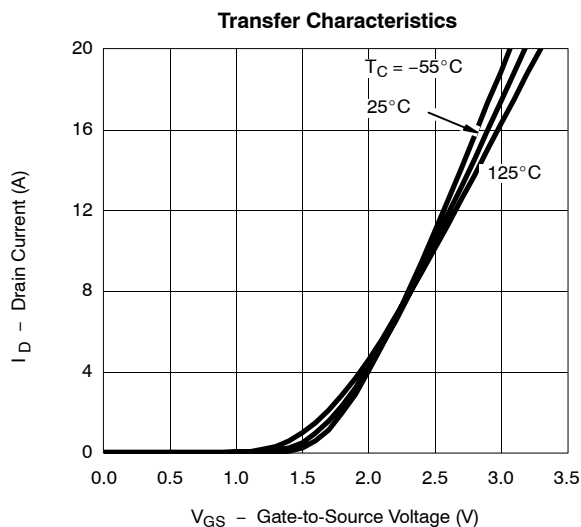
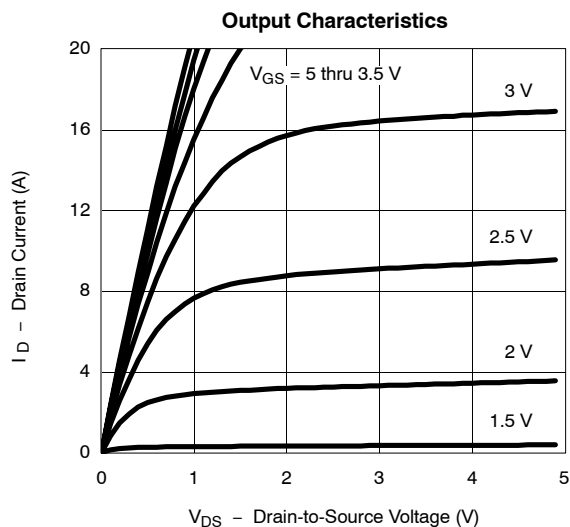
**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.6		-1.4	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			-5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	-20			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4.7 A		0.048	0.06	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1 A		0.08	0.10	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -4.7 A		11		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -1.7 A, V <sub>GS</sub> = 0 V		-0.75	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4.7 A		6	9	nC
Gate-Source Charge	Q <sub>gs</sub>			1.4		
Gate-Drain Charge	Q <sub>gd</sub>			1.9		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		9.5		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 6 Ω		22	35	ns
Rise Time	t <sub>r</sub>			35	55	
Turn-Off Delay Time	t <sub>d(off)</sub>			45	70	
Fall Time	t <sub>f</sub>			25	40	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -1.7 A, di/dt = 100 A/μs		25	50	

Notes

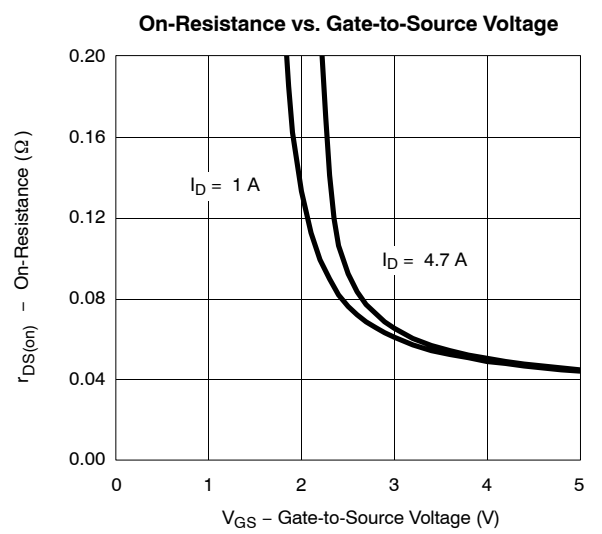
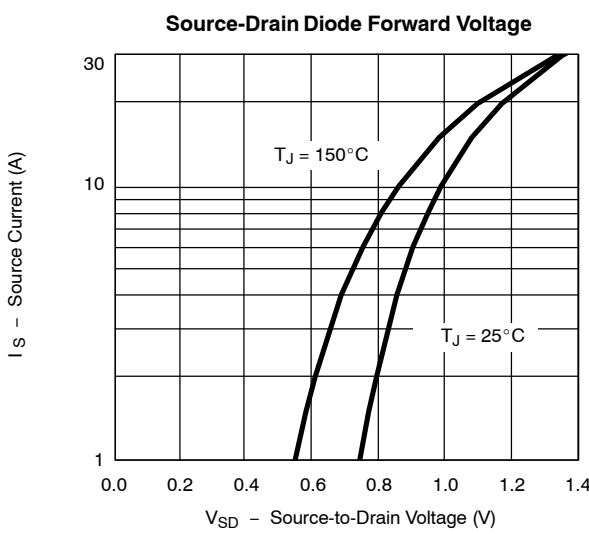
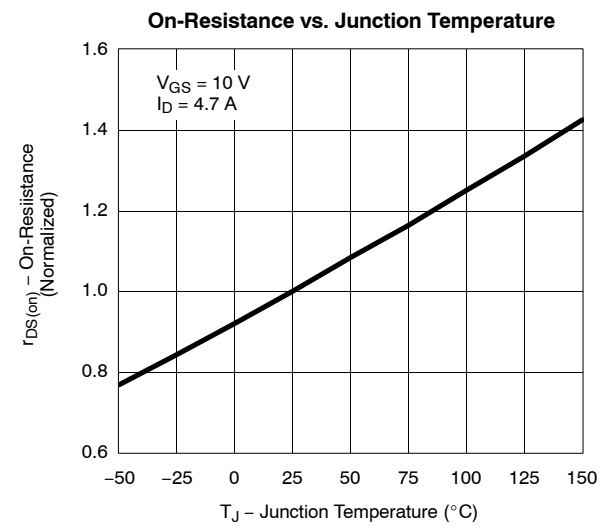
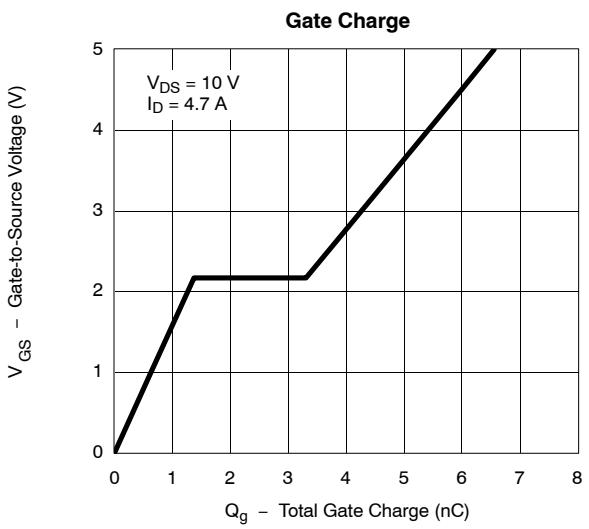
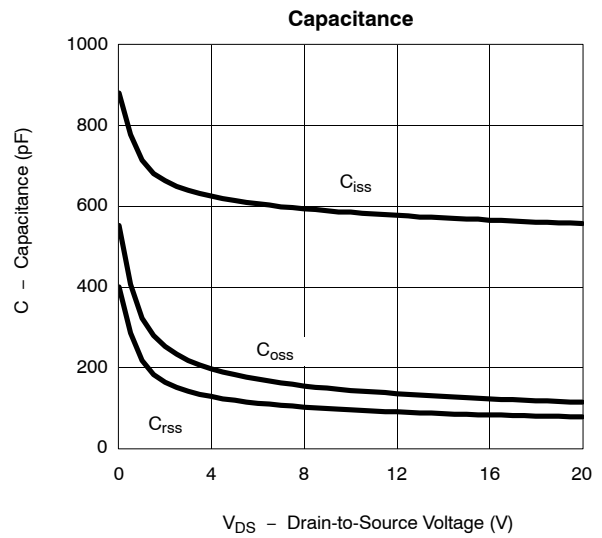
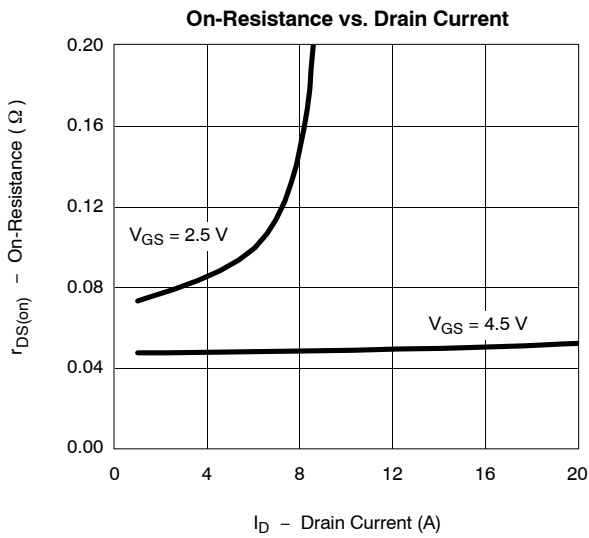
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

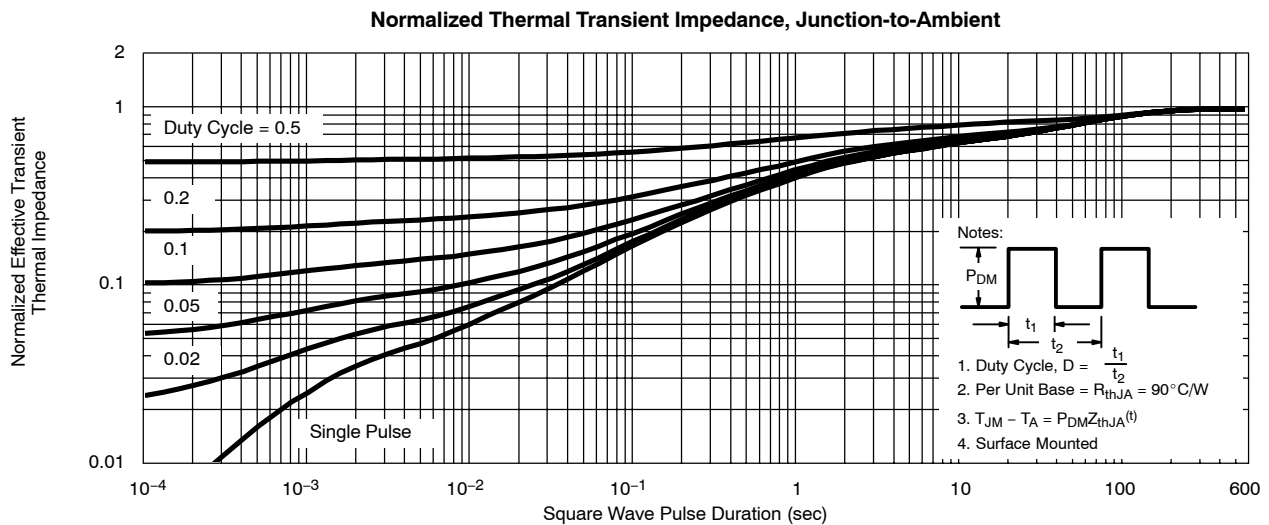
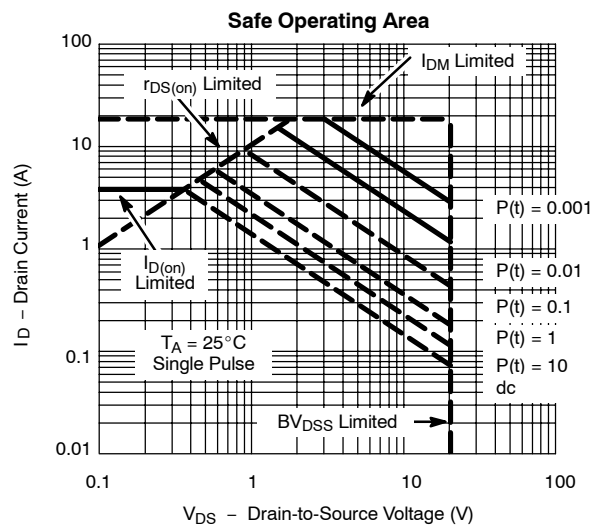
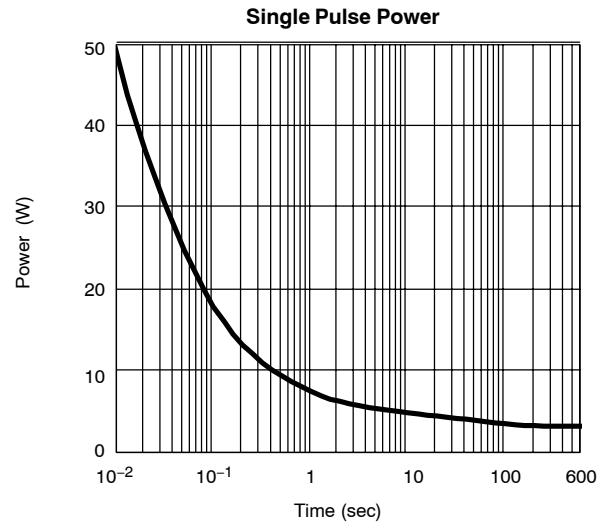
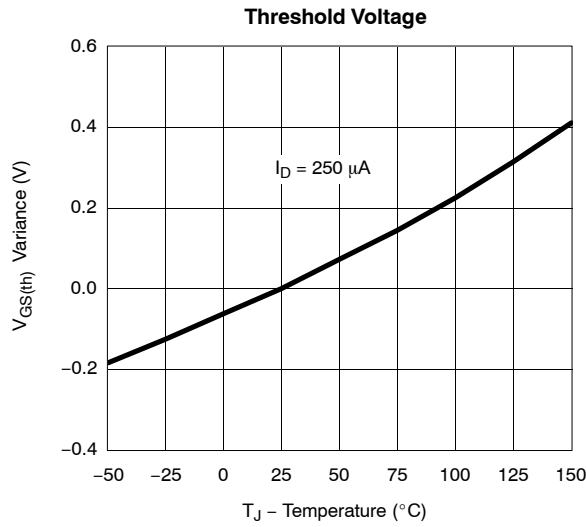




**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**





**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

