DATA SHEET

PCA84C646; PCA84C846
Microcontrollers for TV tuning control and OSD applications

Preliminary specification
Supersedes data of June 1994
File under Integrated Circuits, IC14

1995 Jun 15

Philips
Semiconductors

PHILIPS

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1 FEATURES

1.1 PCF84CXXXA kernel

- 8-bit CPU, ROM, RAM, I/O and derivative logic in one package
- Over 80 instructions
- All instructions of 1 or 2 cycles
- Quasi-bidirectional standard I/O port lines (P0, P1)
- Configuration of I/O lines individually selected by mask
- External interrupt $\overline{INT}$/T0
- 2 direct testable inputs T0, T1
- 8-bit timer/event counter
- Single level vectored interrupt: external ($\overline{INT}$), counter/timer, I^2C-bus and $\overline{VSYNC}$
- Configuration of optimal on-chip oscillator transconductance by mask
- On-chip oscillator clock frequency: 1 to 10 MHz
- Power-on-reset and low-voltage detector
- Low standby voltage and current in Idle and Stop modes
- Single power supply: 4.5 to 5.5 V
- Operating temperature: −20 to +70 °C.

1.2 VST and OSD derivative

- 6 kbytes (PCA84C646) or 8 kbytes (PCA84C846) system ROM, 192 bytes system RAM
- A multi-master I^2C-bus interface
- One 14-bit PWM output for VST
- Three AFC inputs with 4-bit DAC and comparator
- Four 6-bit PWM and four 7-bit PWM outputs (DACs for analog controls)
- Eight port lines with 10 mA LED drive (at ≤1.2 V) capability
- Programmable active level polarities of $\overline{VSYNC}$/$\overline{HSYNC}$
- Display RAM: 64 × 10-bit
- Display character fonts: 64 (62 customized + 2 special reserved codes)
- Display starting position: 64 different positions by software control, both vertical and horizontal
- Character size: 4 different character sizes, line-by-line basis, 1 dot = 1H/1V, 2H/2V, 3H/3V, 4H/4V. (H: OSD clock period, V: number of horizontal scan line height)
- Character matrix: 12 × 18 with no spacing between characters
- Foreground colours: 8, character-by-character basis
- Background colours: 8, word-by-word basis. Available when background is either in North-west shadowing, Box shadowing and Frame shadowing mode
- Background/shadowing modes: 4, No background, North-west shadowing, Box shadowing, Frame shadowing (raster blanking), frame basis
- On-chip oscillator for On Screen Display (OSD) function
- Character blinking rate: 1 : 1, 1 : 3, 3 : 1 (frequency: $\frac{1}{16}$, $\frac{1}{32}$, $\frac{1}{64}$ or $\frac{1}{128}$ of f_{VSYNC}, programmable), character basis
- Display format: flexible display format by using Carriage Return (CR) code
- Spacing between lines: 4 different choices, from 0, 4, 8 or 12 horizontal scan lines
- Auto display character RAM address post increment when writing data
- On-chip Power-on-reset
- $\overline{VSYNC}$ leading edge can generate interrupt (programmable enable/disable by software)
- 8-bit counter triggered by external pulse input.

2 GENERAL DESCRIPTION

The PCA84C646 and PCA84C846 are 8-bit microcontrollers with enhanced OSD and VST functions. The PCA84C646 and PCA84C846 are members of the PCA84C640 CMOS microcontroller family. They include the PCF84CXXXA processor core, 6 or 8 kbytes of ROM and 192 bytes of RAM.

I/O requirements are adequately catered for with 13 general purpose bidirectional I/O lines plus 16 function combined I/O lines. One 14-bit PWM analog control, 3 AFC inputs (4-bit DAC + comparator) for VST and four 6-bit and 7-bit PWM analog control outputs are provided.

In addition to all these features a master-slave I^2C-bus interface, 2 directly testable lines and an enhanced OSD facility for flexible screen format (maximum of 64 character types) are also provided.

The on-chip Phase-Locked Loop (PLL) oscillator for OSD operation considerably reduces the radiation generated by the RC or LC oscillator. An 8-bit timer is integrated on-chip with a 5-bit prescaler. Another 8-bit counter with Schmitt-trigger input is used for clock/timer function application.

Figure 1 shows the block diagram of the PCA84C646 and PCA84C846.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA84C646P	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
PCA84C846P			

4 BLOCK DIAGRAM

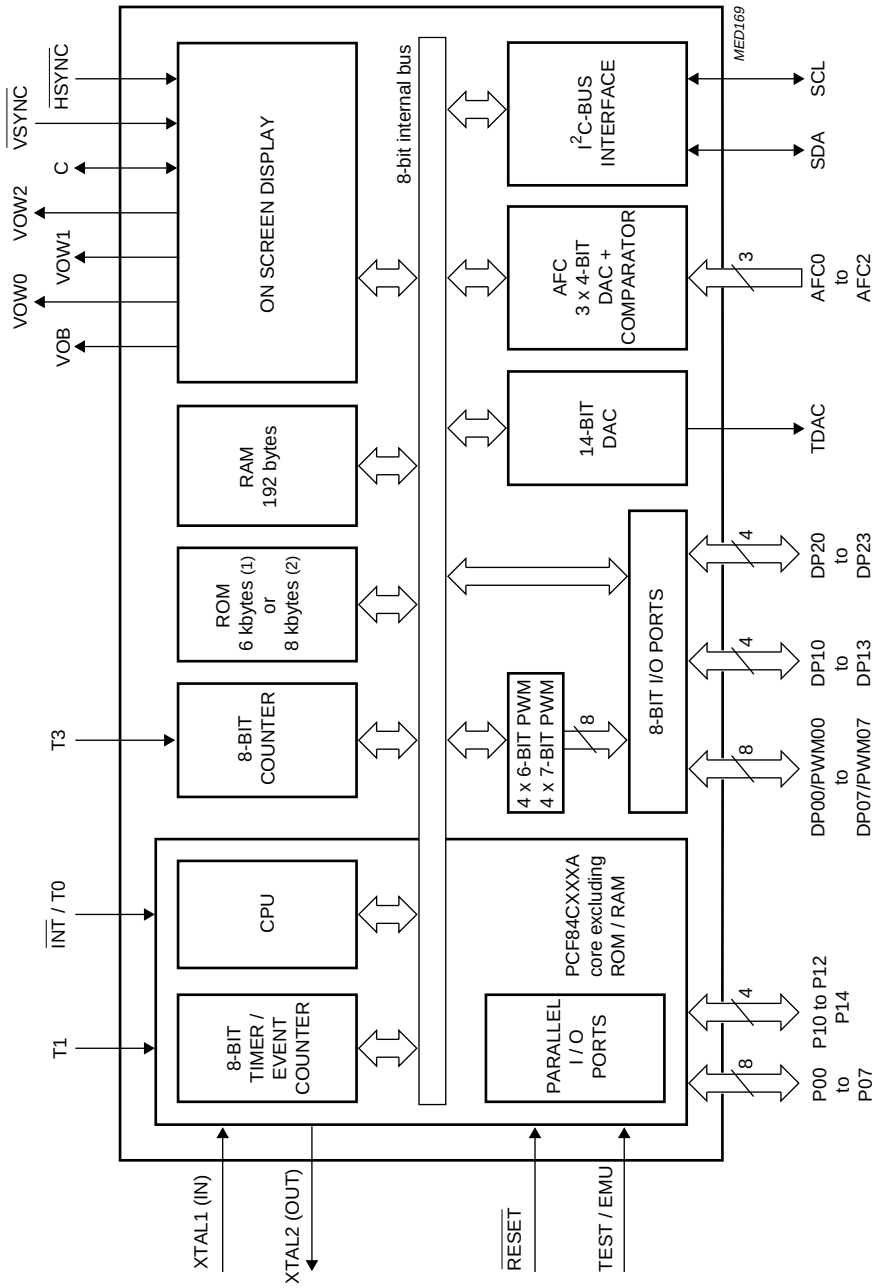


Fig.1 Block diagram

ROM size:
(1) 6 kbytes for PCA84C646.
(2) 8 kbytes for PCA84C846.

5 PINNING INFORMATION

5.1 Pinning

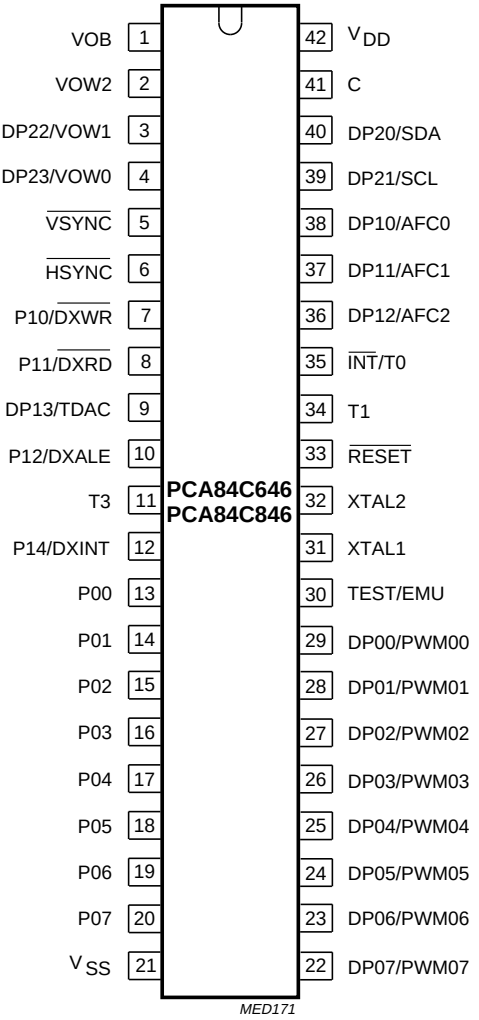


Fig.2 Pin configuration PCA84C646P and PCA84C846P (SDIP42; SOT270-1).

5.2 Pin description

Table 1 Pin description for PCA84C646P and PCA84C846P; SDIP42 (see Fig.2)

SYMBOL	PIN	DESCRIPTION
VOB	1	Video fast blanking output signal.
VOW2	2	Video character outputs or derivative port lines.
DP22/VOW1	3	
DP23/VOW0	4	
$\overline{\text{VSYNC}}$	5	Vertical synchronization signal input, active LOW.
$\overline{\text{HSYNC}}$	6	Horizontal synchronization signal input, active LOW.
P10/$\overline{\text{DXWR}}$	7	Port line 10 or emulation $\overline{\text{DXWR}}$ signal input.
P11/$\overline{\text{DXRD}}$	8	Port line 11 or emulation $\overline{\text{DXRD}}$ signal input.
DP13/TDAC	9	Derivative I/O port or 14-bit D/A PWM.
P12/DXALE	10	Port line 12 or emulation DXALE signal input.
T3	11	Secondary 8-bit counter input pin (Schmitt-trigger).
P14/DXINT	12	Port line 14 or emulation DXINT signal input.
P00 to P07	13 to 20	General I/O port lines (10 mA).
V_{SS}	21	Ground.
DP00/PWM00 to DP07/PWM07	29, 28, 27, 26, 25, 24, 23, 22	Derivative I/O port; 6-bit PWM (PWM04 to 07) or 7-bit PWM (PWM00 to 03).
TEST/EMU	30	Control input of testing and emulation mode, normally LOW.
XTAL1	31	Oscillator input terminal for system clock.
XTAL2	32	Oscillator output terminal for system clock.
$\overline{\text{RESET}}$	33	Initialize input, active LOW.
T1	34	Direct testable pin and event counter input.
$\overline{\text{INT}}$/T0	35	External interrupt/direct testable pin.
DP12/AFC2	36	Derivative I/O port or comparator input with 4-bit DAC.
DP11/AFC1	37	
DP10/AFC0	38	
DP21/SCL	39	Derivative port line or I^2C-bus clock line.
DP20/SDA	40	Derivative port line or I^2C-bus data line.
C	41	External capacitor input for on chip PLL OSD oscillator.
V_{DD}	42	Power supply.

6 RESET

The $\overline{\text{RESET}}$ pin is used as an active LOW input to initialize the microcontroller to a defined state.

A Power-on-reset can be generated by using the RC-circuit as shown in Fig.3.

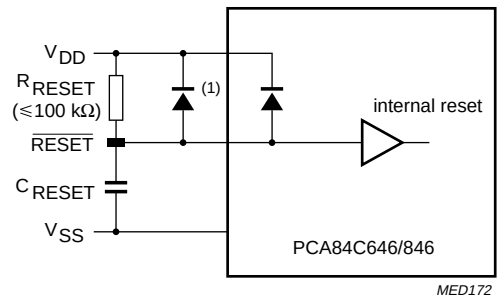
An active reset can be generated by driving the $\overline{\text{RESET}}$ pin from an external logic device. Such an active reset pulse should not fall off before V_{DD} has reached its f_{xtal}-dependent minimum operating voltage.

6.1 Reset trip level

The $\overline{\text{RESET}}$ trip-voltage level is masked to 1.3 V in the PCA84C646 and PCA84C846.

6.2 Reset status

- Derivative Registers status; for details see Table 40
- Program Counter: 00H
- Memory Bank: 00H
- Register Bank: 00H
- Stack Pointer: 00H
- All interrupts disabled
- Timer/event counter 1 stopped and cleared
- Timer prescaler modulo-32 (PS = 0)
- Timer flag cleared
- Serial I/O interface disabled (ESO = 0) and in slave receiver mode
- Idle and Stop mode cleared.



(1) To avoid overload of the internal diode, an external diode should be added in parallel if $C_{RESET} > 0.2$ µF.

Fig.3 External components for $\overline{\text{RESET}}$ pin.

7 ANALOG CONTROL

7.1 6 and 7-bit PWM outputs (PWM00 to PWM07)

The PCA84C646/PCA84C846 has eight PWM outputs for analog controls of e.g. volume, balance, brightness and saturation. These PWM outputs generate pulse patterns with a repetition rate of $^1/_{64} \times f_{PWM}$ or $^1/_{128} \times f_{PWM}$. The analog value is determined by the ratio of the HIGH-time and the repetition time. A DC voltage proportional to the PWM control setting is obtained by means of an external integration network (low-pass filter).

The eight PWM outputs are specified as follows:

- PWM00 to PWM03 outputs with 7-bit resolution
- PWM04 to PWM07 outputs with 6-bit resolution.

Figure 4 shows the block diagram of the 6-bit or 7-bit PWM DAC. The polarity of the PWM0n output is selected as shown in Table 2 by the polarity control bit P6LVL/P7LVL (Derivative Register 23; see Table 25).

The PWM0n output shares the pin with a DP0n I/O line under control of a PWMnE enable bit; for selection see Table 3.

Figure 5 shows the 6 and 7-bit PWM0n output patterns (non-inverted; P6LVL/P7LVL = 0).

The HIGH-time of a PWM0n output is

$t_{HIGH} = [PWMnDL] \times t_0$

where:

[PWMnDL] = the contents of PWMn data latch (n = 0 to 7; Derivative Register 10 to 17; see Table 40)

$t_0 = 1/f_{PWM}$; $f_{PWM} = {}^1/_3 \times f_{xtal}$.

Table 2 Polarity selection for the PWM0n output

P6LVL/P7LVL	POLARITY
1	inverted
0	not inverted

Table 3 Selection of pin function: DP0n/PWM0n (note 1)

PWMnE	FUNCTION
1	PWM0n output
0	DP0n I/O

Note

1. n = 0 to 7.

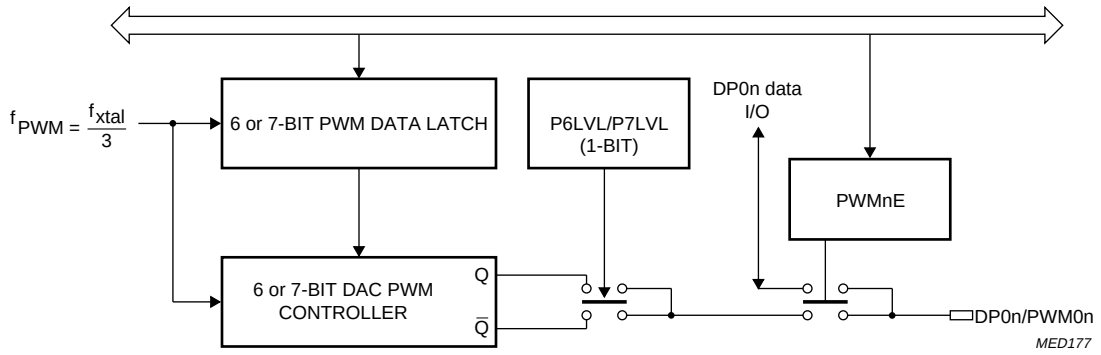


Fig.4 Block diagram of 6-bit or7-bit PWM DAC.

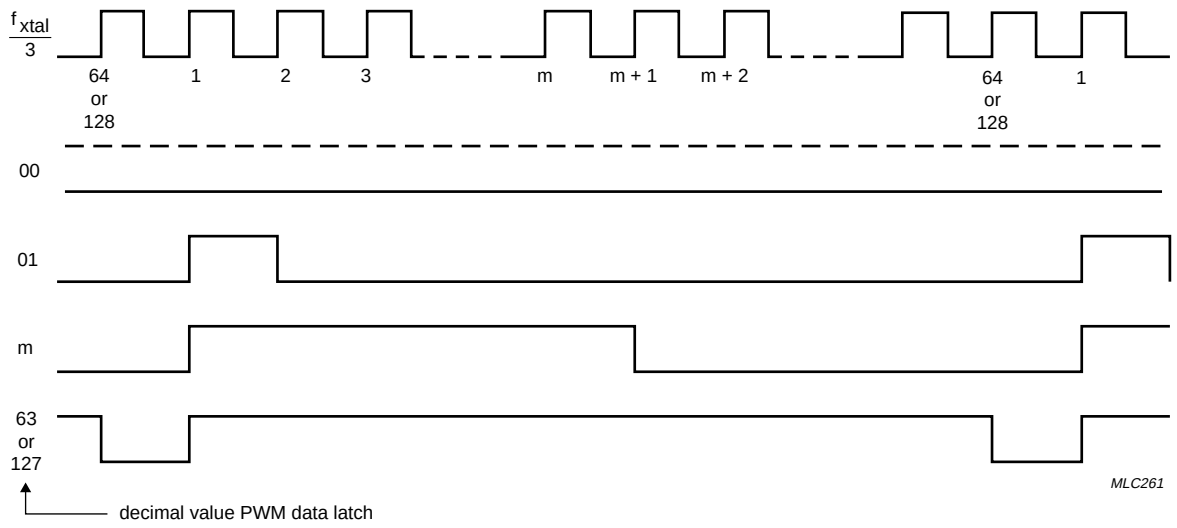


Fig.5 Example PWM0n output patterns (P6LVL/P7LVL = 0).

7.2 VST control 14-bit PWM DAC

The PCA84C646 and PCA84C846 have a PWM DAC output (TDAC) with a resolution of 16384 levels for Voltage Synthesized Tuning (VST).

Figure 6 shows the block diagram of the 14-bit PWM DAC which consists of:

- Two 7-bit DAC interface latches (see Table 40):
  - VSTH: Derivative Register 18; address 18H.
  - VSTL: Derivative Register 19; address 19H.
- One 14-bit DAC data latch: VSTREG, which contents defines the HIGH-time.
- 14-bit counter.
- Pulse control.

The contents of the interface latches VSTH and VSTL are latched into VSTREG. The upper seven bits of VSTREG are used for coarse adjustment, while the lower seven bits are used for fine adjustment.

The contents of the interface latches VSTH and VSTL are latched into VSTREG at the beginning of the first t_{sub} after VSTL is written (see Fig.7). After VSTH and VSTL are latched into VSTREG, it takes one t_{sub} to generate the appropriate pulse pattern.

Therefore, to ensure correct digital-to-analog conversion, two t_{sub} periods should be allowed before beginning the next sequence (changing the contents of VSTH and VSTL).

To ensure that the correct data is latched into VSTREG, VSTH must contain the correct value before VSTL is written; see the note in Fig.7.

The repetition times of the pulse controllers are:

- Coarse, upper seven bits (VSTH):
  $t_{sub} = 128 \times 3/f_{xtal}$
- Fine, lower seven bits (VSTL):
  $t_r = 128 \times t_{sub} = 49152/f_{xtal}$

Output TDAC shares the same pin as DP13; bit TDACE (Derivative Register 22; see Table 22) selects the function of pin DP13/TDAC.

Table 4 Selection of pin function DP13/TDAC

TDACE	FUNCTION
1	TDAC; 14-bit PWM output
0	DP13

7.2.1 COARSE ADJUSTMENT

An active HIGH pulse is generated in every subperiod; the pulse width being determined by the contents of VSTH. The coarse output (OUT1) is LOW at the start of each subperiod and will remain LOW during

$$t_s \leq \frac{(VSTH + 1) \times 3}{f_{xtal}}$$

Where t_s is the time within t_{subn}.

The output will then go HIGH and remain HIGH until the start of the next subperiod. The coarse pulse width may be calculated as: Pulse duration $= (127 - VSTH) \times \frac{3}{f_{xtal}}$.

7.2.2 FINE ADJUSTMENT

Fine adjustment is achieved by generating an additional pulse in specific subperiods. The pulse is added at the start of the selected subperiod and has a pulse width of $3/f_{xtal}$. The contents of VSTL determine in which subperiods a fine pulse will be added. It is the logic 0 state of the value held in VSTL that actually selects the subperiods. When more than one bit is a logic 0 then the subperiods selected will be a combination of those subperiods specified in Table 5. For example, if VSTL = 111 1010 then this is a combination of:

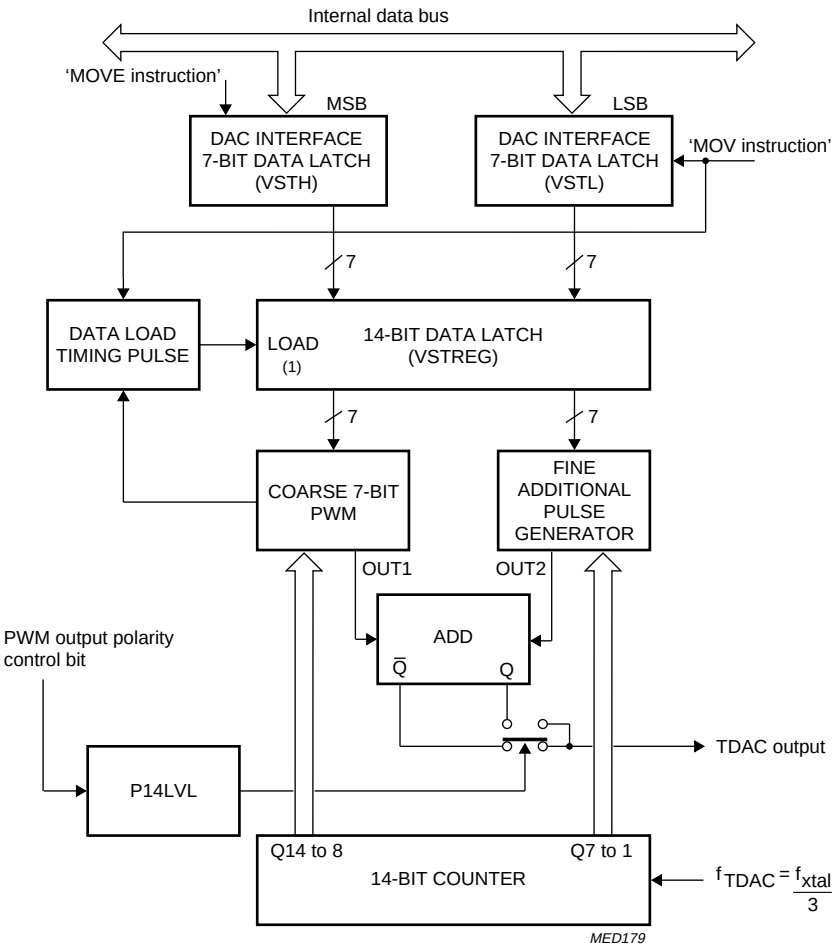
- VSTL = 111 1110: subperiod 64 and
- VSTL = 111 1011: subperiods 16, 48, 80 and 112.

Pulses will be added in subperiods 16, 48, 64, 80 and 112. This example is illustrated in Fig.9.

When VSTL holds 111 1111 fine adjustment is inhibited and the TDAC output is determined only by the contents of VSTH.

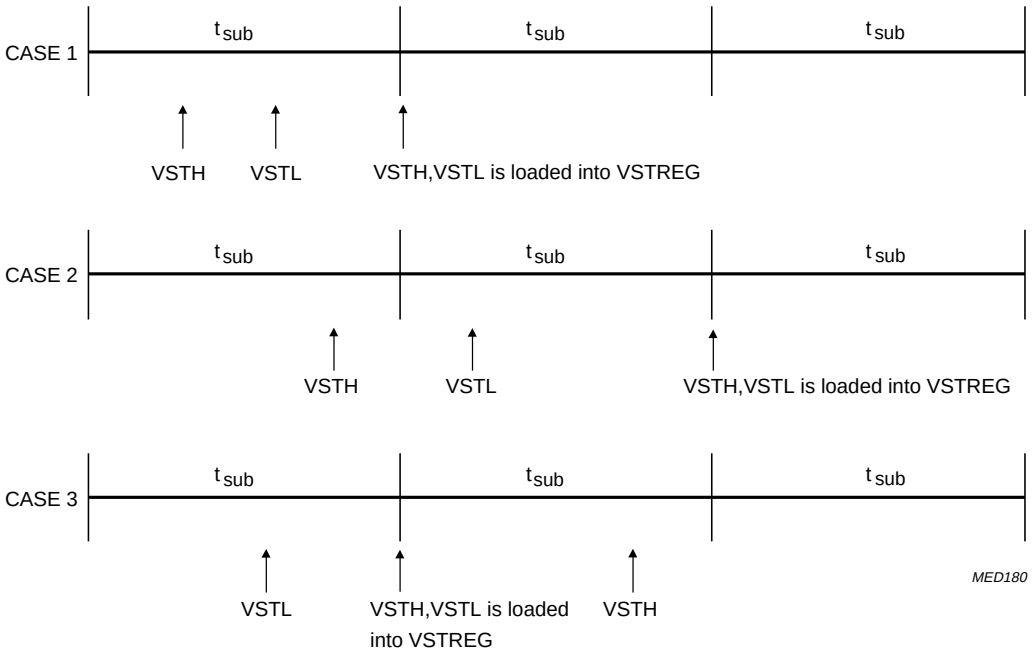
Table 5 Additional pulse distribution

VSTL	ADDITIONAL PULSE IN SUBPERIOD
111 1110	64
111 1101	32 and 96
111 1011	16, 48, 80 and 112
111 0111	8, 24, 40, 56, 72, 88, 104 and 120
110 1111	4, 12, 20, 28, 36, 44, 52...116 and 124
101 1111	2, 6, 10, 14, 18, 22, 26, 30...122 and 126
011 1111	1, 3, 5, 7, 9, 11, 13, 15, 17...125 and 127



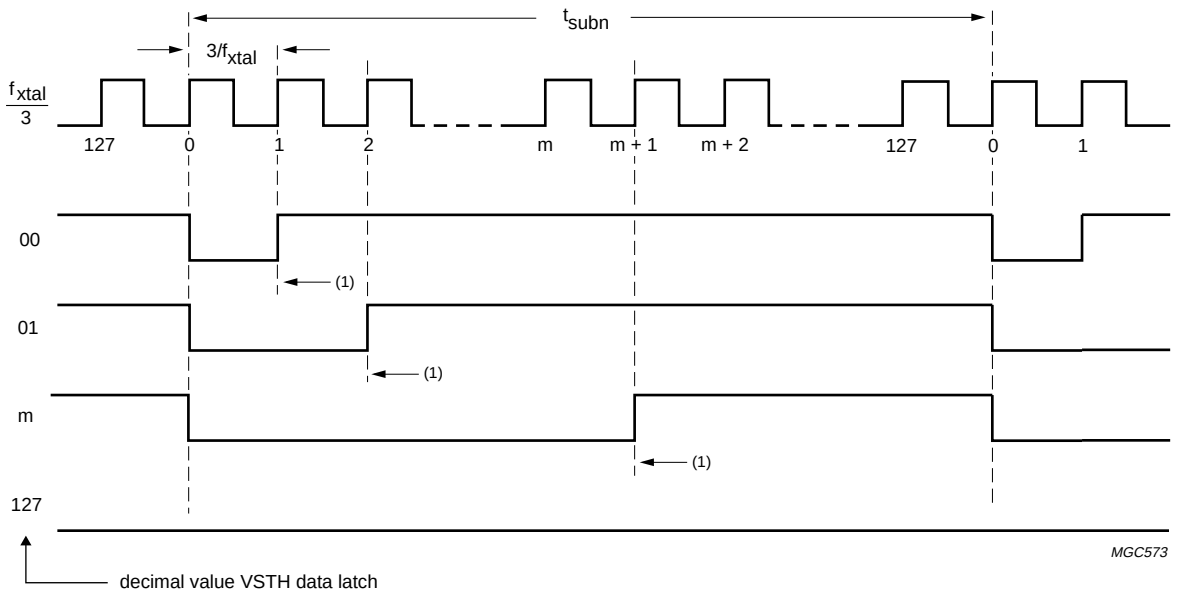
(1) See Fig.7 for timing.

Fig.6 Block diagram of the 14-bit PWM DAC.



In CASE 1 and CASE 2, a new value for VSTH, VSTL is latched into VSTREG.
In CASE 3, VSTL, together with an old value of VSTH are latched into VSTREG.

Fig.7 Latching VSTH, VSTL into VSTREG.



(1) $t_s = \frac{(VSTH + 1) \times 3}{f_{xtal}}$

Fig.8 TDAC output (not inverted) with coarse adjustment only; VSTL = 1111111; P14LVL = 0.

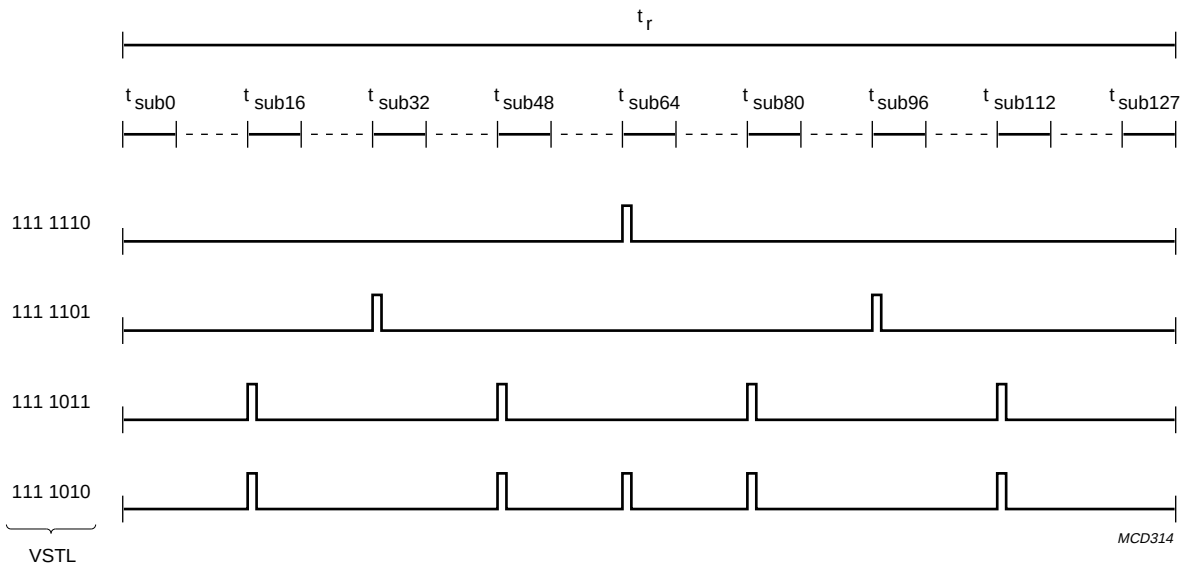
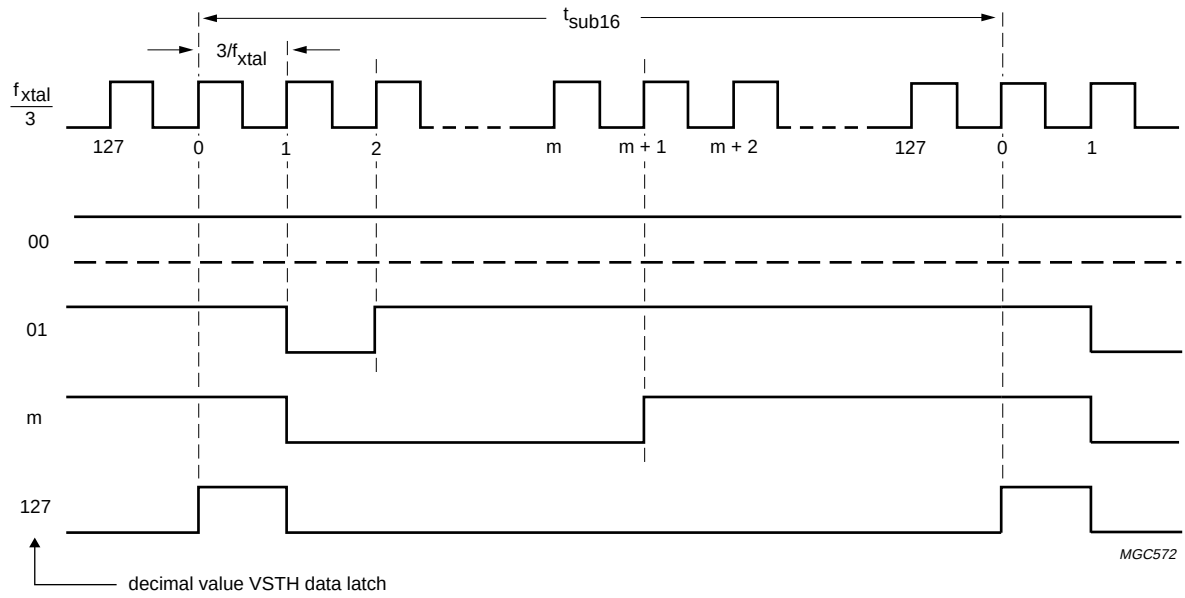


Fig.9 Fine adjustment output (OUT2).



VSTL = 111 1010; Additional pulses in subperiods 16, 48, 64, 80 and 112.

Fig.10 Example of TDAC (not inverted) output pulses for several values of VSTH (t_{sub16}).

8 AFC INPUT

The AFC input is intended to measure the level of the Automatic Frequency Control (AFC) signal. This is done by comparing the AFC signal with the output of a 4-bit digital-to-analog converter as shown in Fig.11. The DAC analog switches select one of the 16 resistor taps that are connected between V_{DD} and V_{SS} (controlled by bits AFCV3, AFCV2, AFCV1, AFCV0; Derivative Register 20). The AFCC signal (bit 0 in Derivative Register 20) then can be tested to check whether the AFC input is higher or lower than the DAC level.

The AFC inputs AFC0, AFC1 and AFC2 share the same pins as Derivative Port lines DP10, DP11 and DP12. The pin functions are selected by bits AFCE0, AFCE1, AFCE2 (AFC enable/disable bits; Derivative Register 22); for selection see Table 6.

AFCH1 and AFCH0 (Derivative Register 20) select one out of three AFC inputs to the comparator; for a correct comparison, enable the corresponding AFC input (AFCi) as shown in Table 7.

The conversion time of the AFC is greater than 6 μs but less than 9 μs. It is recommended to add a NOP instruction between the instruction which changes V_{ref} or channel selection and the instruction which reads the AFCC bit (compare bit).

If the compare bit:

- AFCC = 0, then the AFC voltage < V_{ref}.
- AFCC = 1, then the AFC voltage > V_{ref}.

Table 6 Selection of pin function DP1i/AFCi (i = 0, 1, 2)

BIT	VALUE	PIN FUNCTION	COMPARATOR
AFCE2	1	DP12	disabled
	0	AFC2	enabled
AFCE1	1	DP11	disabled
	0	AFC1	enabled
AFCE0	1	DP10	disabled
	0	AFC0	enabled

Table 7 AFC input selection

AFCH1	AFCH0	SELECT
0	0	AFC Channel 0; AFC0
0	1	AFC Channel 1; AFC1
1	0	AFC Channel 2; AFC2
1	1	reserved

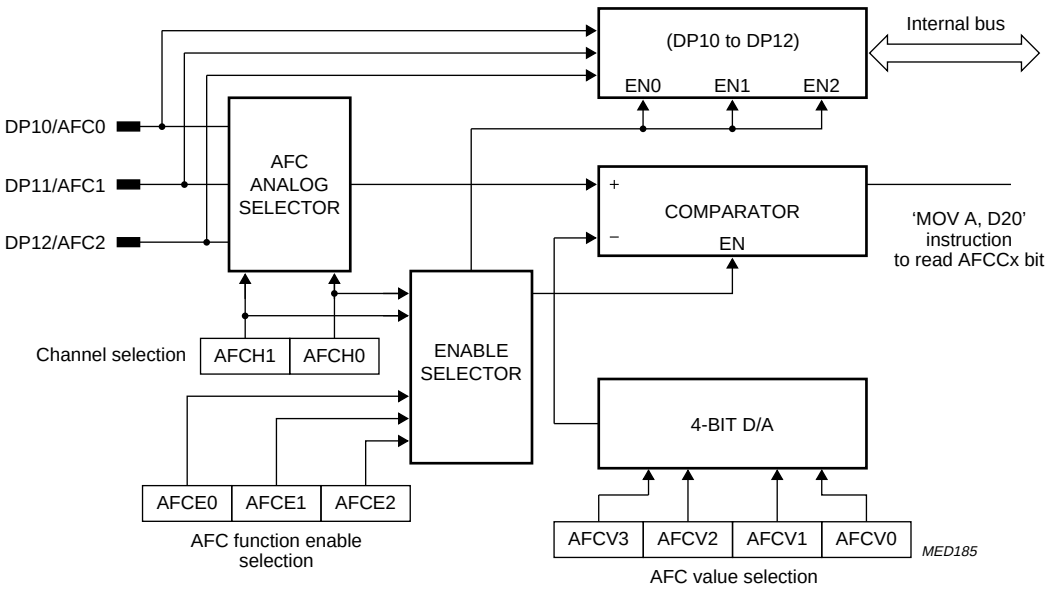


Fig.11 AFC circuit.

Table 8 V_{ref} as a function of AFCV3 to AFCV0

AFCV3	AFCV2	AFCV1	AFCV0	V_{ref}	V_{ref} (V_{DD} = 5.0 V)
0	0	0	0	$V_{DD} \times 1/16$	0.31 V
0	0	0	1	$V_{DD} \times 2/16$	0.62 V
0	0	1	0	$V_{DD} \times 3/16$	0.93 V
0	0	1	1	$V_{DD} \times 4/16$	1.25 V
0	1	0	0	$V_{DD} \times 5/16$	1.56 V
0	1	0	1	$V_{DD} \times 6/16$	1.87 V
0	1	1	0	$V_{DD} \times 7/16$	2.18 V
0	1	1	1	$V_{DD} \times 8/16$	2.50 V
1	0	0	0	$V_{DD} \times 9/16$	2.81 V
1	0	0	1	$V_{DD} \times 10/16$	3.12 V
1	0	1	0	$V_{DD} \times 11/16$	3.43 V
1	0	1	1	$V_{DD} \times 12/16$	3.75 V
1	1	0	0	$V_{DD} \times 13/16$	4.06 V
1	1	0	1	$V_{DD} \times 14/16$	4.37 V
1	1	1	0	$V_{DD} \times 15/16$	4.68 V
1	1	1	1	V_{DD}	5.00 V

9 OSD (ON SCREEN DISPLAY) FUNCTION

9.1 Features

- Display RAM: 64 × 10 bit.
- Display character fonts: 64 (in which 62 customized + 2 special reserved codes).
- Display starting position (of the first character): 64 different positions by software control, both vertical and horizontal.
- Character size: 4 different character sizes, line-by-line basis, 1 dot = 1H/1V, 2H/2V, 3H/3V, 4H/4V.
- Character matrix: 12 × 18 with no spacing between characters.
- Foreground colours: 8, combination of Red, Green, Blue; character-by-character basis.
- Background/shadowing modes: 4, No background, Box shadowing, North-west shadowing, Frame shadowing (raster blanking), frame basis.
- Background colours: 8, combination of Red, Green, Blue; word-by-word basis. Available when background mode is either in Box shadowing or North-west shadowing and Frame shadowing mode.
- On-chip OSD oscillator.
- Character blinking rate: 1 : 1, 1 : 3, 3 : 1 (frequency: $^1/_{16}$, $^1/_{32}$, $^1/_{64}$ or $^1/_{128}$ of f_{VSYNC}, programmable, e.g. NTSC: $^{60}/_{16}$ Hz, PAL: $^{50}/_{64}$ Hz etc.); character basis.
- Display format: flexible display format by using Carriage Return (CR) code, maximum number of characters per line is flexible and depending on the OSD clock.
- Spacing between lines: 4 different choices from 0, 4, 8 or 12 horizontal scan lines.
- Display character RAM auto-address-post-increment when writing data.
- Programmable $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ active input polarity.
- Programmable G (VOW1), B (VOW2), R (VOW0) and FB (VOB) output polarity.

9.2 Horizontal display position control

The horizontal position counter is increased every OSD clock (f_{OSD}) cycle after the programmed level of $\overline{\text{HSYNC}}$ occurs at the $\overline{\text{HSYNC}}$ pin and is reset when the opposite polarity of the $\overline{\text{HSYNC}}$ is reached. Horizontal start position is controlled by Derivative Register 36 (HPOS; see Table 36). The starting position is calculated as:

HP = [4 × (H5 to H0) + 5] × (OSD clock cycle)

where (H5 to H0) = decimal value of register HPOS; (H5 to H0) ≥ 10.

9.3 Vertical display position control

The vertical position counter is increased every $\overline{\text{HSYNC}}$ cycle and is reset by the $\overline{\text{VSYNC}}$ signal. Vertical start position is controlled by Derivative Register 35 (VPOS; see Table 34). The vertical starting position is calculated as:

VP = [4 × (V5 to V0)] × (horizontal scan lines)

where (V5 to V0) = decimal value of register VPOS; (V5 to V0) ≥ 0.

9.4 Clock generator

Figure 12 illustrates the block diagram of the on-chip OSD clock generator which consists of a Phased-Lock Loop (PLL) circuit. The Voltage Controlled Oscillator (VCO) outputs a clock (f_{VCO}) with a frequency range of 8 to 20 MHz (see Fig.12). The input signal $f_1 = \overline{\text{HSYNC}}$.

The programmable active level detector:

- Passes signal f_1, when $\overline{\text{HSYNC}}$ is active HIGH, or
- Inverts signal f_1, when $\overline{\text{HSYNC}}$ is active LOW.

The output signal f_2 is always active HIGH. The VCO is synchronized with the HIGH-to-LOW edge of the f_2 signal.

The value programmed in the 7-bit PLL Programmable Counter control register (PLLCN; Derivative Register 25; see Table 40) determines:

$f_{VCO} = f_1 \times 16 \times$ (decimal value of 7-bit counter);

where 16 < (decimal value of 7-bit counter) < 48.

The value 16 is the 4-bit prescaler which increases or decreases the output of the VCO in steps of ($16 \times f_1$). Given an example of f_1 = 15.750 kHz, the f_{VCO} is then increased or decreased in steps of 16×15.750 kHz = 252 kHz = 0.25 MHz.

The f_{VCO} is fed into a buffer to generate the OSD dot clock frequency signal (f_{OSD}); 4 MHz ≤ f_{OSD} ≤ 12 MHz. Decreasing f_{OSD} gives broader characters. Recommended: 4 MHz ≤ f_{OSD} typical ≤ 12 MHz.

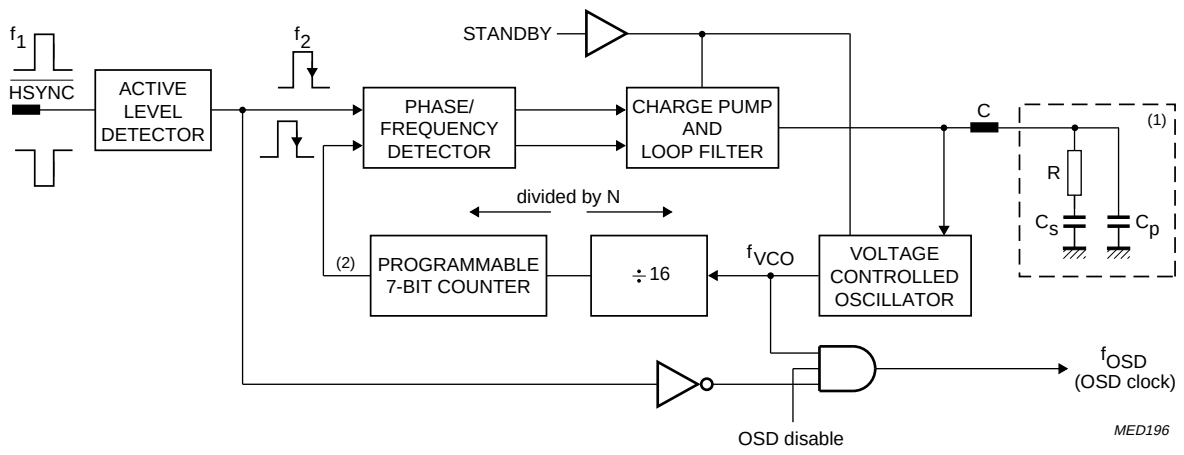
The OSD clock is enabled/disabled by the state of the EN bit (Derivative Register 34; see also Section 12.4). When the OSD clock is disabled (f_{OSD} = LOW) the oscillator remains active, therefore the transient time from the OSD clock start-up to locking into the external $\overline{\text{HSYNC}}$ signal is reduced.

As the on-chip oscillator is always active after Power-on, when the OSD clock is enabled no large currents flow (as for RC or LC oscillators) and therefore radiated noise is dramatically reduced.

9.4.1 MOUNTING PRECAUTIONS

To achieve good OSD performance, take the following precautions for the microcontroller mounting:

- Apply the recommended R, C_s and C_p (PLL loop filter) values as shown in Fig.12 and place them as close as possible to pin C (41).
- To guarantee stable PLL operation, apply a noise-free $\overline{\text{HSYNC}}$ signal (pin 6).
- Avoid heavy loading of the output pins.
- The supply voltage (V_{DD}) must be correctly decoupled. Connect decoupling capacitors as close as possible to the V_{DD} and V_{SS} pins.
- Position microcontroller optimal and away from components bearing high voltage and/or strong current.
- PLL loop filter ground of capacitors C_s and C_p must be directly connected to the V_{SS} pin (21). Avoid a ground loop and separate the ground from other digital signals ground.
- The connection between V_{SS} pin (21) and +5 V regulator ground/switching power supply secondary ground must be as short as possible.



(1) R = 10 to 47 kΩ; typ. 15 kΩ.
C_s = 100 to 470 nF; typ. 220 nF.
$C_p = {}^1/_{10}\ C_s$.
For mounting see Section 9.4.1 “Mounting precautions”.

(2) Example:
If f_1 = 15.750 kHz and (decimal value of 7-bit counter) = 32 then f_{VCO} = 8.064 MHz and the output of the Programmable 7-bit counter is 15.750 kHz.

Fig.12 On-chip OSD oscillator.

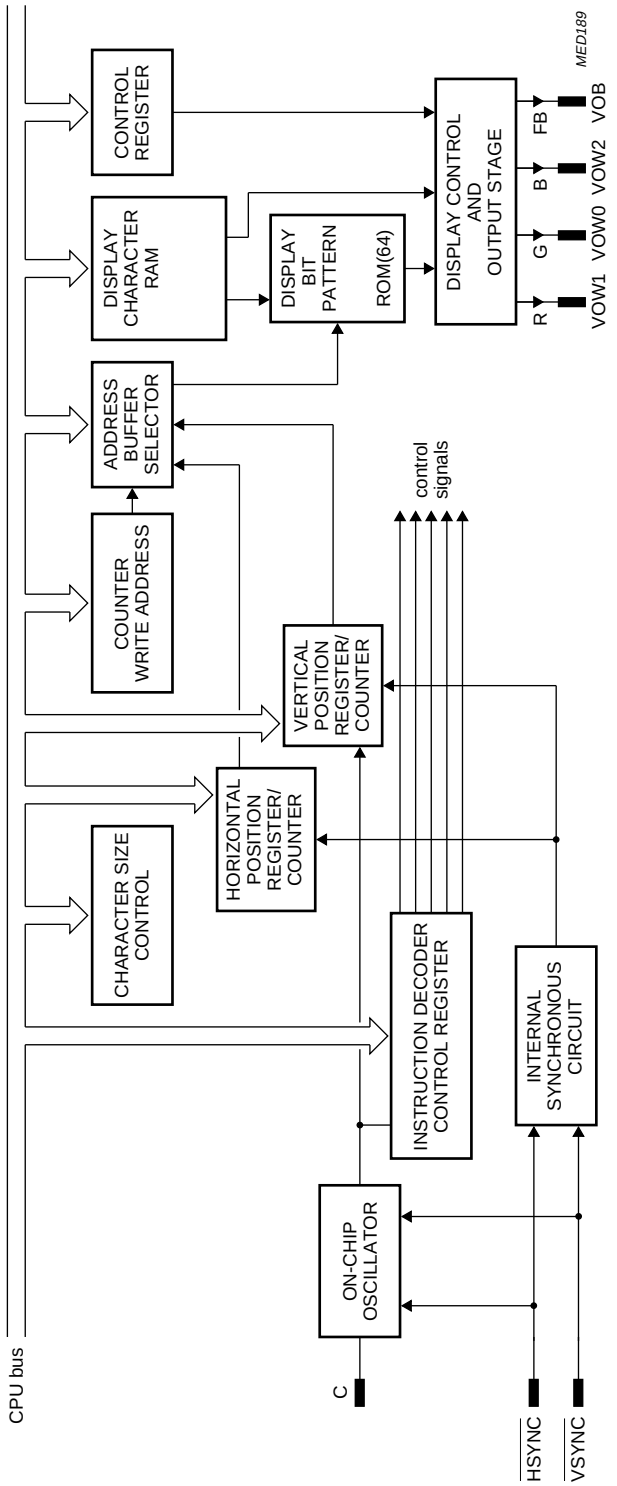


Fig.13 OSD block diagram.

10 DISPLAY RAM ORGANIZATION

The display RAM is organized as 64 × 10 bits.
The general format of each RAM location is as follows:

- Bits <9-4> hold data, comprising:
  - Customer designed Character Font Codes (62)
  - Carriage Return Code (1)
  - Space Code (1).
- Bits <3-0> contain the attributes of the Character Font:
  - Foreground colour and Blinking
  - Character size and Line space
  - Background colour and End-of-Display .

10.1 Description of display RAM codes

There are three data formats for the display RAM code

1. Character Font Code
2. Carriage Return Code
3. Space Code.

The three data formats and their descriptions are shown in Tables 9 to 17. Figure 14 illustrates an example of the timing of FB, R, G, and B pulses when displaying a line of dots stream in a character.
FB = VOB; R = VOW0, G = VOW1; B = VOW2.

Figure 15 shows an example of the screen which includes some Cariage Return and Space codes.

Table 9 Format of Character Font Code

9	8	7	6	5	4	3	2	1	0
C5	C4	C3	C2	C1	C0	T3	T2	T1	T0
Character Font Code (00H - 3DH)						Foreground colour			Blink

Table 10 Description of Character Font Code bits

SYMBOL	DESCRIPTION
C5 to C0	If bits <9-4> are in the range (00H to 3DH), then this is a Character Font Code and 1 from 62 customer designed character fonts can be selected.
T3 to T1	Bits <3-1> determine the (Foreground) colour (1 out of 8) of this character; see Table 11.
T0	Blinking of this character is controlled by bit <0>. See Section 12.3 for duty cycle and frequency control. When T0 = 0; blinking is OFF. When T0 = 1; blinking is ON. Blinking rate: $1/16$, $1/32$, $1/64$ or $1/128 \times f_{VSYNC}$.

Table 11 Selection of Background and Foreground colour

T3 (RED)	T2 (GREEN)	T1 (BLUE)	COLOUR
0	0	0	black
0	0	1	blue
0	1	0	green
0	1	1	cyan
1	0	0	red
1	0	1	magenta
1	1	0	yellow
1	1	1	white

Table 12 Format of Carriage Return Code

9	8	7	6	5	4	3	2	1	0
C5	C4	C3	C2	C1	C0	T3	T2	T1	T0
Carriage Return Code (3EH)						Character size		Line Spacing	

Table 13 Description of Carriage Return Code bits; format is shown in Table 12

SYMBOL	DESCRIPTION
C5 to C0	If bits <9-4> hold 3EH, then this is the Carriage Return Code. The current display line is terminated (a transparent pattern appears on the screen) and the next character will be displayed at the beginning of the next line.
T3 to T2	Bits <3-2> select the size of the of the character to be displayed on the next line; see Table 14.
T1 to T0	Bits <1-0> determine the spacing between lines of displayed characters. Spacing is a multiple of the number of horizontal scan lines. In order to prevent vertical jumping of the display, the first line should be a non-displayed line i.e. the Carriage Return Code. The line spacing for this code must not be zero; see Table 15.

Table 14 Selection of character size

T3	T2	CHARACTER DOT SIZE(1)
0	0	1H/1V
0	1	2H/2V
1	0	3H/3V
1	1	4H/4V

Table 15 Selection of line spacing

T1	T0	LINE SPACING
0	0	0H line
0	1	4H line
1	0	8H line
1	1	12H line

Note

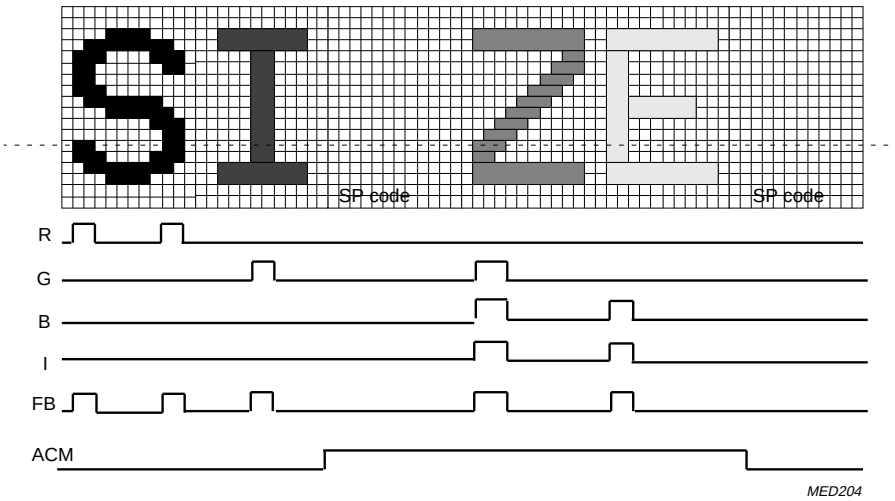
1. H is the OSD clock period; V is the number of horizontal scan lines per dot.

Table 16 Format of Space Code

9	8	7	6	5	4	3	2	1	0
C5	C4	C3	C2	C1	C0	T3	T2	T1	T0
Space Code (3FH)						Background colour			End

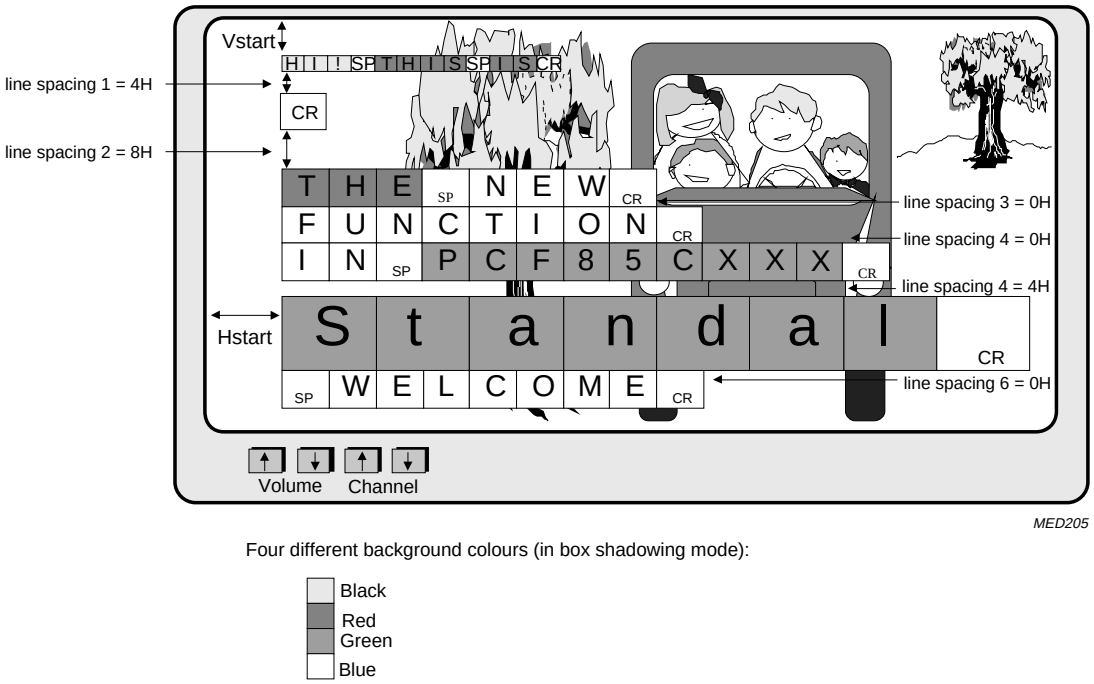
Table 17 Description of Space Code bits; format is shown in Table 16

SYMBOL	DESCRIPTION
C5 to C0	If bits <9-4> hold 3FH, then this is the Space Code. A transparent pattern, equal to one character width, will be displayed on the screen.
T3 to T1	Bits <3-1> determine the background colour of the characters including the Space Code in Box shadowing mode but following the Space Code in North-west shadowing mode. See Section 12.4 for more details. Background colour selection is the same as Foreground colour selection; see Table 11.
T0	Bit <0> is the End-of-Display bit and indicates the end of display of the current screen before exhaustion of display RAM. The last character displayed on the TV screen is either the 64th RAM location or a Space Code with the End-of-display attribute set to logic 1. When T0 = 0; continue display of next character. When T0 = 1; end of display.



"S" : red colour
"I" : green colour
"Z" : G+B+I colour
"E" : B+I colour
1st SP code : ACM = on
2nd SP code : ACM = off

Fig.14 R, G, B and FB timing.



Four different background colours (in box shadowing mode):

Black
Red
Green
Blue

Fig.15 On-screen-display (an example).

10.2 Loading character data into display RAM

Three Derivative Registers are used to address and load data into the display RAM. These registers (configurations are shown in Tables 18, 19 and 20) are described in the following Sections.

10.2.1 DCR ADDRESS REGISTER (DCRAR)

Table 18 DCRAR (address 30H)

7	6	5	4	3	2	1	0
–	–	A5	A4	A3	A2	A1	A0

This is Derivative Register 30 and bits <5-0> holds the address of the location in display RAM to which the data held in registers DCRTR and DCRCR will be written to. Bits <7-6> are reserved.

10.2.2 DCR ATTRIBUTE REGISTER (DCRTR)

Table 19 DCRTR (address 31H)

7	6	5	4	3	2	1	0
–	–	–	–	T3	T2	T1	T0

This is Derivative Register 31 and holds the character font attribute data. The data will be loaded into bits <3-0> of the location in RAM pointed to by the contents of DCRAR. Bits <7-4> are reserved.

10.2.3 DCR CHARACTER REGISTER (DCRCR)

Table 20 DCRCR (address 32H)

7	6	5	4	3	2	1	0
–	–	C5	C4	C3	C2	C1	C0

This is Derivative Register 32 and holds the character data that will be loaded into bits <9-4> of the location in RAM addressed by the contents of DCRAR. Bits <7-6> are reserved.

10.3 Writing character data to display RAM

1. Select the start address in display RAM. The start address is stored in DCRAR and can take any value between 0 and 63.
2. Load the character attributes into DCRTR. If the attributes of a series of displayed characters are the same, only DCRCR needs to be updated.

   The meaning of the attributes (4 bits) is dependent on the contents of the next command (the data in the DCRCR bits <5-0>; i.e. Carriage Return Code, Space Code or Character Font Code).
3. Load the character data into DCRCR. This operation loads the selected RAM location with the data held in registers DCRTR and DCRCR. The address held in DCRAR is then incremented by '1' pointing to the next RAM location in anticipation of the next operation.

Overflow of the DCRAR, i.e. overflow from 63 to 64, makes it reset to zero. After the instruction 'MOV D32H, A' is finished, the post-increment operation is performed automatically. Auto-post-increment operation:

Begin

(DCRAR) ≤ (DCRAR) + 1
If (DCRAR) > 63 then (DCRAR) ≤ 0

End

After master $\overline{\text{RESET}}$ the initial values of DCRAR, DCRTR and DCRCR are all zero. Figure 16 shows how DCRAR is incremented and advanced.

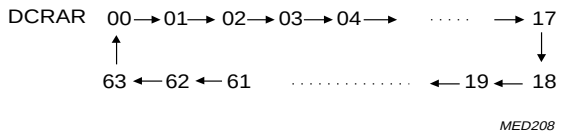


Fig.16 DCRAR increment cycle.

10.4 Default value of the display character

The default values of the display characters, after master $\overline{\text{RESET}}$, are as follows:

- Background colour = Blue (R = 0, G = 0, B = 1)
- Character size = 1V/1H
- End-of-Display control bit = 0.

If another set-up is needed, the first character should be SP code and second character is CR code to define the character size and background colour.

11 CHARACTER ROM

Each character font is stored in the on-chip character ROM in a 12 × 19 dot matrix. However, only elements in Rows 1 to 18 (12 × 18 dot matrix) can be selected as visible dots on the screen.

Row 0 is only used for the combination of two characters in a vertical direction when North-west shadowing mode is selected (for details see Section 12.4). Row 0 contains the same bit pattern of Row 18 of the character above it. If no combined character in vertical direction is intended for this character, Row 0 should be filled with all zeros.

11.1 Character ROM organization

ROM is divided into two parts: ROM1 and ROM2. The organization of the bit patterns stored in ROM1 and ROM2 and the file format to submit to Philips for customized character sets is shown in Fig.17.

A software package (OSDGEM) that assists in the design of character fonts on-screen and that also automatically generates the bit pattern HEX files is available on request. The package is run under the MS-DOS environment for IBM compatible PCs.

Regarding Fig.17 the following points should be noted.

1. Row 0 of each font is reserved for vertical combination of two fonts.
2. Binary 1 denotes visual dots.
3. ROM1 and ROM2 data files are in INTEL hex format on a byte basis. Each byte is structured High nibble followed by Low nibble.
4. The unused last byte of each font in ROM1 must be filled with FFH.
5. The unused last 2½ bytes in ROM2 must be filled with the same data as held in the corresponding address in ROM1.
6. The data bytes of the last 2 reserved fonts (Carriage Return and Space Codes) should be filled with 00H.
7. CS denotes Checksum.

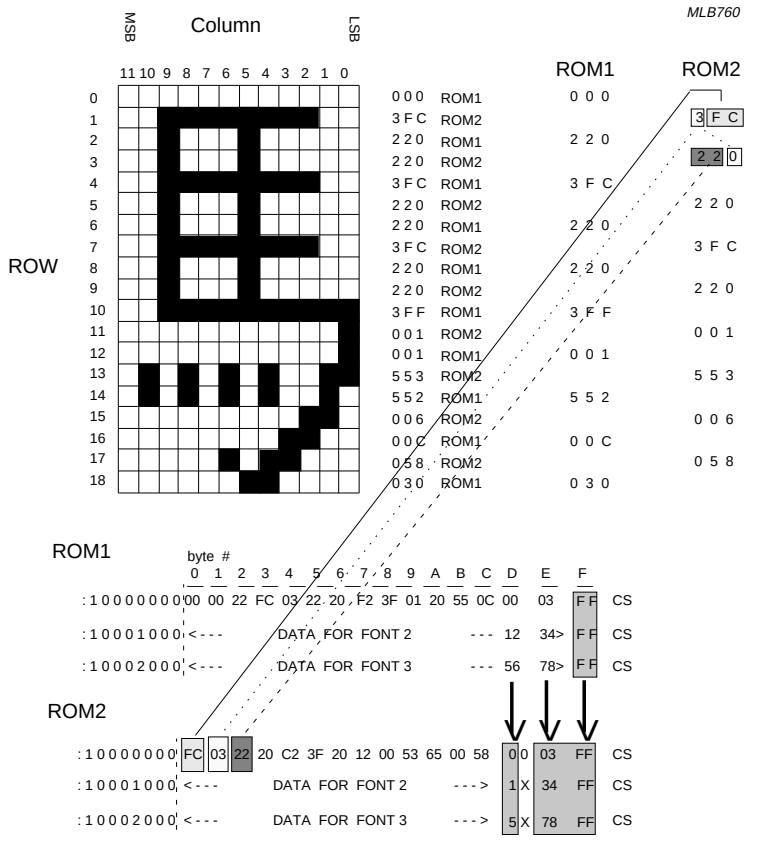


Fig.17 Font pattern stored in character ROM1 and ROM2.

12 OSD CONTROL REGISTERS

The functions of the OSD circuitry are controlled by the Derivative Registers as shown in Table 21.

Table 21 OSD Control Registers overview

NAME	DERIVATIVE REGISTER		FUNCTION
	NUMBER	ADDR	
CON1	22	22H	Enable TDAC; the I^2C-bus lines; the AFC functions and the VOW0 and VOW1 lines.
CON2	23	23H	Selects the output polarity of the PWM outputs and also enables and selects the VSYNC interrupt.
CON3	33	33H	Selects the blinking frequency and the active ratio of the blinking frequency for the OSD.
CON4	34	34H	Selects the 4 display modes; the active state of $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ and the output polarity of the FB and VOW0 to VOW2 outputs. It also enables/disables the OSD clock.
VPOS	35	35H	Selects the vertical starting position of the display row.
HPOS	36	36H	Selects the horizontal starting position of the display row.
BCC	37	37H	Selects the background colour.

12.1 Derivative Register 22 (CON1)

Table 22 Derivative Register 22 (address 22H)

7	6	5	4	3	2	1	0
TDACE	SCLE	SDAE	ADC2E	ADC1E	ADC0E	VOW1E	VOW0E

Table 23 Description of Derivative Register 22 bits

BIT	SYMBOL	DESCRIPTION
7	TDACE	Pulse Width Modulated output TDAC enable bit. When: TDACE = 1; pin DP13/TDAC is selected as output TDAC. TDACE = 0; pin DP13/TDAC is selected as Derivative Port line DP1.
6	SCLE	I^2C-bus clock enable bit. When: SCLE = 1; pin DP21/SCL is selected as SCL (I^2C-bus clock line). SCLE = 0; pin DP21/SCL is selected as Derivative Port line DP21.
5	SDAE	I^2C-bus data enable bit. When: SDAE = 1; pin DP20/SDA is selected as SDA (I^2C-bus data line). SDAE = 0; pin DP20/SDA is selected as Derivative Port line DP20.
4	AFCE2	These 3 bits select the pin function of DP1i/AFC and enable/disable the comparator in the AFC circuit; for the selection and enable/disable function see Table 7.
3	AFCE1	
2	AFCE0	
1	VOW1E	Pin function selection bit. When: VOW1E = 1; pin DP22/VOW1 is selected as VOW1. VOW1E = 0; pin DP22/VOW1 is selected as Derivative Port line DP22.
0	VOW0E	Pin function selection bit. When: VOW0E = 1; pin DP23/VOW1 is selected as VOW1. VOW0E = 0; pin DP23/VOW1 is selected as Derivative Port line DP23.

12.2 Derivative Register 23 (CON2)

Table 24 Derivative Register 23

7	6	5	4	3	2	1	0
VINT	VIEN	–	–	–	P14LVL	P7LVL	P6LVL

Table 25 Description of Derivative Register 23 bits

BIT	SYMBOL	DESCRIPTION
7	VINT	Bit VINT indicates if the interrupt comes from $\overline{\text{VSYNC}}$ (if VINT = 1 and VIEN = 1) or I^2C-bus when the CPU gets interrupted by interrupt vector address 7.
6	VIEN	The $\overline{\text{VSYNC}}$ leading edge (active level detection automatically done by the PCA84C646/PCA84C846) generates an interrupt if bit VIEN = 1 and the SIO interrupt is enabled (i.e. the I^2C-bus and the $\overline{\text{VSYNC}}$ interrupt shares the same interrupt vector).
5 to 4	–	These three bits are reserved.
2	P14LVL	Polarity select bit for output TDA. When: P14LVL = 1; the TDAC output is inverted. P14LVL = 0; the TDAC output is not inverted.
1	P7LVL	Polarity select bit for outputs PWM00 to PWM03. When: P7LVL = 1; the outputs PWM00 to PWM03 are inverted. P7LVL = 0; the outputs PWM00 to PWM03 are not inverted.
0	P6LVL	Polarity select bit for outputs PWM04 to PWM07. When: P6LVL = 1; the outputs PWM04 to PWM07 are inverted. P6LVL = 0; the outputs PWM04 to PWM07 are not inverted.

12.3 Derivative Register 33 (CON3)

Derivative Register 33 is to control the character blinking related operation. Figure 18 shows the timing diagram of character blinking frequency and blinking ratio.

Table 26 Derivative Register 33

7	6	5	4	3	2	1	0
–	–	–	–	BR1	BR0	BF1	BF0

Table 27 Description of Derivative Register 33 bits

BIT	SYMBOL	DESCRIPTION
7 to 4	–	These 4 bits are reserved.
3	BR1	Blinking active ratio select bits. These two bits allow one from a choice of three active blinking ratios to be selected; see Table 28.
2	BR0	
1	BF1	Blinking frequency select bits. These two bits allow one from a choice of four blinking frequencies to be selected. Blinking frequency $= \frac{f_{VSYNC}}{16 \times 2^{(BF1, BF0)}}$ Hz, where '$2^{(BF1, BF0)}$' is a decimal value determined by bits BF1 and BF0; see Table 29.
0	BF0	

Table 28 Active ratio determined by bits BR1 and BR0

BR1	BR0	ACTIVE RATIO
0	0	3 : 1 (default)
0	1	1 : 1
1	0	1 : 3
1	1	reserved

Table 29 Blinking frequency determined by (BF1,BF0)

BF1	BF0	$2^{(BF1, BF0)}$	BLINKING FREQUENCY (Hz)
0	0	1	$1/16 \times f_{VSYNC}$
0	1	2	$1/32 \times f_{VSYNC}$
1	0	4	$1/64 \times f_{VSYNC}$
1	1	8	$1/128 \times f_{VSYNC}$ (default)

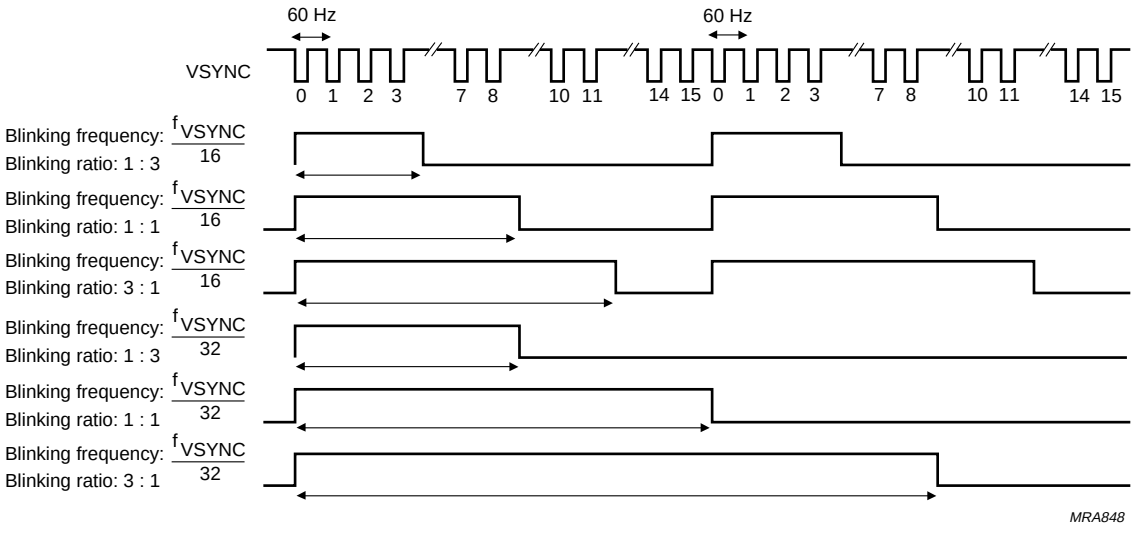


Fig.18 Example of character blinking (NTSC 525LPF/60Hz).

12.4 Derivative Register 34 (CON4)

This register selects the 4 display modes(Mode 0 to Mode 3); the active state of $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ and the output polarity of the FB and VOW0 to VOW2 outputs. It also enables/disables the OSD clock (f_{OSD}).

Table 30 Derivative Register 34

7	6	5	4	3	2	1	0
–	–	S1	S0	Hp	Vp	Bp	EN

Table 31 Description of Derivative Register 34 bits

BIT	SYMBOL	DESCRIPTION
7	–	These two bits are reserved.
6	–	
5	S1	Display mode select bits; see Table 32.
4	S0	
3	Hp	$\overline{\text{HSYNC}}$ signal polarity control bit (see Fig.19). When Hp = 1; the active level of $\overline{\text{HSYNC}}$ is HIGH. When Hp = 0; the active level of $\overline{\text{HSYNC}}$ is LOW (default state).
2	Vp	$\overline{\text{VSYNC}}$ signal polarity control bit (see Fig.19). When Vp = 1; the active level of $\overline{\text{VSYNC}}$ is HIGH. When Vp = 0; the active level of $\overline{\text{VSYNC}}$ is LOW (default state).
1	Bp	Output polarity control bit for FB, VOW0, VOW1 and VOW2 (see Fig.20). When Bp = 1; the polarity of FB, VOW0, VOW1 and VOW2 is HIGH (default state). When Bp = 0; the polarity of FB, VOW0, VOW1 and VOW2 is LOW.
0	EN	OSD clock enable/disable bit. When EN = 1; the OSD clock is enabled. When EN = 0; the OSD clock is disabled.

Table 32 Selection of Display Modes

S1	S0	DISPLAY MODE
0	0	Mode 0 No background mode (see Fig.21). The OSD fonts/characters are directly superimposed on the TV video signals.
0	1	Mode 1 North-west shadowing mode (see Fig.22). Available only in the character size 2V/2H or 4V/4H (V: horizontal line; H: OSD clock).The shadows of the characters are generated by placing a light source on the North-west 45 degree direction (see also Figs 25 and 26). When designing the character bit pattern, care must be taken that the shadows generated by this mode is only within the cell boundary in vertical direction (see Figs 28 and 29 for details). But shadows generated by this mode in horizontal direction has no boundary limitation (Fig.30).
1	0	Mode 2 Box shadowing mode (see Fig.23). Box shadowing is to surround the character font by a 12×18 dots box in background, i.e. within the character font cell; locations with no foreground dots are filled with background dots (see Fig.27).
1	1	Mode 3 Frame shadowing mode (raster blanking; see Fig.24); background colour displayed on full screen where no bit patterns are on.The background colour is controlled by Derivative Register 37 and has 8 different colours; see Table 39.

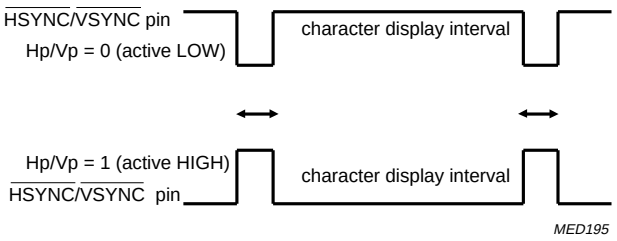


Fig.19 Bits Hp/Vp determine the active level of the HSYNC/VSYNC signal.

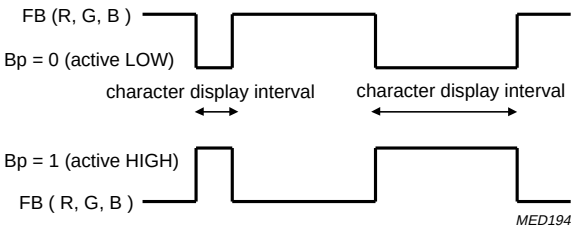


Fig.20 Bit Bp determines the active level of FB, R, G and B.

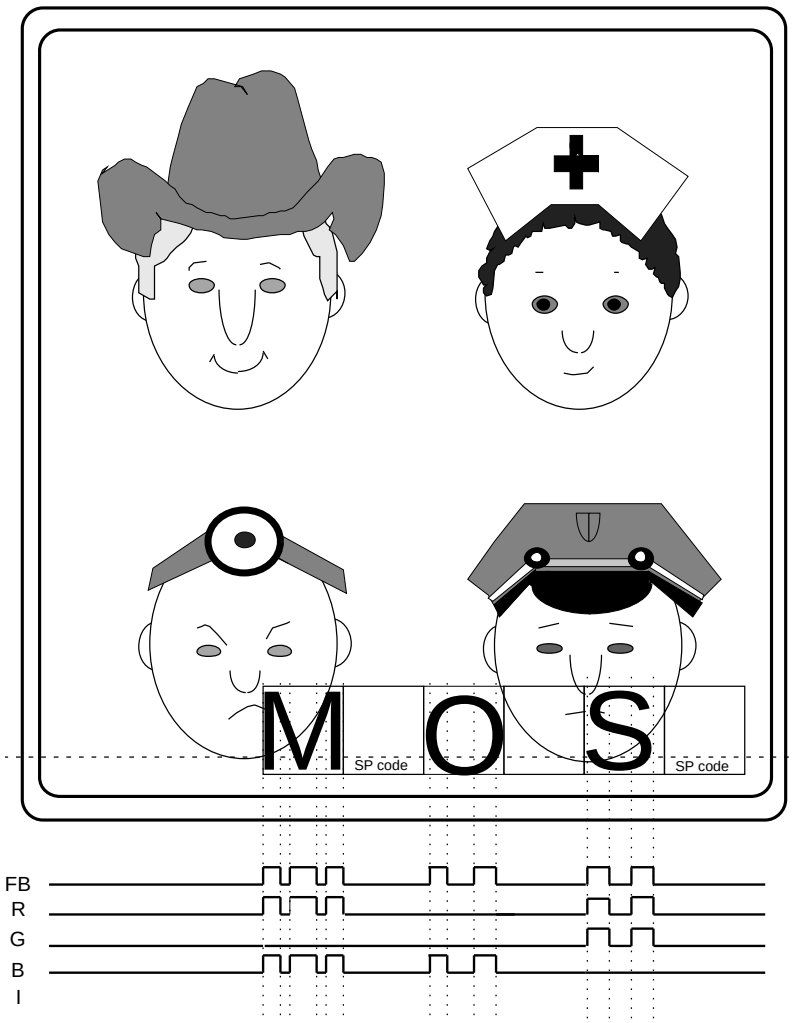
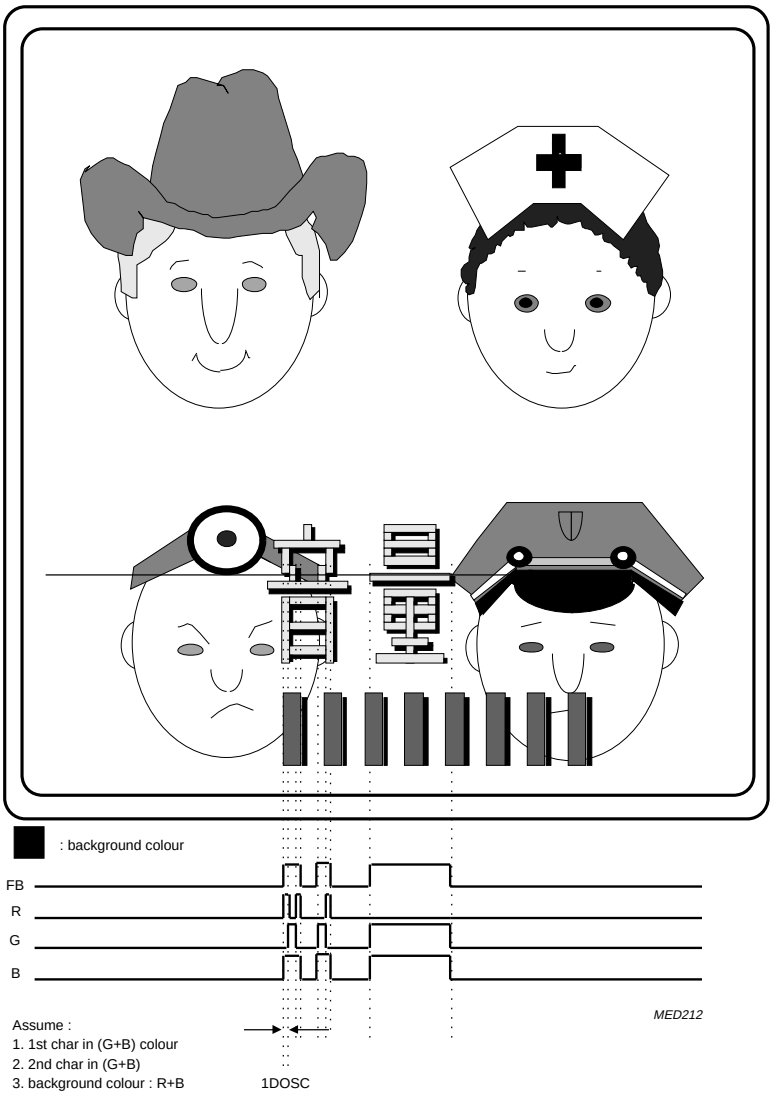


Fig.21 Mode 0: No Background (superimpose) mode.



Available only in character size 2V/2H or 4V/4H.

Fig.22 Mode 1: North-west shadowing mode.

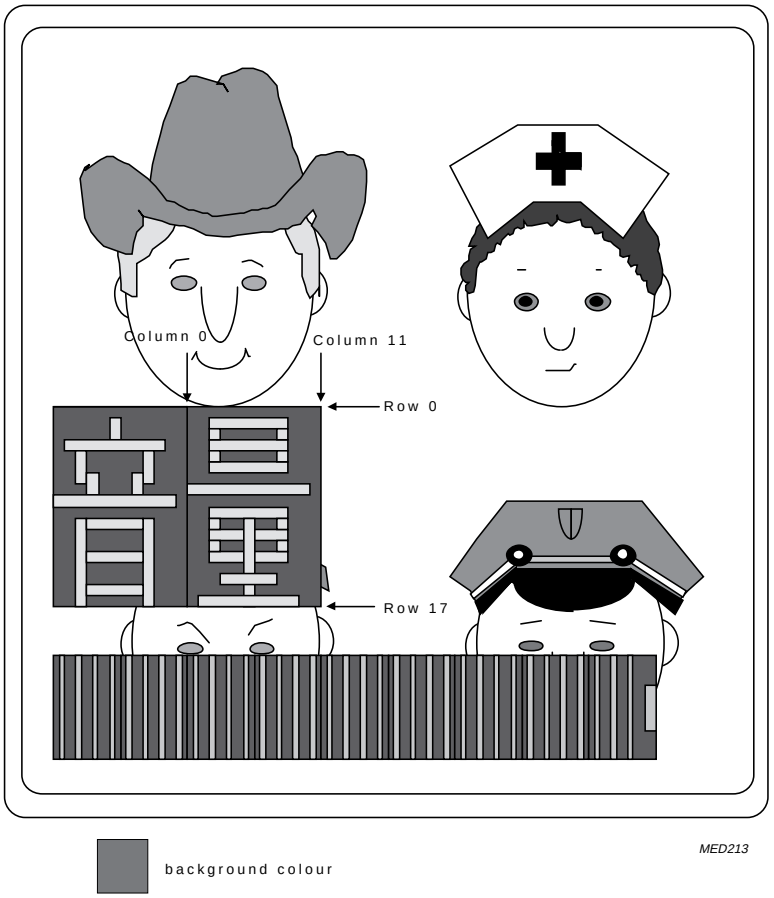


Fig.23 Mode 2: Box shadowing mode.

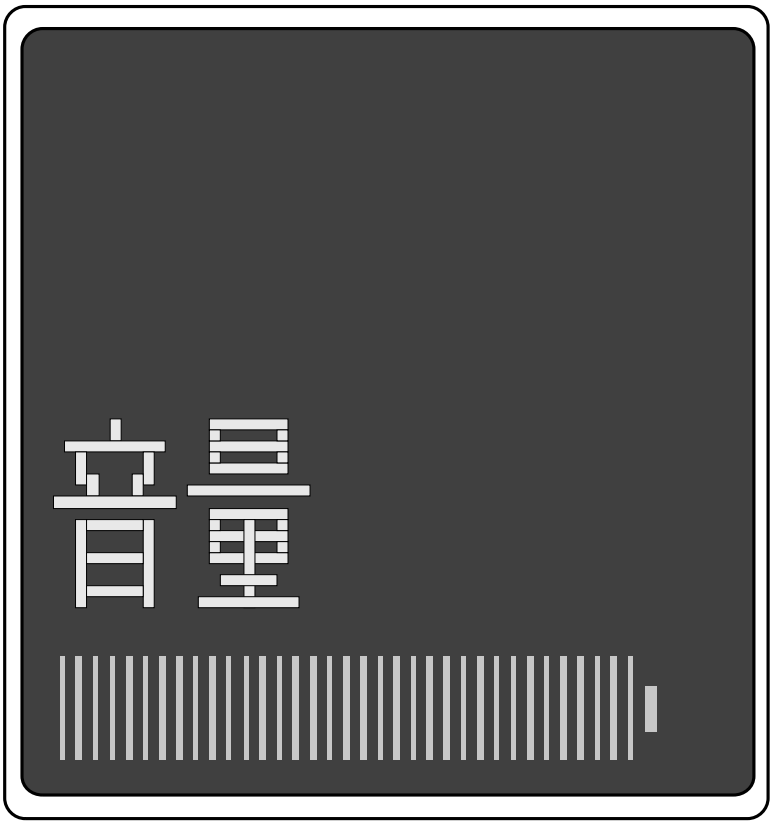


Fig.24 Mode 3: Frame shadowing mode.

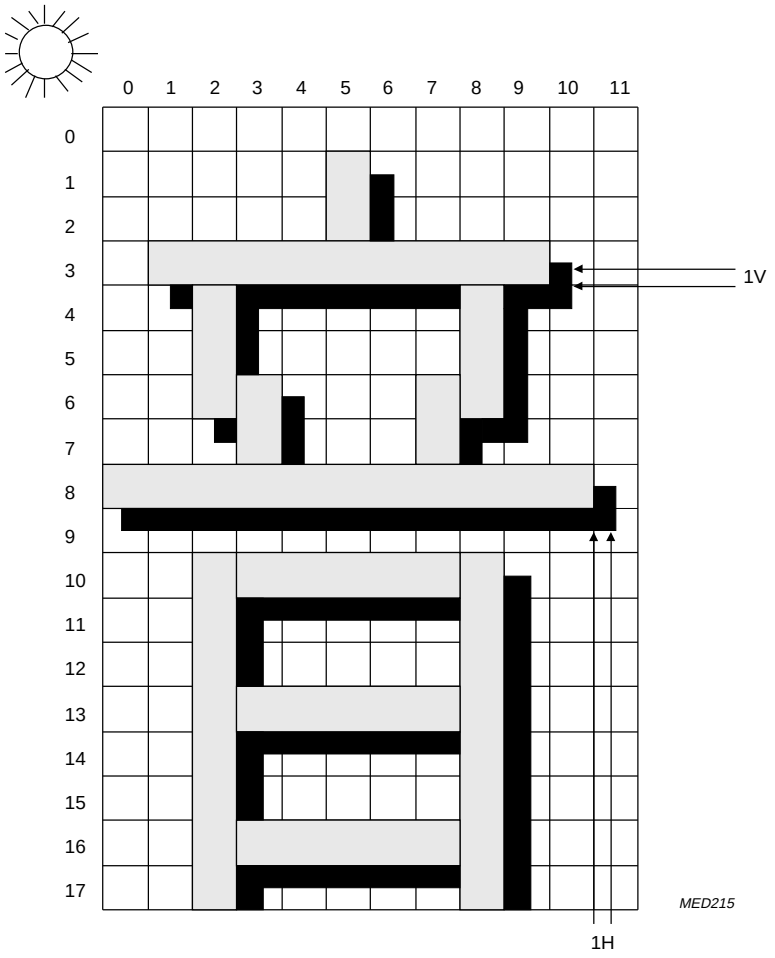


Fig.25 Example of North-west shadowing mode; size = 2V/2H.

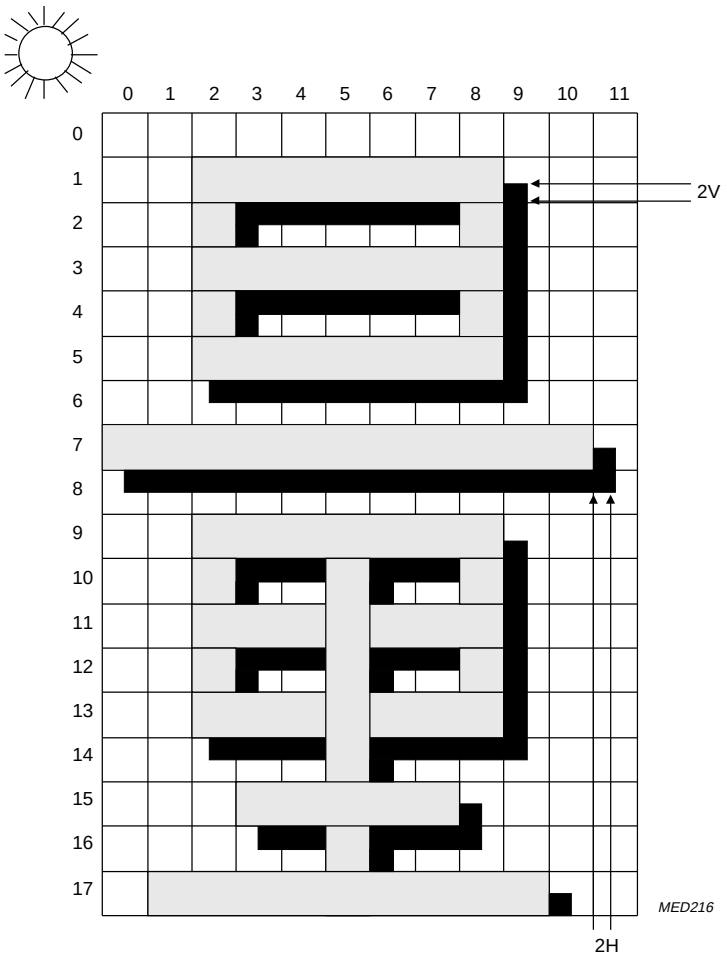


Fig.26 Example of North-west shadowing mode; size = 4V/4H.

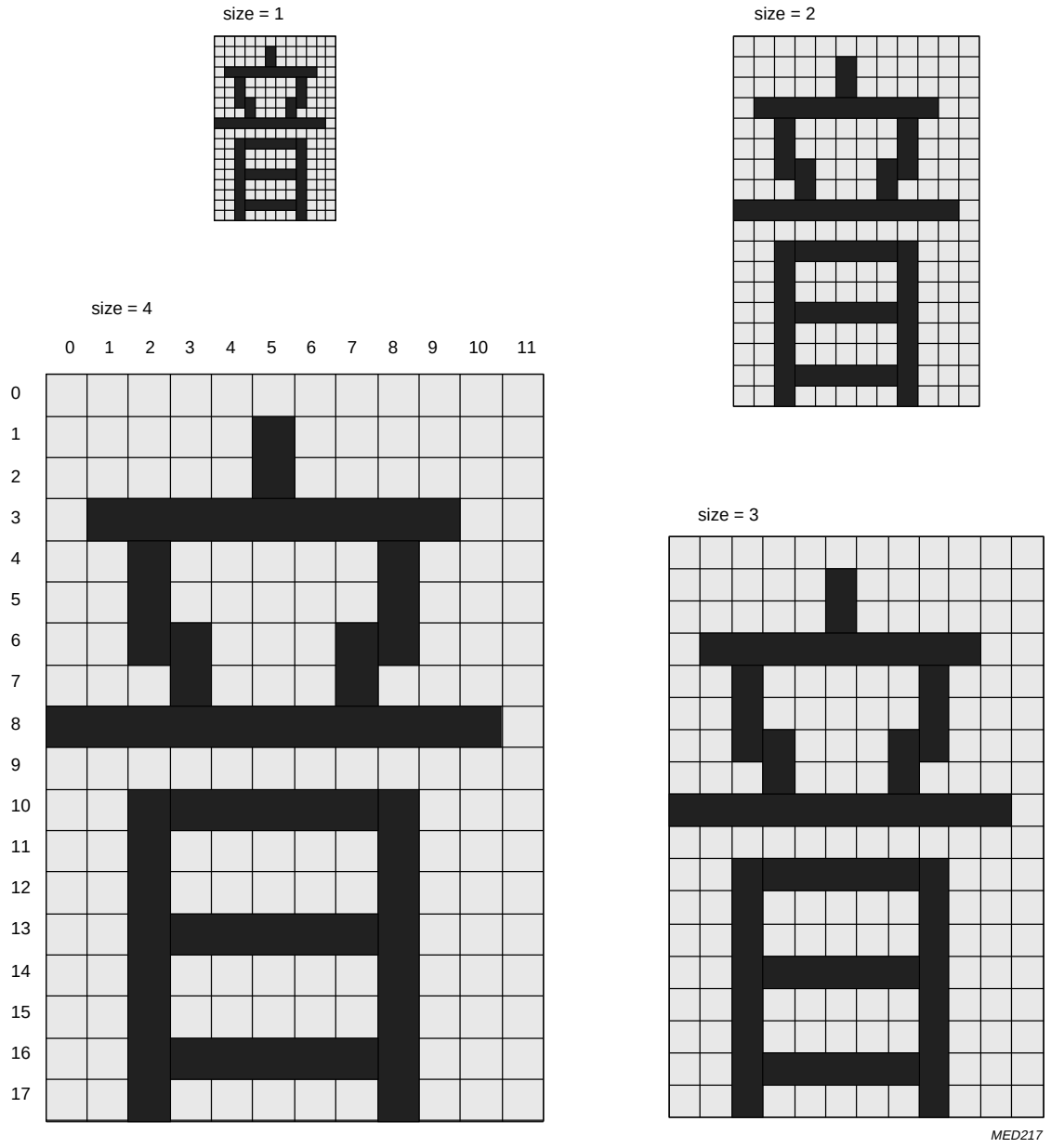


Fig.27 Example of Box shadowing mode.

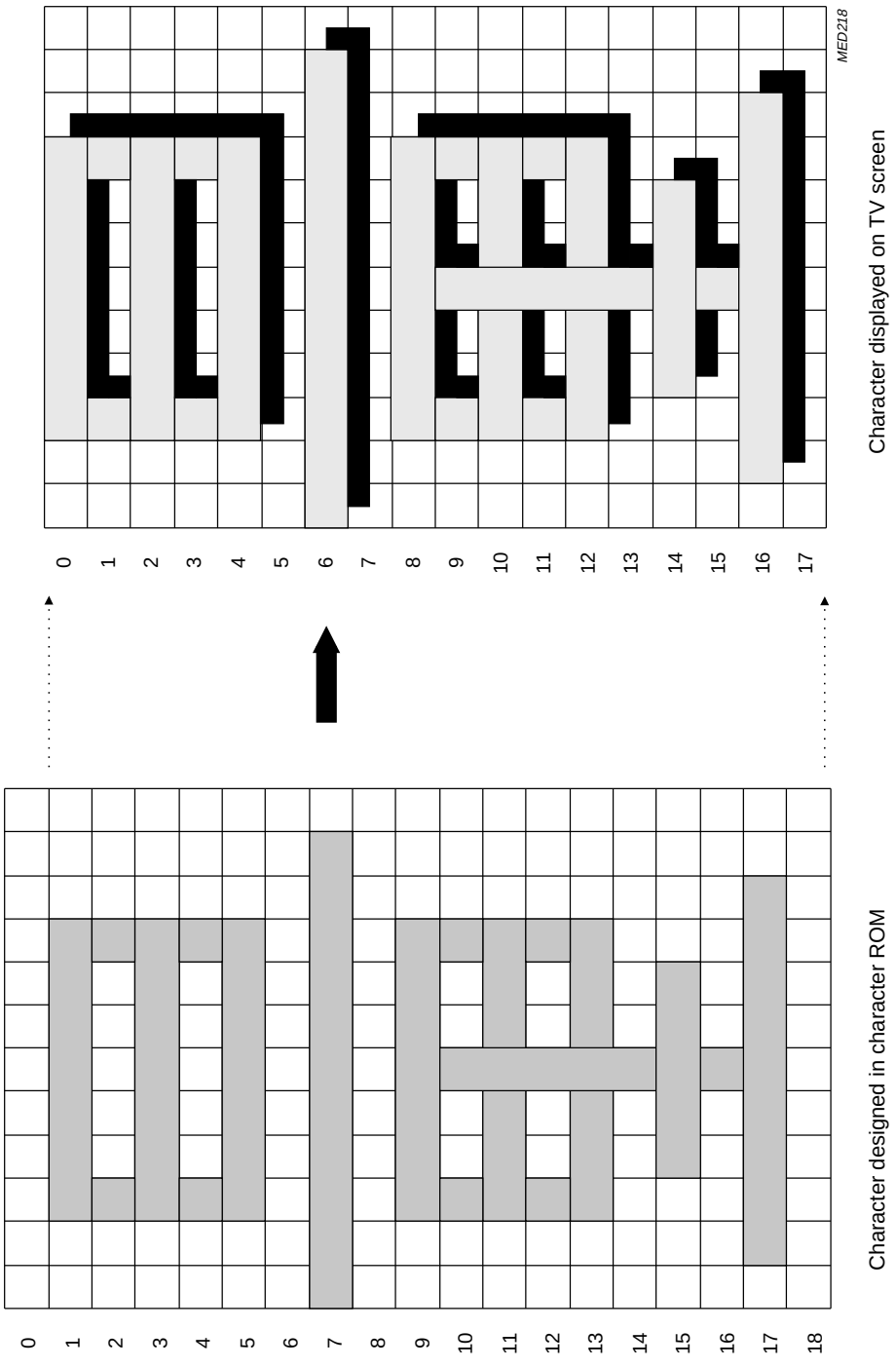


Fig.28 Example 1: North-west shadowing mode; shadow within cell boundary.

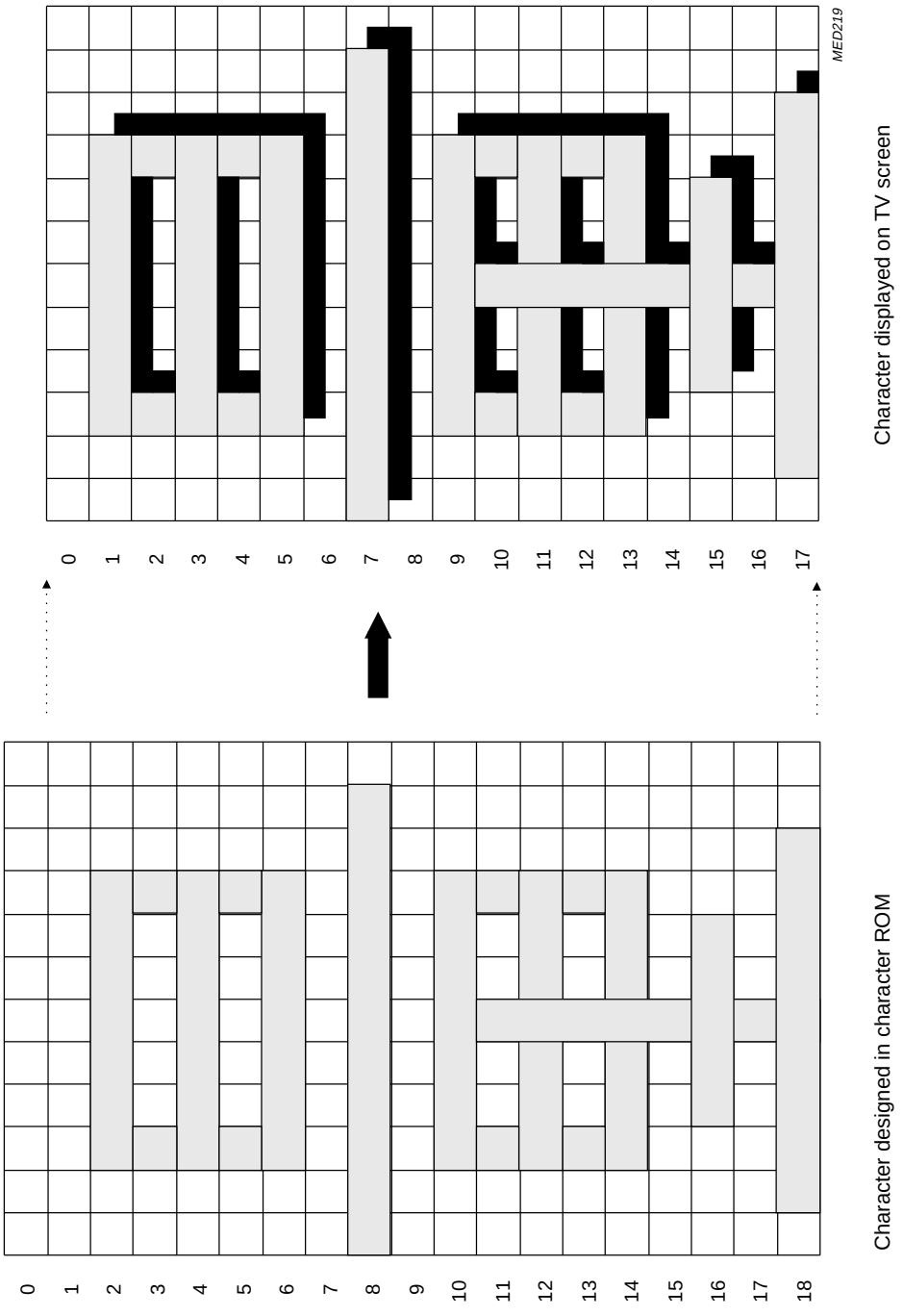
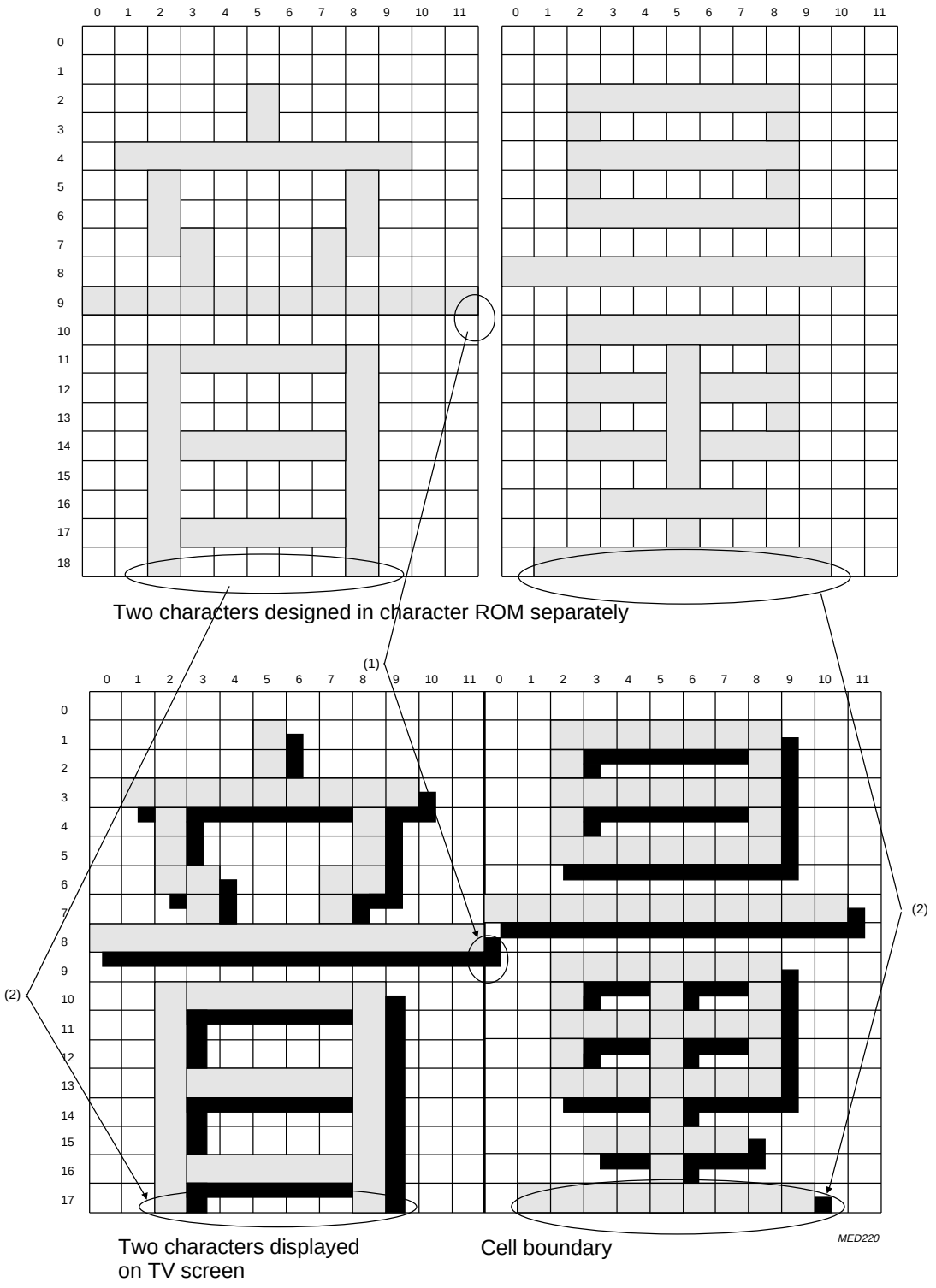


Fig.29 Example 2: North-west shadowing mode; shadow out of cell boundary.



(1) Horizontal shadowing overflow into the next character cell.

(2) Vertical shadowing overflow does not show beyond the bottom of a cell.

Fig.30 North-west shadowing.

12.4.1 SPACE CODE AND CARRIAGE RETURN CODE IN DIFFERENT BACKGROUND/SHADOWING MODES

Mode 0 No background mode. Both the Space Code and the Carriage Return Code are displayed as transparent (no bit) patterns, with the video signal as the background.

Mode 1 North-west shadowing mode. Similar to Mode 0.

Mode 2 Box shadowing mode. The Space Code is displayed as a transparent pattern with selected background colour. This will also be the background colour of the character following the Space Code. However, when the Space Code is used as an end bit, it will be displayed as a transparent pattern superimposed on the video. The Carriage Return Code in Mode 2 is also displayed as a transparent pattern superimposed on the video signal.

Mode 3 Frame shadowing mode. The Space Code and Carriage Return code is displayed as a transparent pattern with background colour; see Table 39.

Space Code and Carriage Return Code in the 4 different background/shadowing modes (0 to 3), with:

- Blinking OFF are shown in Figs 31, 32, 33 and 34.
- Blinking ON are shown in Figs 36, 37, 38 and 39.

Figure 39 shows blinking of a character only within the 12×18 cell boundary. If the shadow of the blinking character crosses over the boundary of the cell of the character next to the one that is not blinking, the shadow dot will still appear on the screen regardless whether the blinking character is ON or OFF.

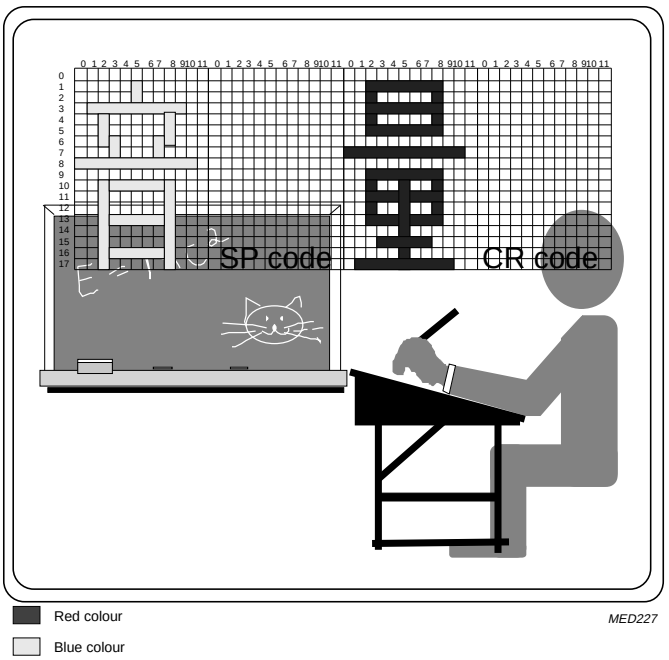


Fig.31 SP and CR codes in Mode 0: No background mode (superimpose; transparent pattern).

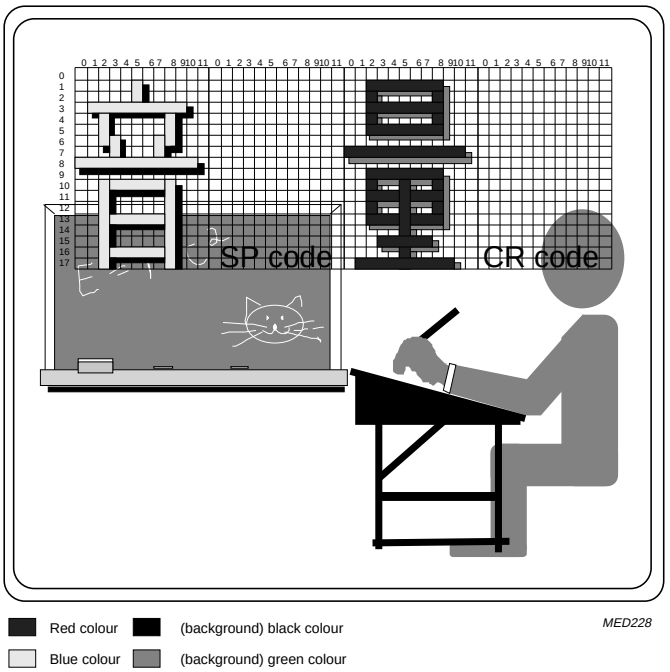
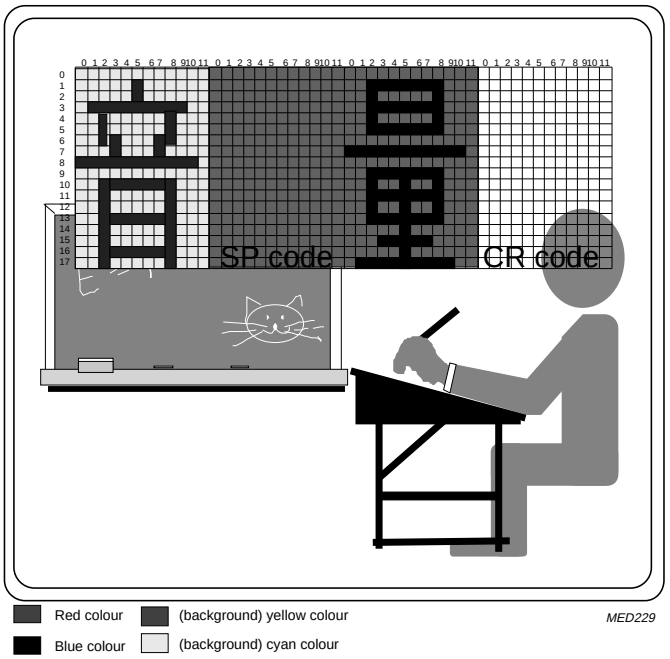
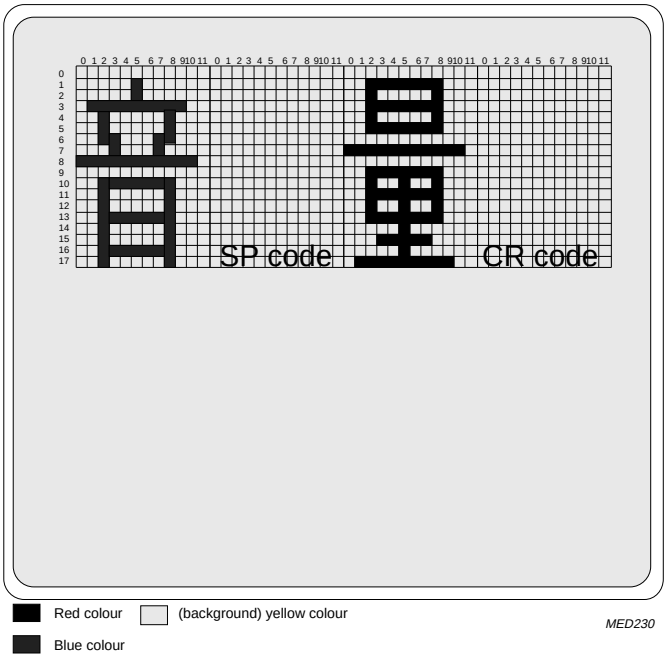


Fig.32 SP and CR codes in Mode 1: North-west shadowing mode (transparent pattern).



SP code is a transparent pattern with the background colour of the character it intends to change or keep.
CR code is always a transparent pattern with the video signal as its background.
SP code can change the background colour of itself and the character/word next to it (in this example: from cyan to yellow).

Fig.33 SP and CR codes in Mode 2: Box shadowing mode.



SP and CR codes are all transparent pattern with the background colour as its colour.

Fig.34 SP and CR codes in Mode 3: Frame shadowing mode.

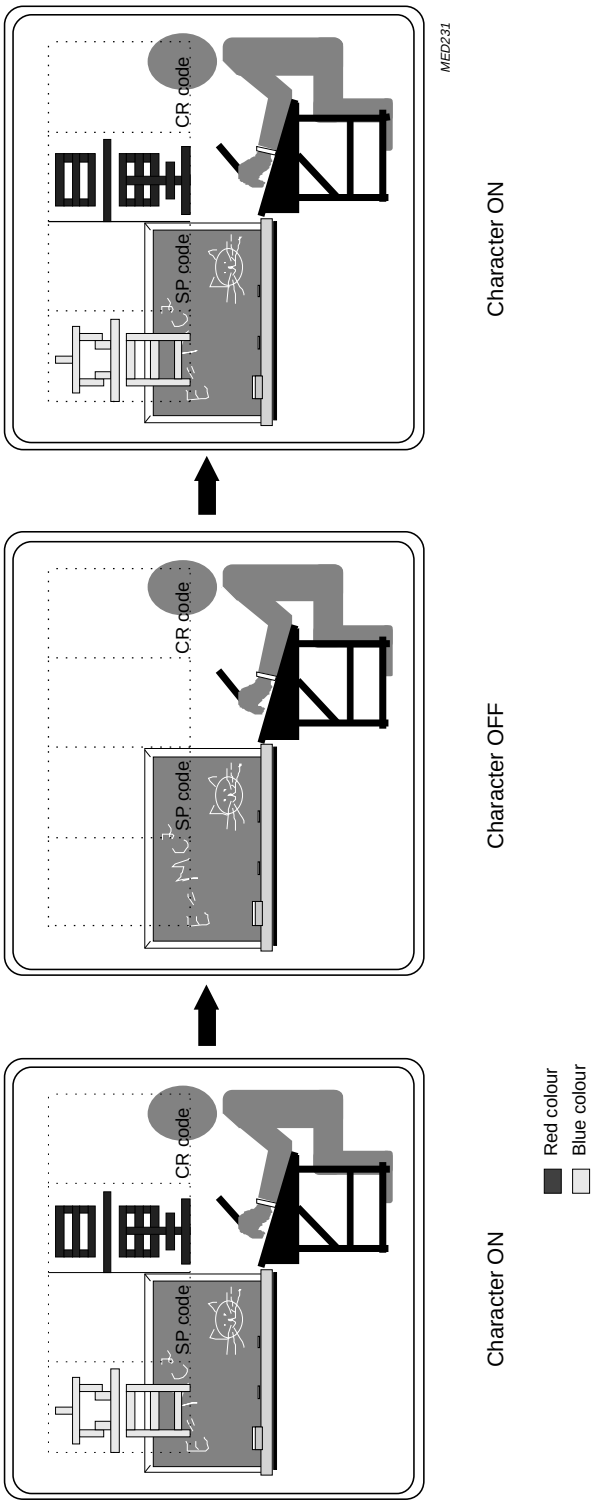


Fig.35 SP and CR codes in Mode 0: No background mode (superimpose; transparent pattern) with blinking of character is set to active.

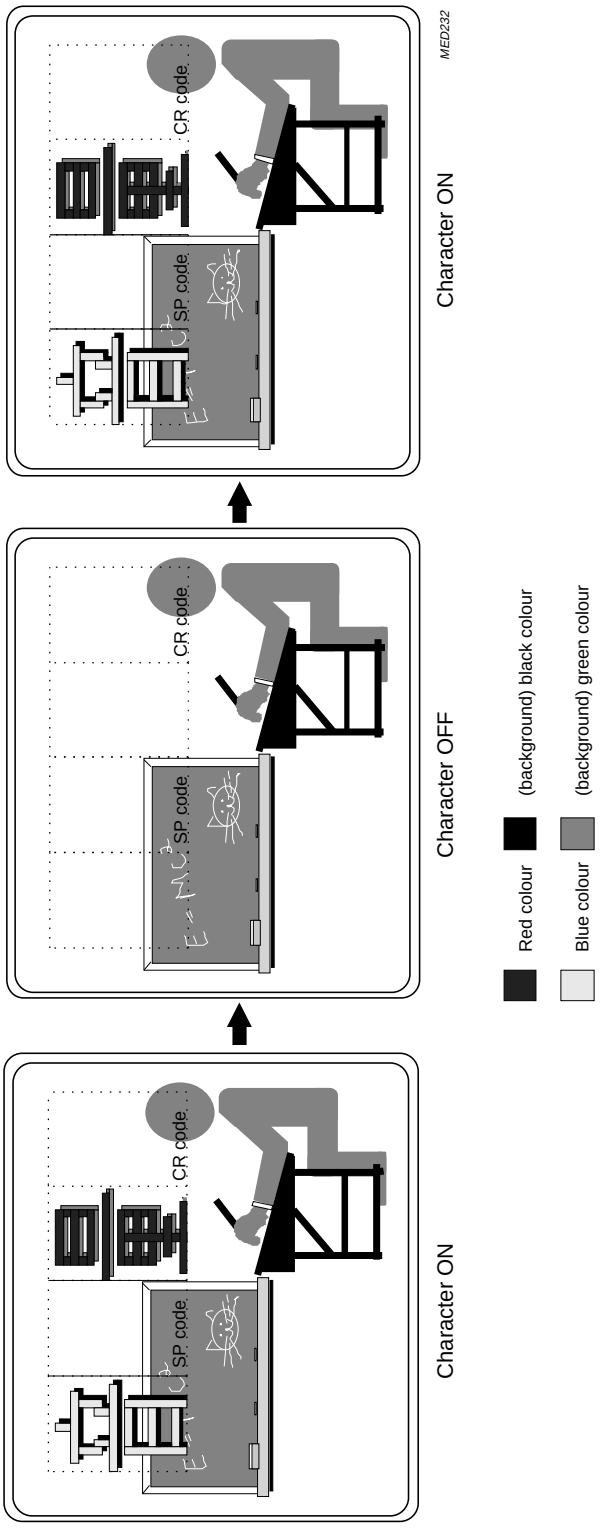


Fig.36 SP and CR codes in Mode 1: North-west shadowing mode (transparent pattern) with blinking of character is set to active.

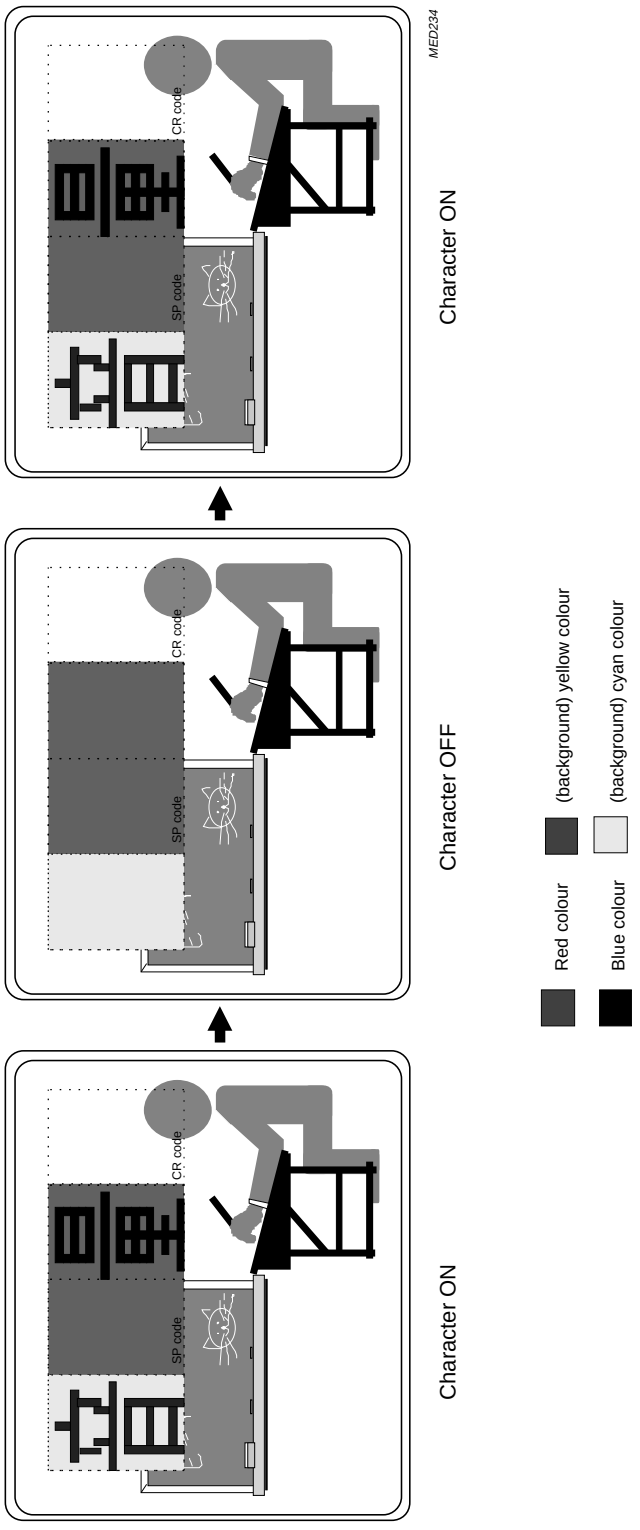


Fig.37 SP and CR codes in Mode 2: Box shadowing mode with blinking of character set to active.

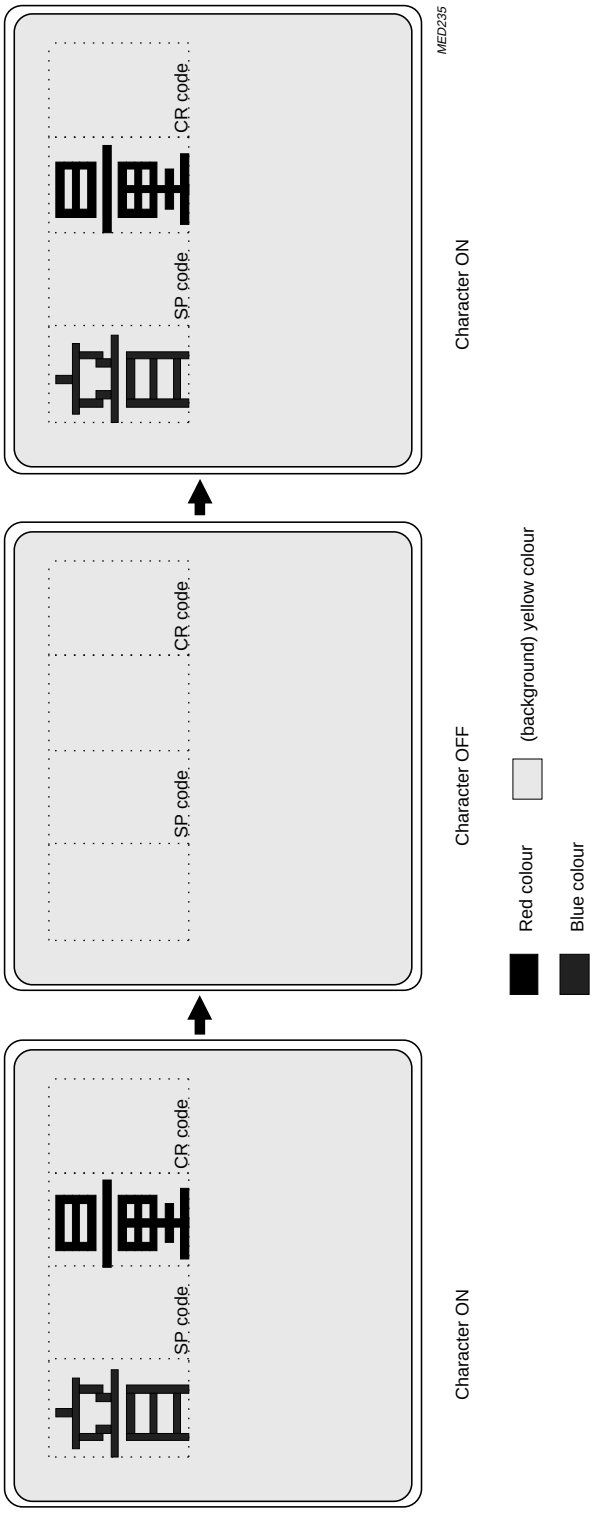
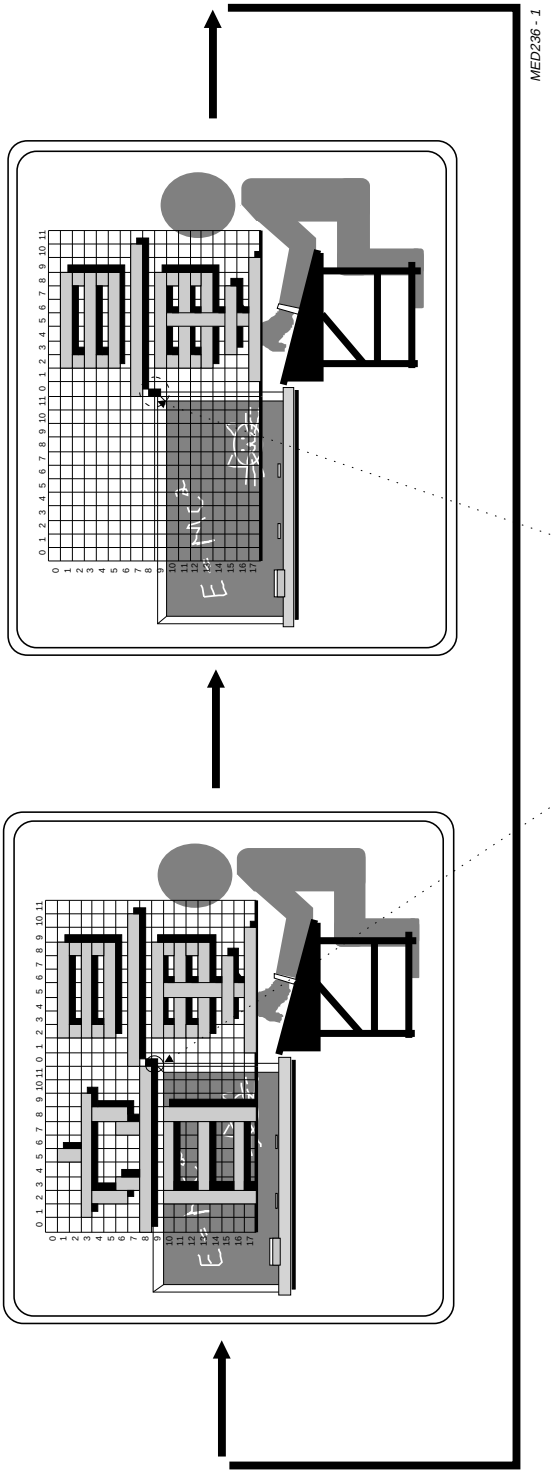


Fig.38 SP and CR codes in Mode 3: Frame shadowing mode with blinking of character set to active.



In this example:
- 1st character is in blinking mode
- 2nd character is not
- the first character bit pattern is designed such that the north-west shadow of the 1st character falls into the cell of 2nd character.

When the 1st character is blinking and displayed on the screen there is no problem. However, when the 1st character is off then the shadow of the 1st character falls into 2nd character cell and will remain there.

To avoid this happening:
- design bit pattern in such a way that shadow does not cross the cell boundary
- make adjacent characters all blinking or all not blinking.

Fig.39 Blinking of character is within the character cell only (12 × 18).

12.5 Derivative Register 35 (VPOS)

Derivative Register 35 selects the vertical starting position of the display row.

Table 33 Derivative Register 35 (address 35H)

7	6	5	4	3	2	1	0
–	–	V5	V4	V3	V2	V1	V0

Table 34 Description of Derivative Register 35 bits

BIT	SYMBOL	DESCRIPTION
7 to 6	–	Reserved.
5	V5	These 6 bits enable 1 of 64 vertical start positions to be selected for the display row. The vertical starting position is calculated as follows: VP = [4 × (V5 to V0)] × horizontal scan lines Where (V5 to V0) is the decimal value of the contents of Register 35; (V5 to V0) ≥ 0.
4	V4	
3	V3	
2	V2	
1	V1	
0	V0	

12.6 Derivative Register 36 (HPOS)

Derivative Register 36 selects the horizontal starting position of the display row.

Table 35 Derivative Register 36 (address 36H)

7	6	5	4	3	2	1	0
–	–	H5	H4	H3	H2	H1	H0

Table 36 Description of Derivative Register 36 bits

BIT	SYMBOL	DESCRIPTION
7 to 6	–	Reserved.
5	H5	These 6 bits enable 1 of 64 horizontal start positions to be selected for the display row. The horizontal starting position is calculated as follows: HP = [4 × (H5 to H0) + 5] × OSD clock cycle Where (H5 to H0) is the decimal value of the contents of Register 36; (H5 to H0) ≥ 10.
4	H4	
3	H3	
2	H2	
1	H1	
0	H0	

12.7 Derivative Register 37 (BCC)

Derivative Register 37 selects the background colour when the OSD is in Frame shadowing mode.

Table 37 Derivative Register 37

7	6	5	4	3	2	1	0
–	–	–	–	–	BCR	BCG	BCB

Table 38 Description of Derivative Register 37 bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	Reserved.
2	BCR	These three bits are used to select the background colour in Frame shadowing mode; see Table 39.
1	BCG	
0	BCB	

Table 39 Selection of Background colour in Frame shadowing mode

BCR (RED)	BCG (GREEN)	BCB (BLUE)	COLOUR
0	0	0	black
0	0	1	blue
0	1	0	green
0	1	1	cyan
1	0	0	red
1	0	1	magenta
1	1	0	yellow
1	1	1	white

13 COMBINATION OF TWO OR MORE FONT CELLS TO FORM A NEW FONT

The user can combine two (or more) font cells to form a new higher resolution pattern; see Figs 40, 41, 42 and 43.

Combination of two cells in horizontal direction needs no special care. All 4 background/shadowing modes are applicable; see Figs 40 and 41.

However the combination of two cells in a vertical direction needs the following special care:

- Space between two rows should be programmed as ‘0’ (bit <1-0> of Carriage Return Code = 00).
- Row 0 in the character ROM is to be used in the North-west shadowing mode. If this mode is intended for use by this formed character font, the ROW 0 should contain the bit pattern of Row 18 of the font above it (see Figs 42 and 43).

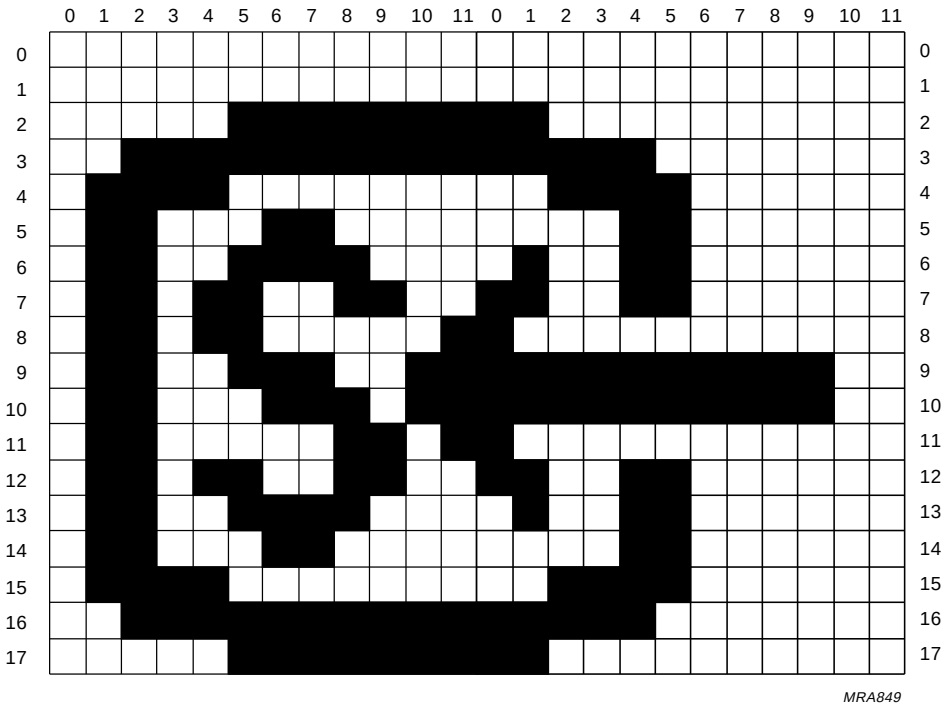


Fig.40 Combination of two character cells in horizontal direction to form a new font; without shadowing.

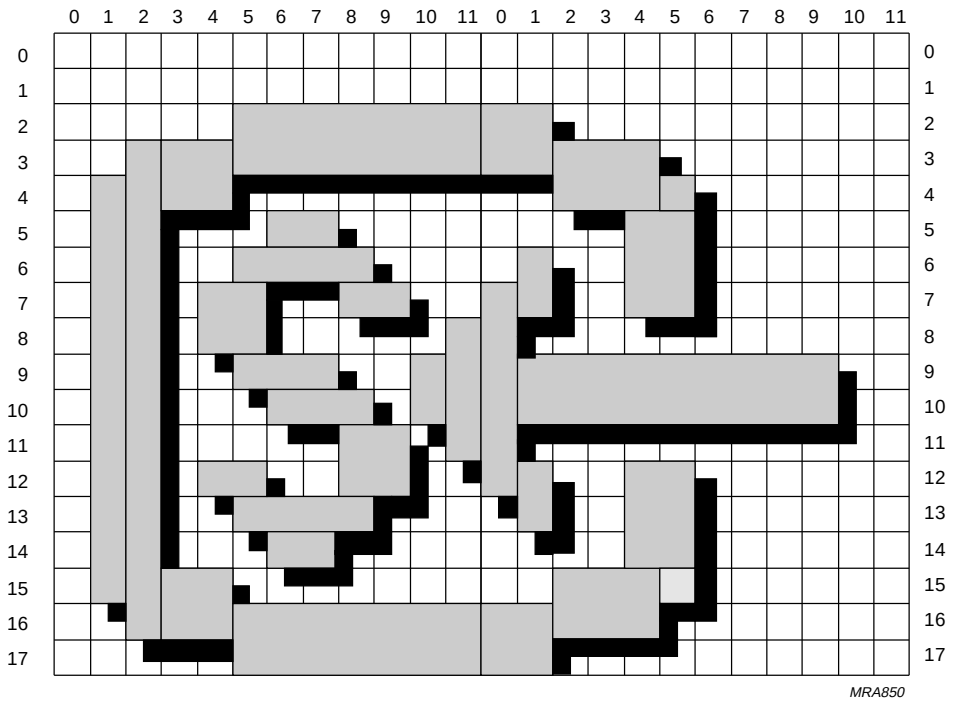
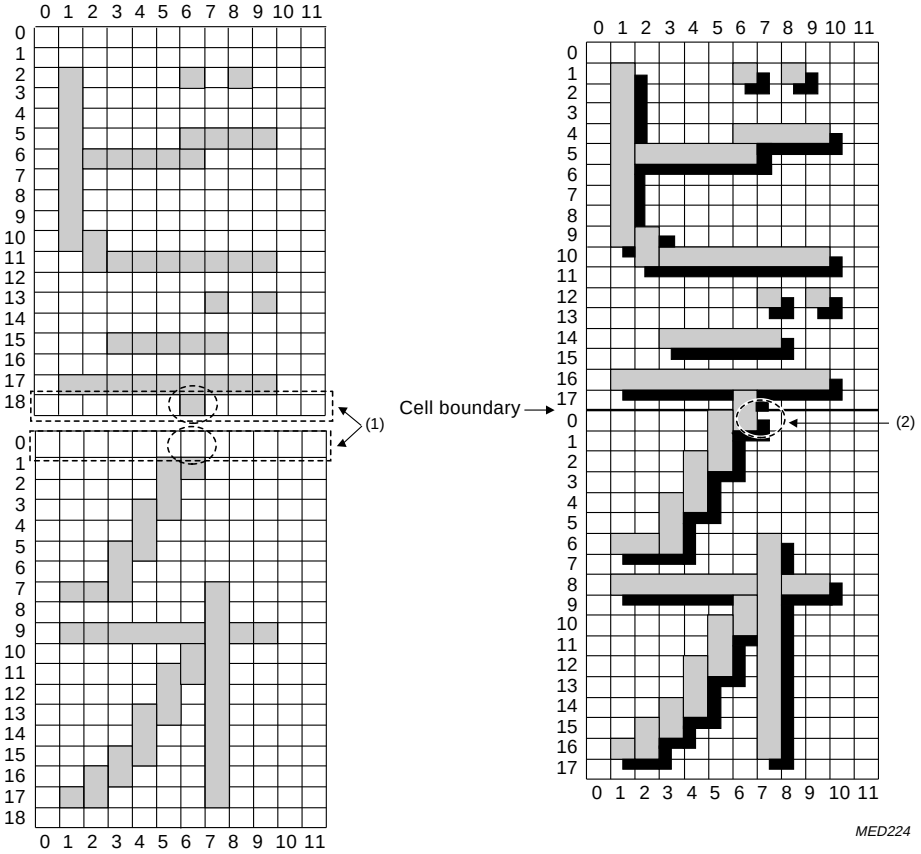


Fig.41 Combination of two character cells in horizontal direction to form a new font; with North-west shadowing.



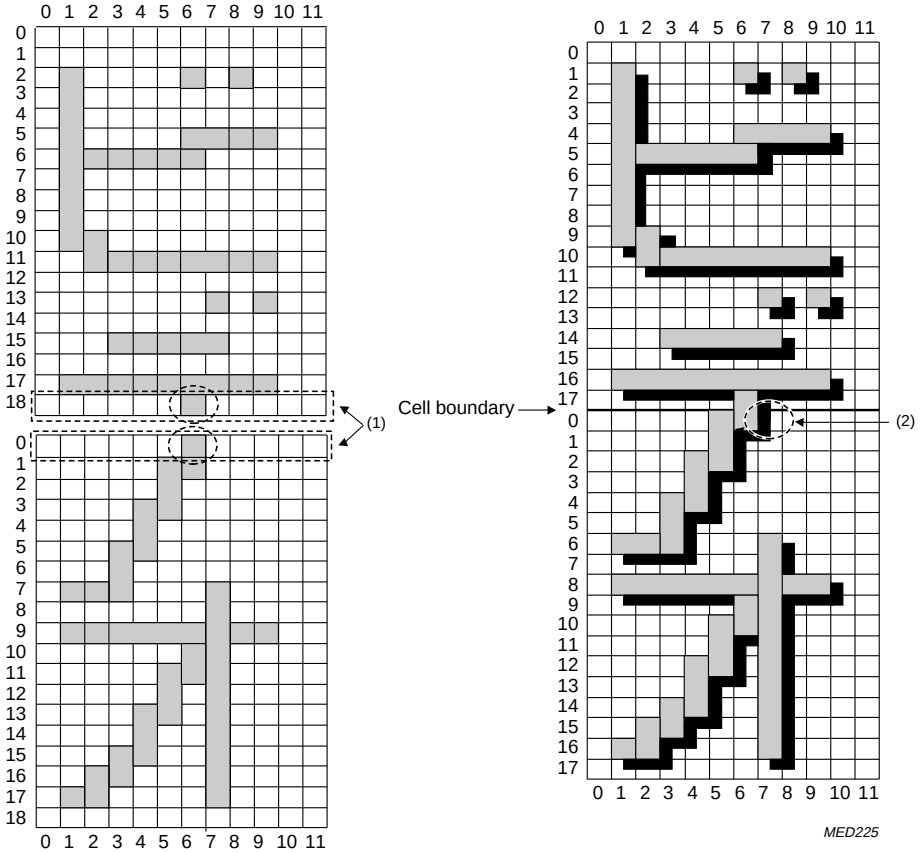
Character pattern stored in the ROM/RAM

Character pattern displayed on the screen

(1) The bit pattern of Row 18 of the upper character is not equal to that of Row 0 of the lower character.

(2) Due to the situation of (1), in the North-west shadowing mode a gap in the shadow might occur.

Fig.42 Combination of two characters in vertical direction to form a new pattern; contents Row 18 (upper cell) not equal to contents of Row 1(lower cell).



Character pattern stored in the ROM/RAM

Character pattern displayed on the screen

(1) The bit pattern of Row 18 of the upper character is equal to that of Row 0 of the lower character.

(2) Due to the situation of (1), in the North-west shadowing mode a gap in the shadow is avoided.

Fig.43 Combination of two characters in vertical direction to formulate a new pattern; contents Row 18 (upper cell) equal to contents of Row 1(lower cell).

14 OSD CLOCK IN DIFFERENT TV STANDARDS

14.1 Maximum number of characters per row

The number of characters per row is a function of the OSD clock frequency and the TV standard used.

The active video signal period of a horizontal line is 53.5 μs (see Fig.44). However, in order to reduce the jittering of the screen edge, overscan is normally applied by the TV manufacturer and this reduces the visible video signal period to $^{9}/_{10} \times 53.5$ μs = 48.15 μs.

The examples given below show how the number of characters per row and the character width may be obtained for the NTSC 525LPF/60 Hz TV standard using different OSD clock frequencies.

14.1.1 EXAMPLE 1

- For the OSD clock frequency f_{OSD} = 6 MHz; clock period = 0.166 μs. The number of visible dots on one horizontal line is 290 (48.15 μs/0.166 μs).
- Start of the first character dot is roughly 45 dots after $\overline{\text{HSYNC}}$ (see Section 9.2; command B, C, D). Therefore 290 − 45 = 245 dots are visible.
- Since each character is composed of 12 × 18 dots, the maximum characters displayed on a row is 20 (245/12).
- On a 19" TV screen, the width of a horizontal line is approximately 370 mm and this gives a character width of 18.5 mm (370 mm/20).

14.1.2 EXAMPLE 2

- For the OSD clock frequency f_{OSD} = 10 MHz; clock period = 0.1 μs. The number of visible dots on one horizontal line is 481 (48.15 μs/0.1 μs).
- Start of the first character dot is roughly 45 dots after $\overline{\text{HSYNC}}$ (see Section 9.2; command B, C, D). Therefore 481 − 45 = 436 dots are visible.
- Since each character is composed of 12 × 18 dots, the maximum characters displayed on a row is 36 (436/12).
- On a 19" TV screen, the width of a horizontal line is approximately 370 mm and this gives a character width of 10.3 mm (370 mm/36).

14.2 Maximum number of rows per frame

The number of rows per frame is a function of the number of active lines per display field and the number of vertical dots in the character matrix (which is 18).
The number of rows per frame (N) is calculated as shown below.

$$N = \frac{\text{number of active lines per field}}{18}$$

The three examples shown below illustrate how the maximum number of rows per frame is obtained for each TV scanning standard.

14.2.1 EXAMPLE 1; NTSC 525LPF/60 HZ

The number of active lines per field for this standard is between 241.5 and 249.5H (see Fig.45). If the value of 241 is used then the maximum number of rows per frame is 13.

14.2.2 EXAMPLE 2; PAL 625LPF/50 HZ

With this standard it is not necessary to divide $\overline{\text{HSYNC}}$ by two as both the horizontal and vertical frequency are doubled. The maximum number of rows per frame is 15.

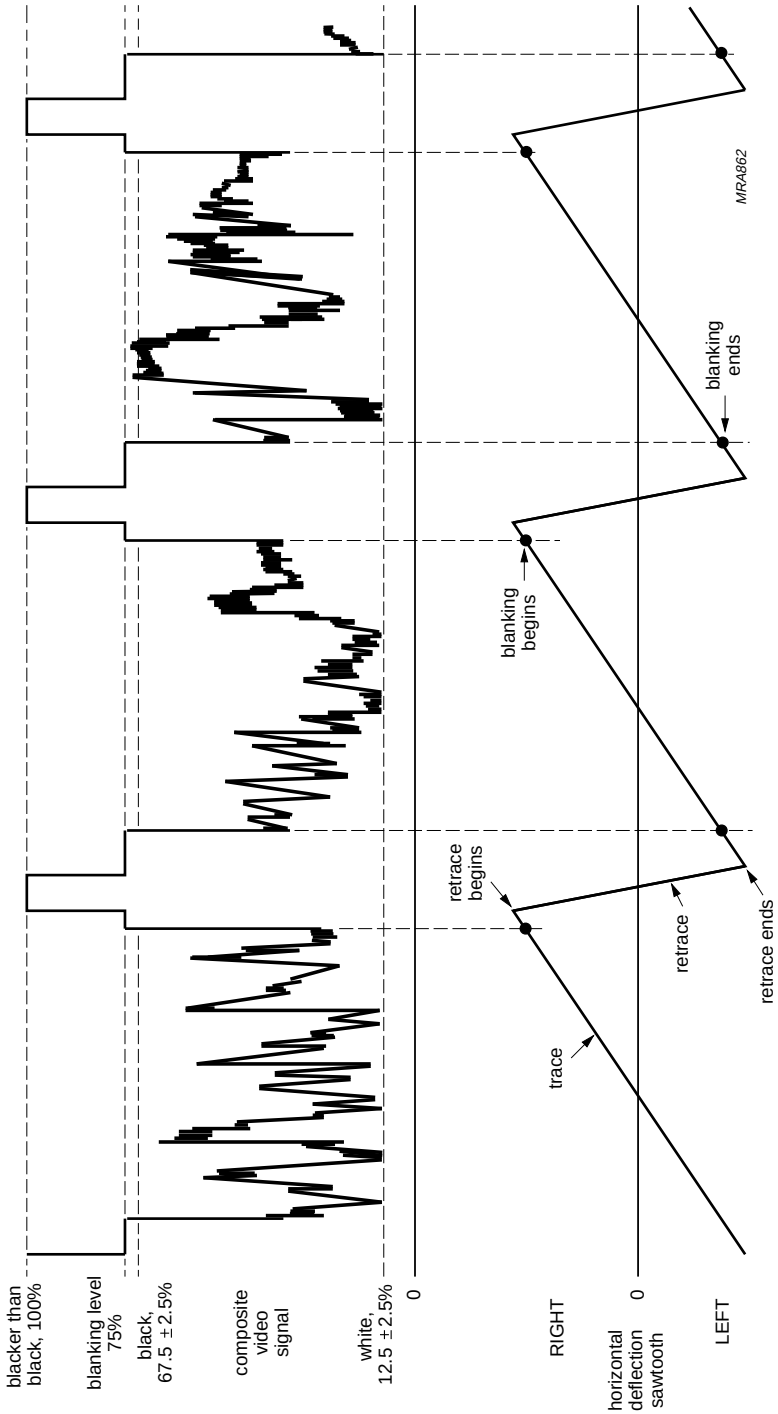


Fig.44 Composite video signal for three horizontal lines compared to three horizontal deflection sawteeth (NTSC 525LPF/60 Hz).

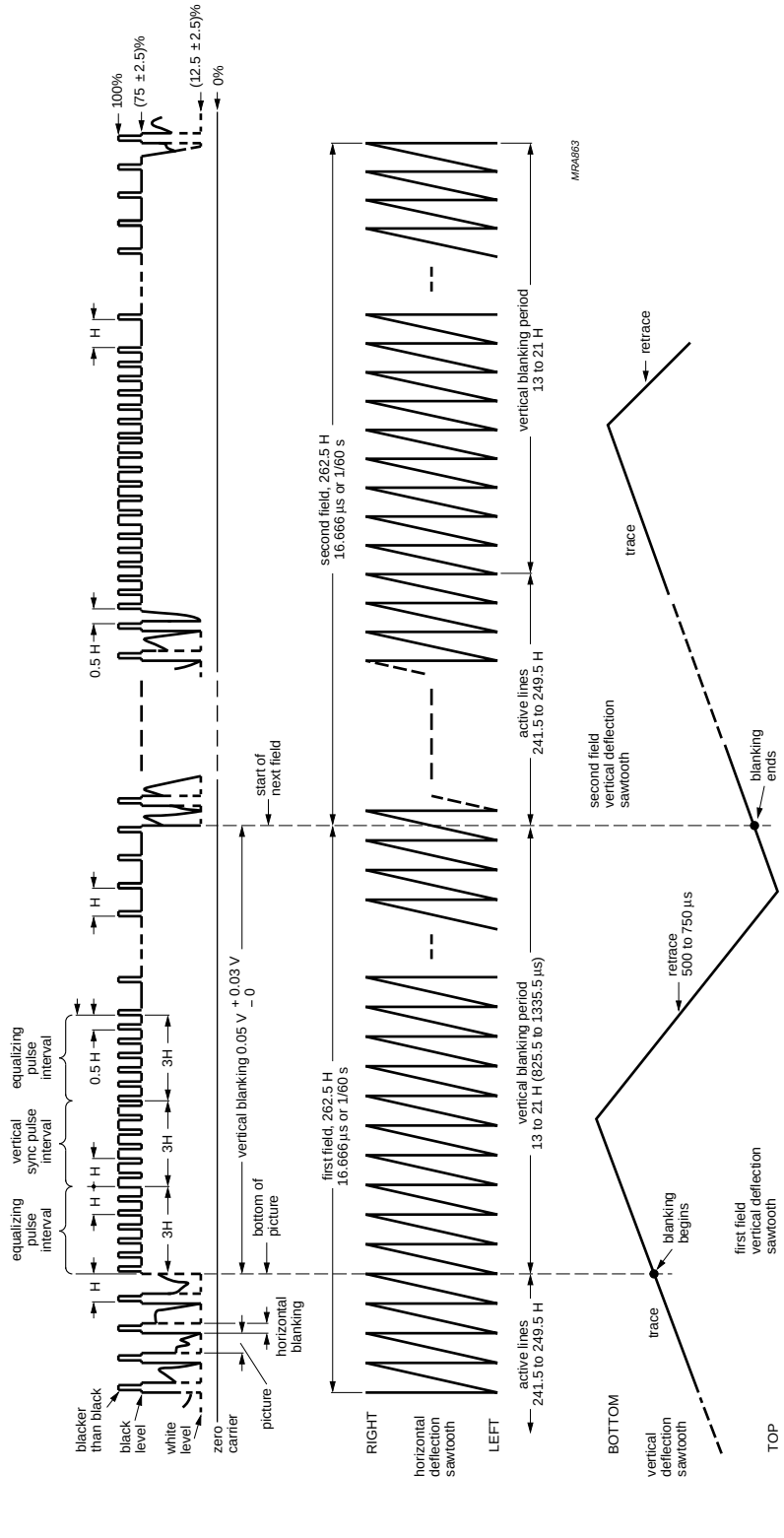


Fig.45 Vertical sync and blanking pulse intervals for one frame (NTSC 525LPF/60 Hz).

15 T3: 8-BIT COUNTER

Figure 46 shows the block diagram of the 8-bit counter. A Schmitt-trigger input pin shapes the slow slope of the input signal into a square wave. The rising edge of the signal increases the (ripple) counter by 1.

The data in the counter can be read by instruction 'MOV A, D24H' (Derivative Register 24). As soon as data is read, this counter is reset to **zero**. Overflow or Power-on-reset both reset the counter value to **zero**. Minimum distance between two successive pulses (rising edges) is 30 μs.

16 I²C-BUS MASTER SLAVE TRANSCEIVER

The I²C-bus master and slave transceiver is integrated. In control register CON1 (Derivative Register 22) bits SCLE and SDAE select the function of pins DP20/SDA and DP21/SCL (for selection see Table 23); SDA = I²C-bus data and SCL = clock line. Both pins are only available in port option 2 (see Fig.48).

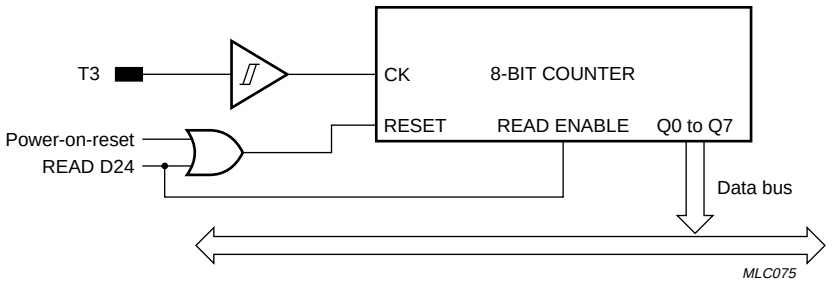


Fig.46 T3: 8-bit counter block diagram.

17 DERIVATIVE REGISTERS

Table 40 Register map PCA84C646/PCA84C846

Values within parenthesis show the bit state after a reset operation; 'X' denotes an undefined state.

ADDR (HEX)	REG	7	6	5	4	3	2	1	0	R/W
00	DP0R (Terminal)	DP07 (X)	DP06 (X)	DP05 (X)	DP04 (X)	DP03 (X)	DP02 (X)	DP01 (X)	DP00 (X)	R
01	DP1R (Terminal)	– (X)	– (X)	– (X)	– (X)	DP13 (X)	DP12 (X)	DP11 (X)	DP10 (X)	R
02	DP2R (Terminal)	– (X)	– (X)	– (X)	– (X)	DP23 (X)	DP22 (X)	DP21 (X)	DP20 (X)	R
03	DP0R (Latch)	DP07 (1)	DP06 (1)	DP05 (1)	DP04 (1)	DP03 (1)	DP02 (1)	DP01 (1)	DP00 (1)	RW
04	DP1R (Latch)	– (X)	– (X)	– (X)	– (X)	DP13 (1)	DP12 (1)	DP11 (1)	DP10 (1)	RW
05	DP2R (Latch)	– (X)	– (X)	– (X)	– (X)	DP23 (1)	DP22 (1)	DP21 (1)	DP20 (1)	RW
10	PWM0	– (X)	PWM06 (0)	PWM05 (0)	PWM04 (0)	PWM03 (0)	PWM02 (0)	PWM01 (0)	PWM00 (0)	RW
11	PWM1	– (X)	PWM16 (0)	PWM15 (0)	PWM14 (0)	PWM13 (0)	PWM12 (0)	PWM11 (0)	PWM10 (0)	RW
12	PWM2	– (X)	PWM26 (0)	PWM25 (0)	PWM24 (0)	PWM23 (0)	PWM22 (0)	PWM21 (0)	PWM20 (0)	RW
13	PWM3	– (X)	PWM36 (0)	PWM35 (0)	PWM34 (0)	PWM33 (0)	PWM32 (0)	PWM31 (0)	PWM30 (0)	RW
14	PWM4	– (X)	– (X)	PWM45 (0)	PWM44 (0)	PWM43 (0)	PWM42 (0)	PWM41 (0)	PWM40 (0)	RW
15	PWM5	– (X)	– (X)	PWM55 (0)	PWM54 (0)	PWM53 (0)	PWM52 (0)	PWM51 (0)	PWM50 (0)	RW
16	PWM6	– (X)	– (X)	PWM65 (0)	PWM64 (0)	PWM63 (0)	PWM62 (0)	PWM61 (0)	PWM60 (0)	RW
17	PWM7	– (X)	– (X)	PWM75 (0)	PWM74 (0)	PWM73 (0)	PWM72 (0)	PWM71 (0)	PWM70 (0)	RW
18	VSTL	– (X)	VST06 (0)	VST05 (0)	VST04 (0)	VST03 (0)	VST02 (0)	VST01 (0)	VST00 (0)	RW
19	VSTH	– (X)	VST13 (0)	VST12 (0)	VST11 (0)	VST10 (0)	VST09 (0)	VST08 (0)	VST07 (0)	RW
20	AFCCN	– (X)	AFCH1 (0)	AFCH0 (0)	AFCV3 (0)	AFCV2 (0)	AFCV1 (0)	AFCV0 (0)	AFCC[1] (X)	RW
21	PWME	PWM7E (0)	PWM6E (0)	PWM5E (0)	PWM4E (0)	PWM3E (0)	PWM2E (0)	PWM1E (0)	PWM0E (0)	RW
22	CON1	TDACE (0)	SCLE (0)	SDAE (0)	AFCE2 (0)	AFCE1 (0)	AFCE0 (0)	VOW1E (0)	VOW0E (0)	RW
23	CON2	VINT (0)	VIEN (0)	– (X)	– (X)	– (X)	P14LVL (0)	P7LVL (0)	P6LVL (0)	RW

ADDR (HEX)	REG	7	6	5	4	3	2	1	0	R/W
24	T3CON	T3B7 (0)	T3B6 (0)	T3B5 (0)	T3B4 (0)	T3B3 (0)	T3B2 (0)	T3B1 (0)	T3B0 (0)	R
25	PLLCN	– (X)	PLL6 (0)	PLL5 (0)	PLL4 (0)	PLL3 (0)	PLL2 (0)	PLL1 (0)	PLL0 (0)	RW
30	DCRAR	– (X)	– (X)	DCRA5 (0)	DCRA4 (0)	DCRA3 (0)	DCRA2 (0)	DCRA1 (0)	DCRA0 (0)	RW
31	DCRTR	– (X)	– (X)	– (X)	– (X)	DCRT3 (1)	DCRT2 (1)	DCRT1 (1)	DCRT0 (1)	W
32	DCRCR	– (X)	– (X)	DCRC5 (1)	DCRC4 (1)	DCRC3 (1)	DCRC2 (1)	DCRC1 (1)	DCRC0 (1)	W
33	CON3	– (X)	– (X)	– (X)	– (X)	BR1 (0)	BR0 (0)	BF1 (1)	BF0 (1)	RW
34	CON4	– (X)	– (X)	S1 (0)	S0 (0)	Hp (0)	Vp (0)	Bp (1)	EN (0)	RW
35	VPOS	– (X)	– (X)	V5 (1)	V4 (1)	V3 (1)	V2 (1)	V1 (1)	V0 (1)	W
36	HPOS	– (X)	– (X)	H5 (0)	H4 (0)	H3 (0)	H2 (0)	H1 (0)	H0 (0)	W
37	BCC	– (X)	– (X)	– (X)	– (X)	– (X)	BCR (0)	BCG (0)	BCB (1)	W

Note

1. This bit is Read only.

18 INPUT/OUTPUT

There are 3 different port options available for the port pins in the 84CXXX derivatives (see Figs 47, 48 and 49).

Each I/O port line may be individually configured using one of three mask options. The three I/O mask options are specified below:

Option 1 Standard input/output with switched pull-up current source; this is shown in Fig.47.

Option 1 Input/output with Open drain output; this is shown in Fig.48.

Option 2 Push-pull output; this is shown in Fig.49.

The state of each output port after a Power-on-reset can also be selected using the mask options. All port mask options are given in Section 19.1.

The output stage consists of 4 transistors:

TR1: N - channel transistor for ‘sink’

TR2: P - channel transistor for ‘boost-up’

TR3: P - channel transistor for ‘pull-up’

TR4: P - channel transistor for ‘constant current’.

See Tables 41 and 42 for possible port option list.

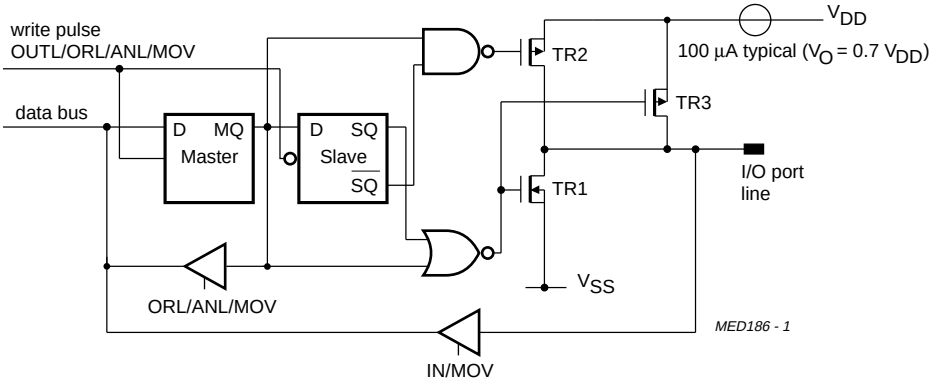


Fig.47 Standard output with switched pull-up current source (Option 1).

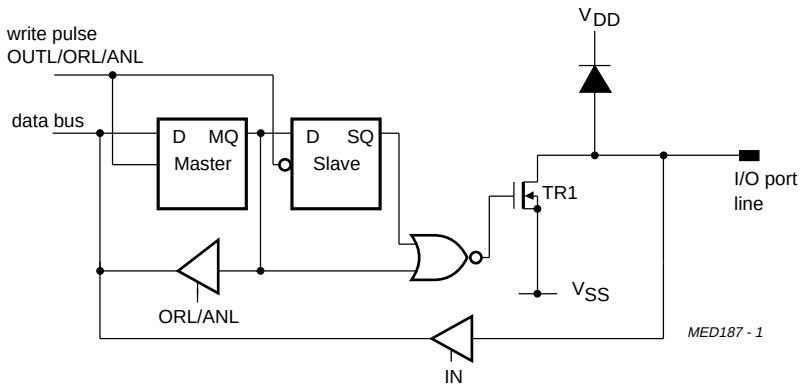


Fig.48 Open drain output (Option 2).

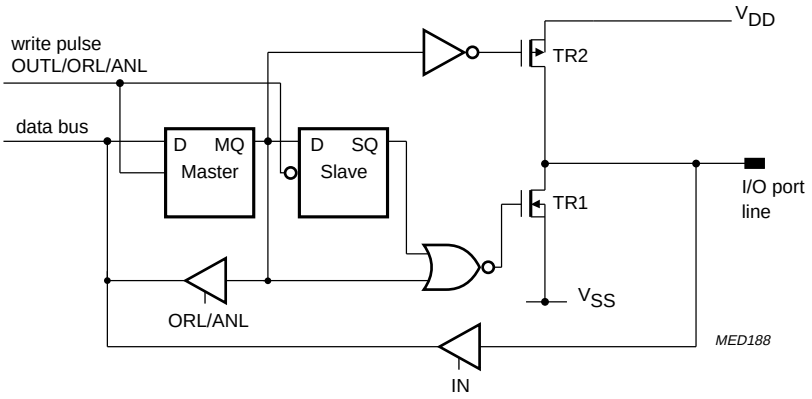


Fig.49 Push-pull output (Option 3).

19 OPTION LISTS

19.1 Port option

For the port options (1, 2 and 3) see Figs 47, 48 and 49.

Table 41 Port options for making piggyback

Only the port pins whose options are left blank, e.g. DP00, can be user mask programmable.

PORT	PIN	OPTION		PORT/DPORT	PIN	OPTION		DPORT	PIN	OPTION		DPORT	PIN	OPTION	
P00	13	1	S[1]	P10	7	1	S	DP00	29			DP20	40	2	S
P01	14	1	S	P11	8	1	S	DP01	28			DP21	39	2	S
P02	15	1	S	P12	10	1	S	DP02	27			DP22	3		
P03	16	1	S	P14	12	1	S	DP03	26			DP23	4		
P04	17	1	S	DP10	38			DP04	25						
P05	18	1	S	DP11	37			DP05	24						
P06	19	1	S	DP12	36			DP06	23			VOB[2]	1		
P07	20	1	S	DP13	9			DP07	22			VOW2[2]	2		

Notes

1. S = SET (and R = RESET), initial H or L after power-on reset.
2. Option 2 or 3 only (i.e. output only).

Table 42 Port options for production

Only the port pins whose options are left blank, e.g. DP00, can be user mask programmable.

PORT	PIN	OPTION		PORT/DPORT	PIN	OPTION		DPORT	PIN	OPTION		DPORT	PIN	OPTION	
P00	13			P10	7			DP00	29			DP20	40	2	S[1]
P01	14			P11	8			DP01	28			DP21	39	2	S
P02	15			P12	10			DP02	27			DP22	3		
P03	16			P14	12			DP03	26			DP23	4		
P04	17			DP10	38			DP04	25						
P05	18			DP11	37			DP05	24						
P06	19			DP12	36			DP06	23			VOB[2]	1		
P07	20			DP13	9			DP07	22			VOW2[2]	2		

Notes

1. S = SET (and R = RESET), initial H or L after power-on reset.
2. Option 2 or 3 only (i.e. output only).

19.2 On-chip oscillator transconductance

OPTION	typ. g_m at 5 V	f_{osc} FOR QUARTZ	f_{osc} FOR PXE
LOW (g_{mL})	0.4 mS	1 to 6 MHz	not allowed
MEDIUM (g_{mM})	1.6 mS	4 to 10 MHz	1 to 6 MHz
HIGH (g_{mH})	4.5 mS	not allowed	3 to 10 MHz

20 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.3	+7	V
V_I	all input voltages	–0.3	V_{DD} + 0.3	V
P_{tot}	total power dissipation	–	1	W
I_{OH}	maximum source current for all port lines	–	–10	mA
I_{OL}	maximum sink current for all port lines	–	30	mA
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	ambient operating temperature	–20	+70	°C

21 DC CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = –20 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		4.5	5.0	5.5	V
I_{DD}	operating supply current	$f_{OSD(RC)}$, $f_{OSD(LC)}$ = f_{xtal}				
		f_{xtal} = 10 MHz	–	5	10	mA
		f_{xtal} = 6 MHz	–	3.5	7	mA
		$f_{OSD(RC)}$, $f_{OSD(LC)}$ = stop				
		f_{xtal} = 10 MHz	–	3	6	mA
		f_{xtal} = 6 MHz	–	1.5	4	mA
Input Ports P00, P01, DP00, DP01 and DP02						
V_{IL}	LOW level input voltage	V_{DD} = 4.5 V to 5.5 V	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	V_{DD} = 4.5 V to 5.5 V	$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	V_{DD} = 4.5 V to 5.5 V; $V_{SS} < V_I < V_{DD}$	–	–	±10	µA
Output Port P00						
V_{OL}	LOW level output voltage	I_{OL} = 10 mA	–	–	1.2	V
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–3.0	–7.0	–	mA
DP00/PWM00 to DP07/PWM07 as derivative Port						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	5.0	12.0	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–3.0	–7.0	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DP00/PWM00 to DP07/PWM07 as PWM output Port						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	0.7	1.5	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–0.7	–1.5	–	mA
Port P10 to P13 outputs						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	5.0	12.0	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–3.0	–7.0	–	mA
Outputs VOB and VOW2						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	1.4	3.0	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–1.4	–3	–	mA
DP10/AFC0, DP11/AFC1 and DP12/AFC2 as derivative output Port						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	5.0	12.0	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–3.0	–7.0	–	mA
DP20/SDA and DP21/SCL outputs						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	3.0	–	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–	–7.0	–	mA
DP22/VOW1, DP23/VOW0 and DP13/TDAC as derivative output Port						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	5.0	12.0	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–3.0	–7.0	–	mA
DP22/VOW1 and DP23/VOW0 as VOWi output						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	1.4	3.0	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} – 0.4$ V	–1.4	–3.0	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DP13/TDAC as TDAC output						
I_{OL}	LOW level output sink current	V_{OL} = 0.4 V	1.4	3.0	–	mA
I_{OH}	HIGH level pull-up output source current	$V_O = 0.7V_{DD}$	–40	–100	–	µA
	HIGH level pull-up output source current	$V_O = V_{SS}$	–	–140	–400	µA
	HIGH level push-pull output source current	$V_O = V_{DD} - 0.4$ V	–1.4	–3.0	–	mA
EMU/TEST, $\overline{\text{RESET}}$, $\overline{\text{INT}}$/T0, T1, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ and T3 (Schmitt-trigger input)						
V_{IL}	LOW level input voltage	V_{DD} = 4.5 V to 5.5 V	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	V_{DD} = 4.5 V to 5.5 V	$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	V_{DD} = 4.5 V to 5.5 V; $V_{SS} < V_I < V_{DD}$	–1.0	–	+1.0	µA

22 AC CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = –20 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
f_{xtal}	crystal frequency (note 1)		1	–	10.0	MHz
$f_{osc\text{-}XTAL}$	oscillator frequency; option 1	g_m = 0.4 mS (typ.)	1	–	6.0	MHz
$f_{osc\text{-}PXE}$			not allowed			MHz
$f_{osc\text{-}XTAL}$	oscillator frequency; option 2	g_m = 1.6 mS (typ.)	4.0	–	10.0	MHz
$f_{osc\text{-}PXE}$			1.0	–	6.0	MHz
$f_{osc\text{-}XTAL}$	oscillator frequency; option 3	g_m = 4.5 mS (typ.)	not allowed			MHz
$f_{osc\text{-}PXE}$			3.0	–	10.0	MHz
C_{XTAL1}	external capacitance at XTAL1					
	with XTAL resonator		not required			pF
	with PXE resonator		–	30	100	pF
C_{XTAL2}	external capacitance at XTAL2					
	with XTAL resonator		not required			pF
	with PXE resonator		–	30	100	pF
f_{OSD}	OSD clock frequency		4.0	8.0	12.0	MHz

Note

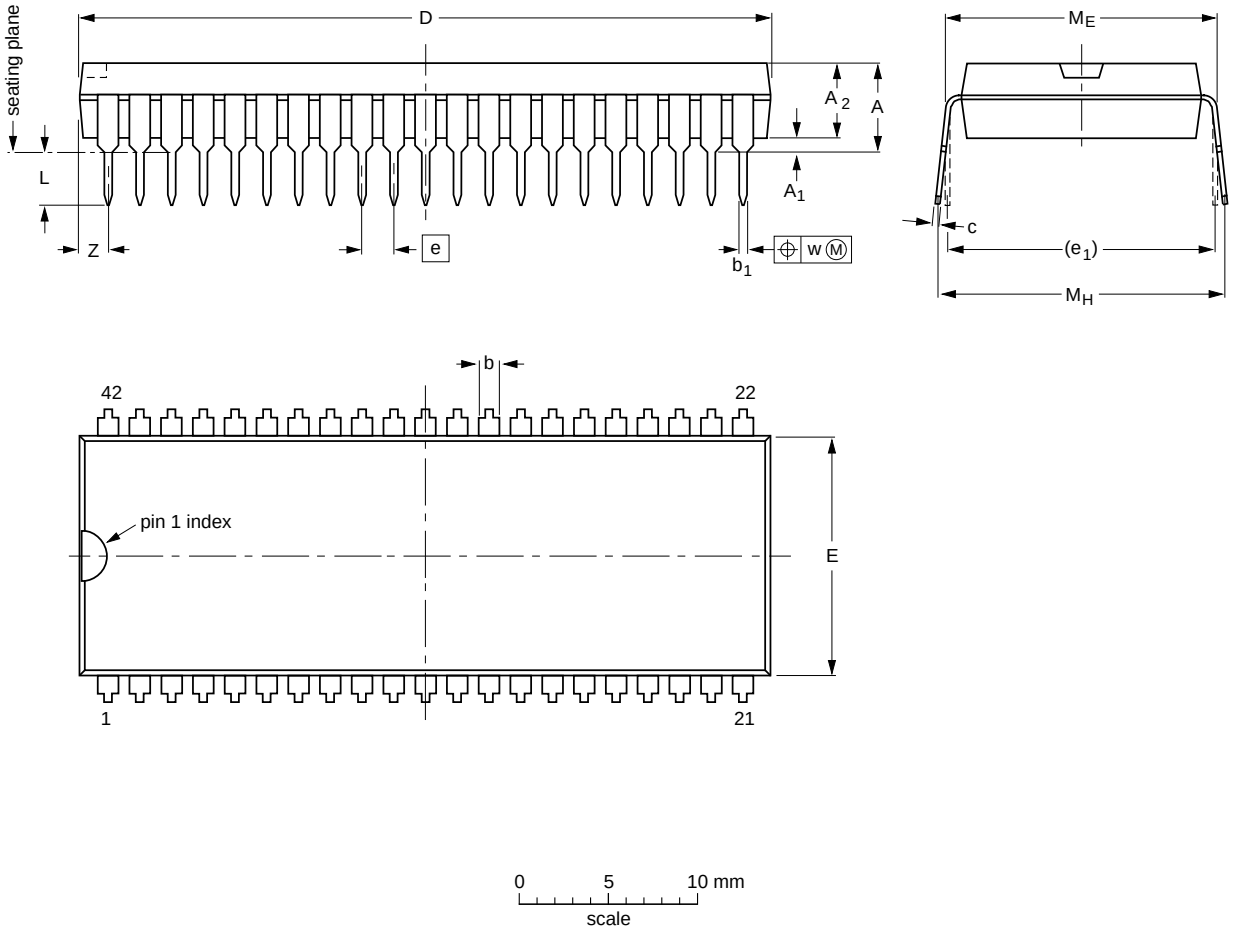
1. Oscillator with three (3) options for optimum use.

23 AFC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_{AFC}	conversion time (from any change in the AFC: channel number, voltage level, enable/disable) with f_{xtal} = 10 MHz	–	–	7	µs
DP10/AFC0, DP11/AFC1 and DP12/AFC2 comparator input					
V_{AI}	comparator analog input voltage	V_{SS}	–	V_{DD}	V
V_{AE}	conversion error range	–	–	±0.5	LSB

24 PACKAGE OUTLINE

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

25 SOLDERING

25.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

25.2 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

25.3 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

26 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

27 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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Printed in The Netherlands

453061/1500/03/pp72 Date of release: 1995 Jun 15

Document order number: 9397 750 00166

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