PRELIMINARY

MX29F1615

16M-BIT [2M x8/1M x16] CMOS SINGLE VOLTAGE FLASH EEPROM

FEATURES

- 5V ± 10% write and erase
- JEDEC-standard EEPROM commands
- Endurance:100 cycles
- Fast access time: 90/100/120ns
- Auto Erase and Auto Program Algorithms
  - Automatically erases the whole chip
  - Automatically programs and verifies data at specified addresses
- Status Register feature for detection of program or erase cycle completion
- Low VCC write inhibit is equal to or less than 3.2V
- Software and hardware data protection
- Page program operation
  - Internal address and data latches for 64 words per page
  - Page programming time: 0.9ms typical
- Low power dissipation
  - 30mA typical active current
  - 1uA typical standby current
- CMOS and TTL compatible inputs and outputs
- Package Type:
  - 42 lead PDIP

GENERAL DESCRIPTION

The MX29F1615 is a 16-mega bit Flash memory organized as either 1M wordx16 or 2M bytex8. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F1615 is packaged in 42-pin PDIP. It is designed to be reprogrammed and in standard EPROM programmers.

The standard MX29F1615 offers access times as fast as 90ns,allowing operation of high-speed microprocessors without wait. To eliminate bus contention, the MX29F1615 has separate chip enables($\overline{CE}$) and output enable ($\overline{OE}$) control.

MXIC's Flash memories augment EPROM functionality with electrical erasure and programming. The MX29F1615 uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

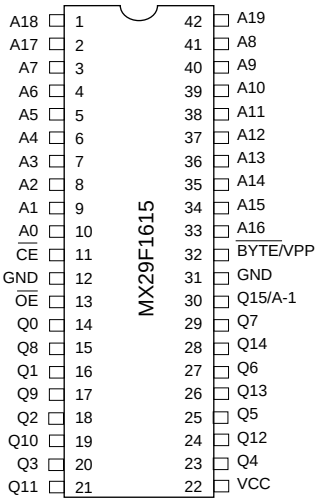
To allow for simple in-system reprogrammability, the MX29F1615 requires high input voltages (10V) on BYTE/VPP pin for programming. Reading data out of the device is similar to reading from an EPROM.

MXIC Flash technology reliably stores memory contents even after 100 cycles. The MXIC's cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F1615 uses a 5V ± 10% VCC supply to perform the Auto Erase and Auto Program algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC +1V.

PIN CONFIGURATIONS

42 PDIP(600mil)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0 - A19	Address Input
Q0 - Q14	Data Input/Output
Q15/A - 1	Q15(Word mode)/LSB addr.(Byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$/VPP	Word/Byte Selection Input/Write Enable Input
VCC	Power Supply
GND	Ground Pin

BLOCK DIAGRAM

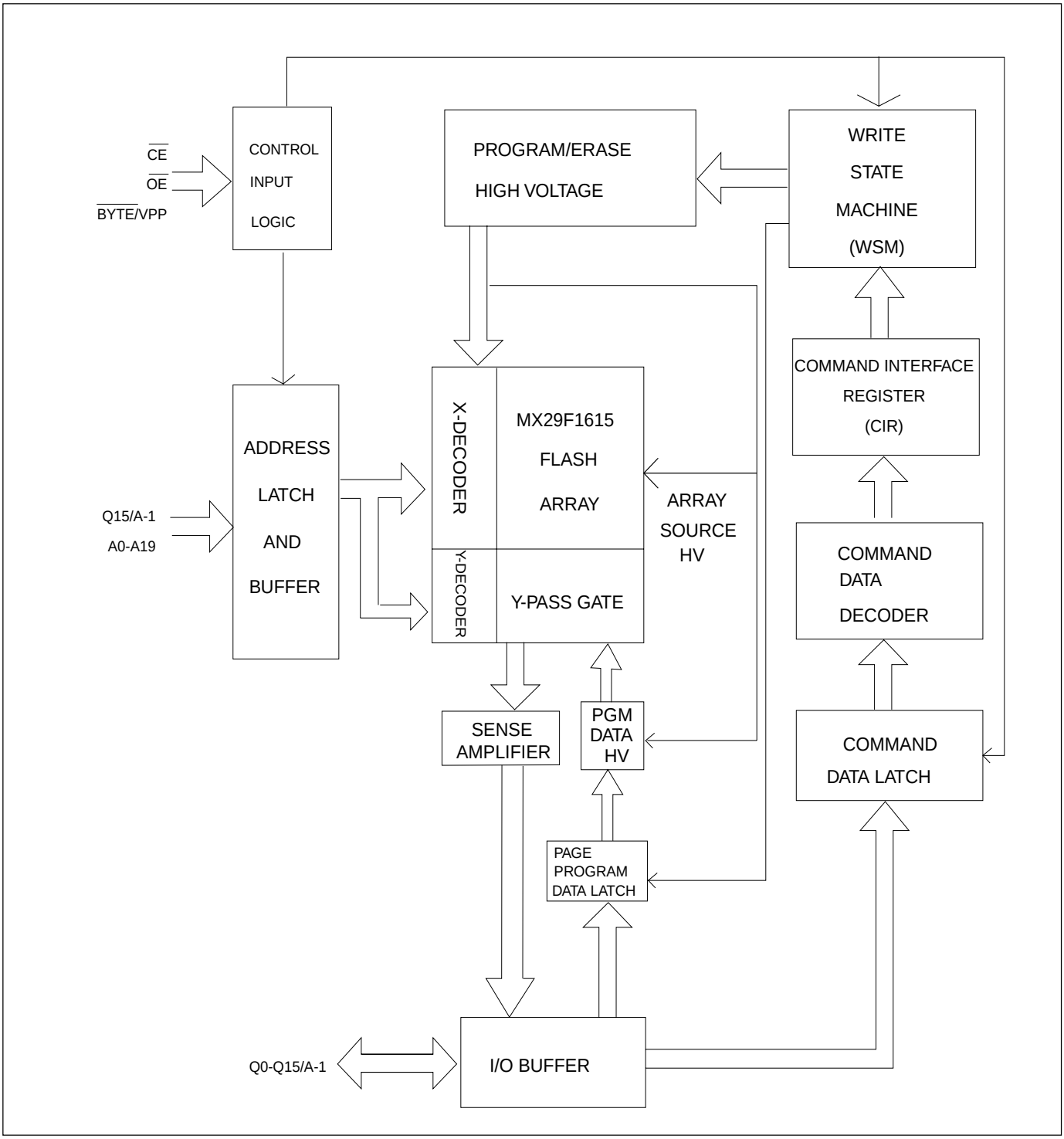


Table1.PIN DESCRIPTIONS

SYMBOL	TYPE	NAME AND FUNCTION
A0 - A19	INPUT	ADDRESS INPUTS: for memory addresses. Addresses are internally latched during a write cycle.
Q0 - Q7	INPUT/OUTPUT	LOW-BYTE DATA BUS: Input data and commands during Command Interface Register(CIR) write cycles. Outputs array,status and identifier data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled.
Q8 - Q14	INPUT/OUTPUT	HIGH-BYTE DATA BUS: Inputs data during x 16 Data-Write operations. Outputs array, identifier data in the appropriate read mode; not used for status register reads. Floated when the chip is de-selected or the outputs are disabled
Q15/A -1	INPUT/OUTPUT	Selects between high-byte data INPUT/OUTPUT($\overline{BYTE}$/VPP = HIGH) and LSB ADDRESS($\overline{BYTE}$/VPP = LOW) for read operation.
$\overline{CE}$	INPUT	CHIP ENABLE INPUTS: Activate the device's control logic, Input buffers, decoders and sense amplifiers. With $\overline{CE}$ high, the device is de-selected and power consumption reduces to Standby level upon completion of any current program or erase operations. $\overline{CE}$ must be low to select the device. Device selection occurs with the latter falling edge of $\overline{CE}$. The first rising edge of $\overline{CE}$ disables the device.
$\overline{OE}$	INPUT	OUTPUT ENABLES: Gates the device's data through the output buffers during a read cycle OE is active low.
$\overline{BYTE}$/VPP	INPUT	BYTE ENABLE: While operating read mode, $\overline{BYTE}$/VPP Low places device in x8 mode. All data is then input or output on Q0-7 and Q8-14 float. AddressQ15/A-1 selects between the high and low byte. While operating read mode, $\overline{BYTE}$/VPP high places the device in x16 mode, and turns off the Q15/A-1 input buffer. Address A0, then becomes the lowest order address. Write Enable is active while apply 10V on the $\overline{BYTE}$/VPP pin.
VCC		DEVICE POWER SUPPLY(5V±10%)
GND		GROUND

BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU . All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Table2.1 Bus Operations

Mode	Notes	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$/VPP	A0	A1	A9	Q0-Q7	Q8-Q14	Q15/A-1
Read	1,5	VIL	VIL	VIH/VIL	X	X	X	DOUT	HighZ/DOUT	VIL/VIH/DOUT
Output Disable	1	VIL	VIH	VIH/VIL	X	X	X	HighZ	HIghZ	HighZ/X
Standby	1	VIH	X	X	X	X	X	X	X	X
Manufacturer ID	2,4	VIL	VIL	VIH/VIL	VIL	VIL	VID	C2H	High Z/00H	VIL/OB
Device ID MX29F1615	2,4	VIL	VIL	VIH/VIL	VIH	VIL	VID	6BH	High Z/00H	VIL/OB
Write	1,3,6	VIL	VIH	VHH	X	X	X	DIN	DIN	DIN

NOTES :

1. X can be VIH or VIL for address or control pins.
2. A0 and A1 at VIL provide manufacturer ID codes. A0 at VIH and A1 at VIL provide device ID codes.
3. Commands for different Erase operations or Data program operations can only be successfully completed through proper command sequence.
4. VID = 11.5V- 12.5V.
5. Q15/A-1 = VIL, Q0 - Q7 =D0-D7 out . Q15/A-1 = VIH, Q0 - Q7 = D8 -D15 out.
6. VHH=9.5V~10.5V

WRITE OPERATIONS

Commands are written to the COMMAND INTERFACE REGISTER (CIR) using standard microprocessor write timings. The CIR serves as the interface between the microprocessor and the internal chip operation. The CIR can decipher Read Array, Read Silicon ID, Erase and Program command. In the event of a read command, the CIR simply points the read path at either the array or the silicon ID, depending on the specific read command given. For a program or erase cycle, the CIR informs the write state machine that a program or erase has been requested. During a program cycle, the write state machine will control the program sequences and the CIR will only respond to status reads. During a sector/chip erase cycle, the CIR will respond to status reads and erase suspend. After the write state machine has completed its task, it will allow the CIR to respond to its full command set. The CIR stays at read status register mode until the microprocessor issues another valid command sequence.

Device operations are selected by writing commands into the CIR. Table 3 below defines 16 Mbit flash command.

TABLE 3. COMMAND DEFINITIONS(Word-Wide Mode, $\overline{BYTE}$/VPP=VHH)

Command Sequence		Read/ Reset	Silicon ID Read	Page Program	Chip Erase	Read Status Reg.	Clear Status Reg.
Bus Write Cycles Req'd		4	4	4	6	4	3
First Bus	Addr	5555H	5555H	5555H	5555H	5555H	5555H
Write Cycle	Data	AAH	AAH	AAH	AAH	AAH	AAH
Second Bus	Addr	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH
Write Cycle	Data	55H	55H	55H	55H	55H	55H
Third Bus	Addr	5555H	5555H	5555H	5555H	5555H	5555H
Write Cycle	Data	F0H	90H	A0H	80H	70H	50H
Fourth Bus	Addr	RA	00H/01H	PA	5555H	X	
Read/Write Cycle	Data	RD	C2H/6BH	PD	AAH	SRD	
Fifth Bus	Addr				2AAAH		
Write Cycle	Data				55H		
Sixth Bus	Addr				5555H		
Write Cycle	Data				10H		

Notes:

1. Address bit A15 -- A19 = X = Don't care for all address commands except for Program Address(PA).
   5555H and 2AAAH address command codes stand for Hex number starting from A0 to A14.
2. Bus operations are defined in Table 2.
3. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{CE}$ pulse.
4. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{CE}$.
   SRD = Data read from status register.
5. Only Q0-Q7 command data is taken, Q8-Q15 = Don't care.

DEVICE OPERATION

SILICON ID READ

The Silicon ID Read mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force VID (11.5V~12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from VIL to VIH. All addresses are don't cares except A0 and A1.

The manufacturer and device codes may also be read via the command register, for instances when the MX29F1615 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 3.

Byte 0 (A0=VIL) represents the manfacturer's code (MXIC=C2H) and byte 1 (A0=VIH) the device identifier code (MX29F1615=6BH).

The Silicon ID Read mode will be terminated after the following write command cycle.

Table 4. MX29F1615 Silion ID Codes

Type	A_{19}	A_{18}	A_{17}	A_{16}	A_1	A_0	Code(HEX)	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Manufacturer Code	X	X	X	X	VIL	VIL	C2H*	1	1	0	0	0	0	1	0
MX29F1615 Device Code	X	X	X	X	VIL	VIH	6BH	0	1	1	0	1	0	1	1

* MX29F1615 Manufacturer Code = C2H, Device Code = 6BH when $\overline{BYTE}$/VPP = VIL
MX29F1615 Manufacturer Code = 00C2H, Device Code = 006BH when $\overline{BYTE}$/VPP= VIH

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/ reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the CIR contents are altered by a valid command sequence.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

The MX29F1615 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{BYTE}$/VPP is high or low the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

Note that the read/reset command is not valid when program or erase is in progress.

PAGE PROGRAM

To initiate Page program mode, a three-cycle command sequence is required. There are two " unlock" write cycles. These are followed by writing the page program command-A0H.

Any attempt to write to the device without the three-cycle command sequence will not start the internal Write State Machine(WSM), no data will be written to the device.

After three-cycle command sequence is given, a word load is performed by applying a low pulse on the $\overline{CE}$ input with $\overline{CE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$. Maximum of 64 words of data may be loaded into each page by the same procedure as outlined in the page program section below.

PROGRAM

Any page to be programmed should have the page in the erased state first, i.e. performing sector erase is suggested before page programming can be performed.

The device is programmed on a page basis. If a word of data within a page is to be changed, data for the entire page can be loaded into the device. Any word that is not loaded during the programming of its page will be still in the erased state (i.e. FFH). Once the words of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data word has been loaded into the device, successive words are entered in the same manner. The time between word loads must be less than 30us otherwise the load period could be teminated. A6 to A19 specify the page address, i.e., the device is page-aligned on 64 words boundary. The page address must be valid during each high to low transition of $\overline{CE}$. A0 to A5 specify the byte address within the page. The word may be loaded in any order; sequential loading is not required. If a high to low transition of $\overline{CE}$ is not detected whithin 100us of the last low to high transition, the load period will end and the internal programming period will start. The Auto page program terminates when status on Q7 is '1' at which time the device stays at read status register mode until the CIR contents are altered by a valid command sequence.

CHIP ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command-80H. Two more "unlock" write cycles are then followed by the chip erase command-10H.

Chip erase does not require the user to program the device prior to erase.

The automatic erase begins on the rising edge of the last $\overline{CE}$ pulse in the command sequence and terminates when the status on Q7 is "1" at which time the device stays at read status register mode. The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence.

READ STATUS REGISTER

The MXIC's16 Mbit flash family contains a status register which may be read to determine when a program or erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status command to the CIR. After writing this command, all subsequent read operations output data from the status register until another valid command sequence is written to the CIR. A Read Array command must be written to the CIR to return to the Read Array mode.

The status register bits are output on Q2 - Q7(table 6) whether the device is in the byte-wide (x8) or word-wide (x16) mode for the MX29F1615. In the word-wide mode the upper byte, Q(8:15) is set to 00H during a Read Status command. In the byte-wide mode, Q(8:14) are tri-stated and Q15/A-1 retains the low order address function. Q0-Q1 is set to 0H in either x8 or x16 mode.

It should be noted that the contents of the status register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$ whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the status register change while reading the status register. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the completion of a program or erase operation will not be evident.

The Status Register is the interface between the microprocessor and the Write State Machine (WSM). When the WSM is active, this register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation. The WSM sets status bits four through seven and clears bits six and seven, but cannot clear status bits four and five. If Erase fail or Program fail status bit is detected, the Status Register is not cleared until the Clear Status Register command is written. The MX29F1615 automatically outputs Status Register data when read after Chip Erase, Page Program or Read Status Command write cycle. The internal state machine is set for reading array data upon device power-up, or after deep power-down mode.

CLEAR STATUS REGISTER

The Eraes fail status bit (Q5) and Program fail status bit (Q4) are set by the write state machine, and can only be reset by the system software. These bits can indicate various failure conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several pages or erasing multiple blocks in squence). The status register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. Additionally, once the program(erase) fail bit happens, the program (erase) operation can not be performed further. The program(erase) fail bit must be reset by system software before further page program or sector (chip) erase are attempted. To clear the status register, the Clear Status Register command is written to the CIR. Then, any other command may be issued to the CIR. Note again that before a read cycle can be initiated, a Read command must be written to the CIR to specify whether the read data is to come from the Array, Status Register or Silicon ID.

TABLE 5. MX29F1615 STATUS REGISTER

	STATUS	NOTES	Q7	Q6	Q5	Q4	Q3
IN PROGRESS	PROGRAM	1, 2	0	0	0	0	0
	ERASE	1, 3	0	0	0	0	0
COMPLETE	PROGRAM	1, 2	1	0	0	0	0
	ERASE	1, 3	1	0	0	0	0
FAIL	PROGRAM	1, 4	1	0	0	1	0
	ERASE	1, 4	1	0	1	0	0
AFTER CLEARING STATUS REGISTER			1	0	0	0	0

NOTES:

1. Q7 : WRITE STATE MACHINE STATUS
   1 = READY, 0 = BUSY
   Q6 : RESERVED FOR FUTURE ENHANCEMENTS
   Q5 : ERASE FAIL STATUS
   1 = FAIL IN ERASE, 0 = SUCCESSFUL ERASE
   Q4 : PROGRAM FAIL STATUS
   1 = FAIL IN PROGRAM, 0 = SUCCESSFUL PROGRAM
   Q3=0 = RESERVED FOR FUTURE ENHANCEMENTS.
   Other bits are reserved for future use ; mask them out when polling the Status Register.
2. PROGRAM STATUS is for the status during Page Programming.
3. ERASE STATUS is for the status during Chip Erase.
4. FAIL STATUS bit(Q4 or Q5) is provided during Page Program or Chip Erase modes respectively.
5. Q3 = 0 all the time.

DATA PROTECTION

The MX29F1615 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read Array mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transitions or system noise.

LOW VCC WRITE INHIBIT

To avoid initiation of a write cycle during VCC power-up and power-down, a write cycle is locked out for VCC less than VLKO(= 3.2V , typically 3.5V). If VCC < VLKO, the command register is disabled and all internal program/ erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the VCC level is greater than VLKO. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional write when VCC is above VLKO.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 10ns (typical) on $\overline{CE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL,$\overline{CE}$ = VIH or $\overline{BYTE}$/VPP=VIH/VIL To initiate a write cycle $\overline{CE}$ must be a logical zero, $\overline{BYTE}$/VPP must be at VHH while $\overline{OE}$ is a logical one.

Figure 1. AUTOMATIC PAGE PROGRAM FLOW CHART

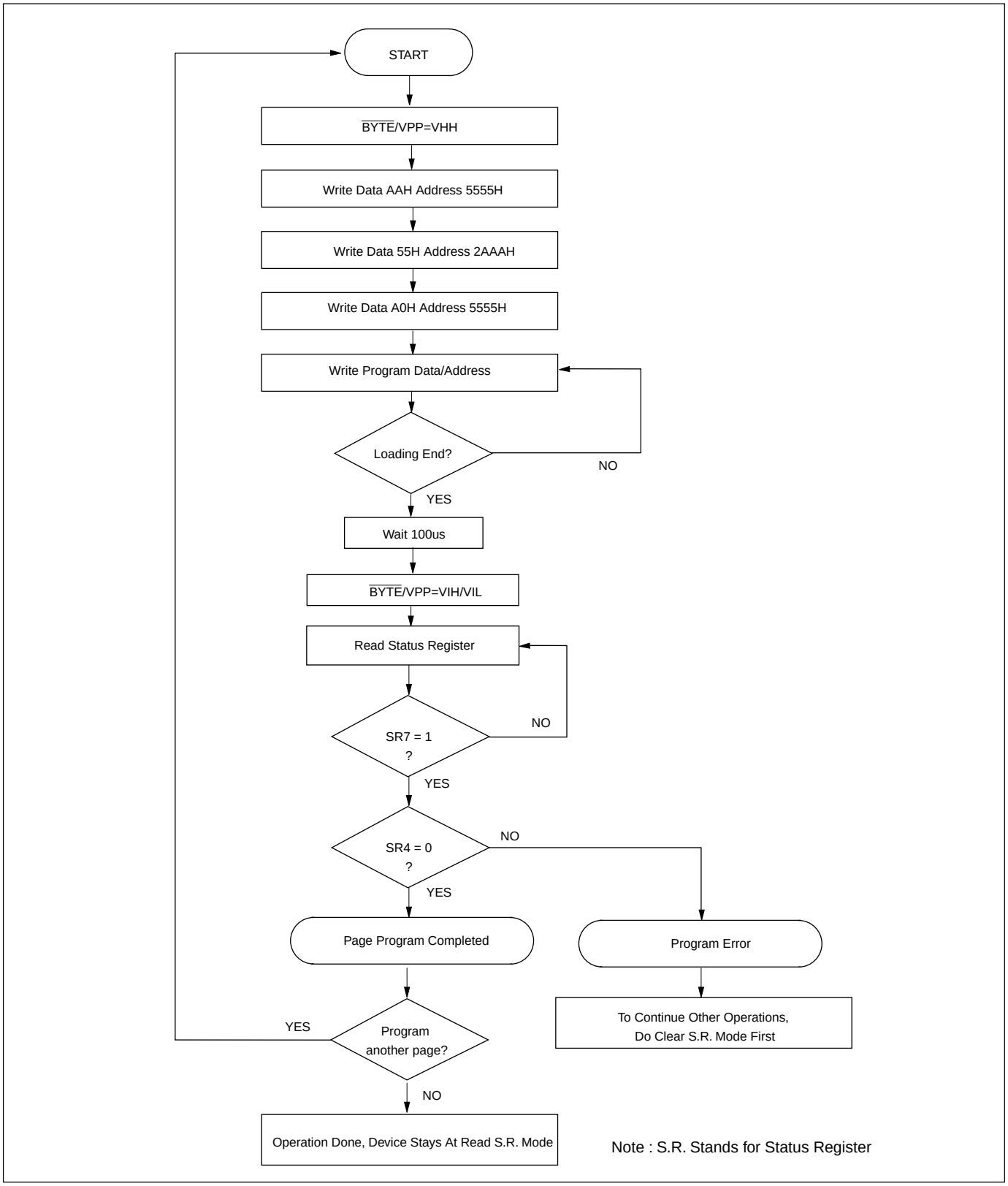
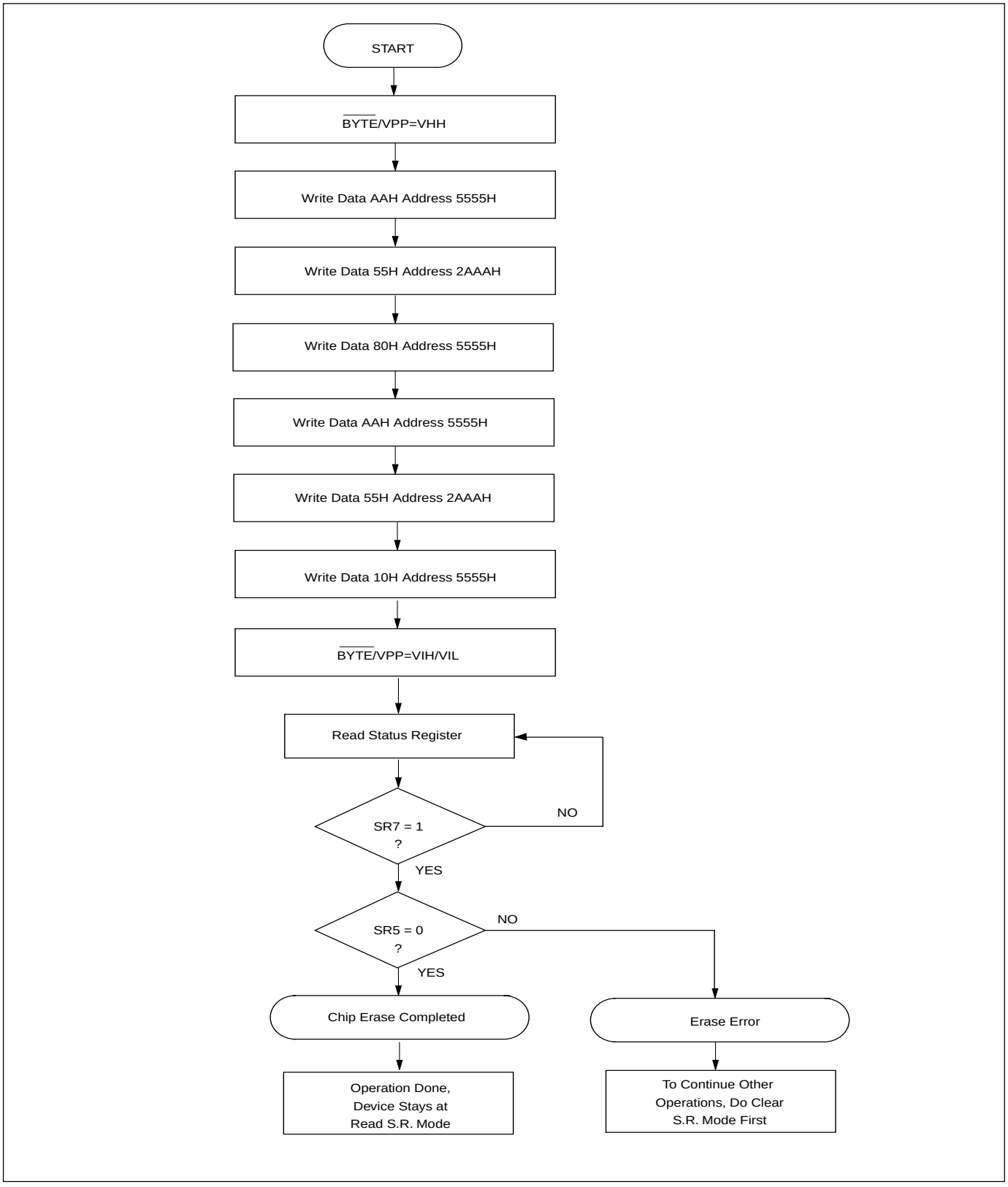


Figure 2. AUTOMATIC CHIP ERASE FLOW CHART



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0℃ to 70℃
Storage Temperature	-65℃ to 125℃
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9	-0.5V to 13.5V
$\overline{BYTE}$/VPP	-0.5V to 10.5V

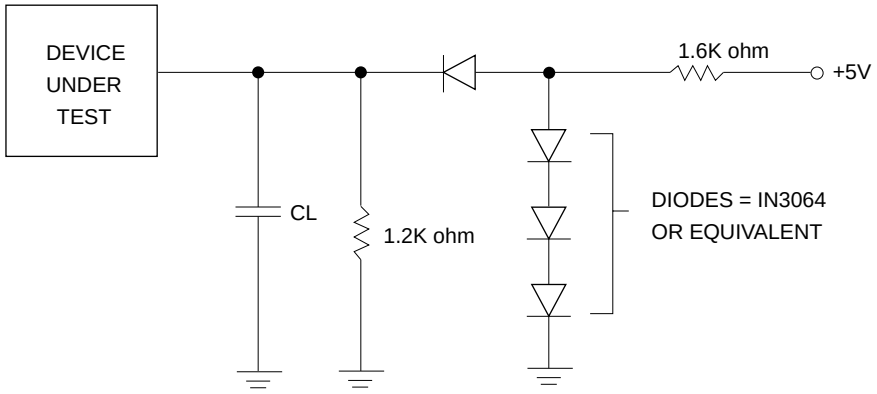
NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25℃, f = 1.0 MHz

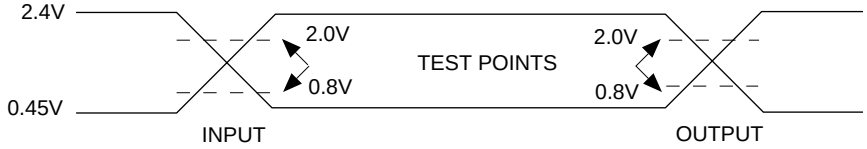
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			14	pF	VIN = 0V
CIN2	Control Pin Input Capacitance			16	pF	VIN=0V
COUT	Output Capacitance			16	pF	VOUT = 0V

SWITCHING TEST CIRCUITS



CL = 100 pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are < 10ns.

DC CHARACTERISTICS = 0℃ to 70℃, VCC = 5V±10%

SYMBOL	PARAMETER	NOTES	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
IIL	Input Load Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current(CMOS)	1		1	100	uA	VCC = VCC Max $\overline{CE}$= VCC ± 0.2V
ISB2	VCC Standby Current(TTL)			2	4	mA	VCC = VCC Max $\overline{CE}$= VIH
ICC1	VCC Read Current	1		50	60	mA	VCC = VCC Max CMOS: $\overline{CE}$ = GND ± 0.2V $\overline{BYTE}$/VPP=GND ± 0.2VorVCC ± 0.2V Inputs = GND ± 0.2V or VCC ± 0.2V TTL : $\overline{CE}$ = VIL, $\overline{BYTE}$/VPP = VIL or VIH Inputs = VIL or VIH, f = 10MHz, IOUT = 0 mA
ICC2	VCC Read Current	1		30	35	mA	VCC = VCC Max, CMOS: $\overline{CE}$ = GND ± 0.2V $\overline{BYTE}$/VPP = VCC ± 0.2V or GND ± 0.2V Inputs = GND ± 0.2V or VCC ± 0.2V TTL: $\overline{CE}$ = VIL, $\overline{BYTE}$/VPP= VIH or VIL Inputs = VIL or VIH, f = 5MHz, IOUT = 0mA
ICC3	VCC Erase Suspend Current	1,2		5	10	mA	$\overline{CE}$= VIH BLock Erase Suspended
ICC4	VCC Program Current	1		30	50	mA	Program in Progress
ICC5	VCC Erase Current	1		30	50	mA	Erase in Progress
VIL	Input Low Voltage	3	-0.3		0.8	V	
VIH	Input High Voltage	4	2.4		VCC+0.3V		
VOL	Output Low Voltage				0.45	V	IOL = 2.1mA
VOH	Output High Voltage		2.4			V	IOH = -2mA

DC CHARACTERISTICS = 0℃ to 70℃, VCC = 5V±10%(CONTINUE P.15)

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at VCC = 5.0V, T = 25℃. These currents are valid for all product versions (package and speeds).
2. ICC3 is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of ICC3 and ICC1/2.
3. VIL min. = -1.0V for pulse width is equal to or less than 50ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20ns.
4. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20ns. If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS—READ OPERATIONS

		29F1615-90		29F1615-10		29F1615-12			
SYMBOL	**DESCRIPTIONS**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**	**CONDITIONS**
tACC	Address to Output Delay		90		100		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		90		100		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		50		50		60	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Delay	0	35	0	35	0	35	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

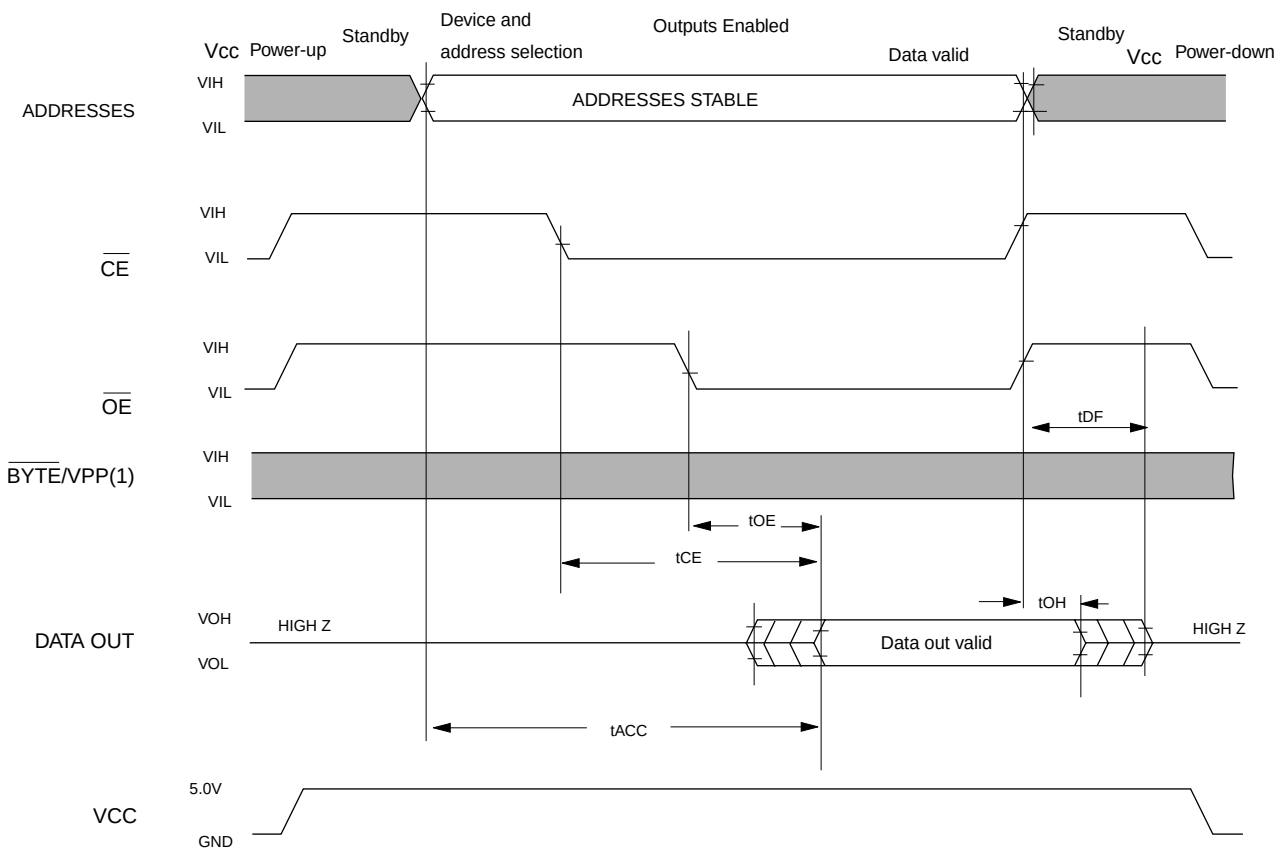
TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: 10ns
- Output load: 1TTL gate+100pF(Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Figure 3. READ TIMING WAVEFORMS



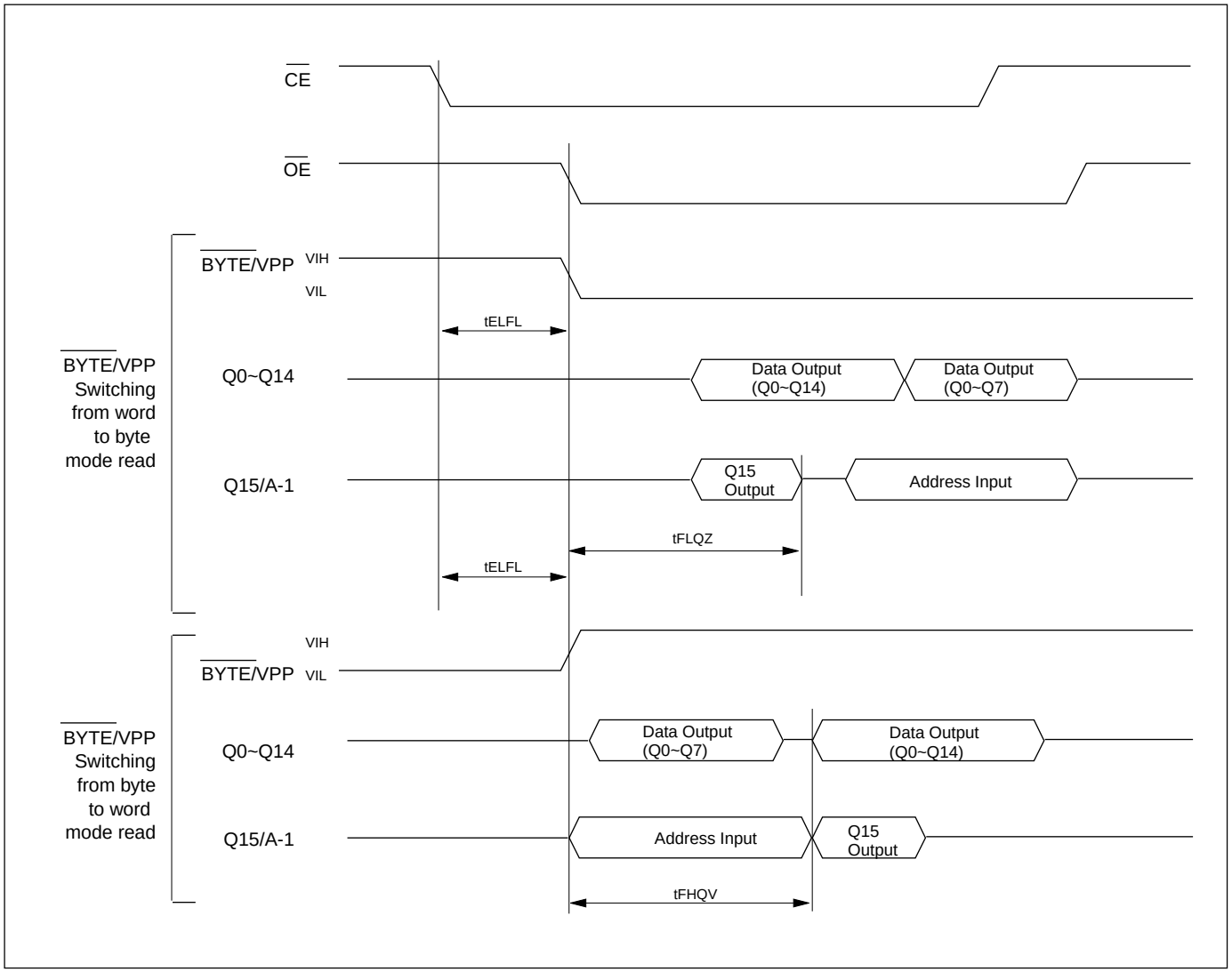
NOTE:

1.For real world application, BYTE/VPP pin should be either static high(word mode read) or static low(byte mode read); dynamic switching of BYTE/VPP pin is not recommended.

AC CHARACTERISTICS– WORD/BYTE CONFIGURATION ($\overline{BYTE}$/VPP)

		Speed Options			
Symbol	**Description**	**90**	**100**	**120**	**unit**
tELFL/tELFH	$\overline{CE}$ to $\overline{BYTE}$/VPP Switching Low or High MAX	5	5	5	ns
tFLQZ	$\overline{BYTE}$/VPP Switching Low to Output HIHG ZMax	30	30	30	ns
tFHQV	$\overline{BYTE}$/VPP Switching High to Output ActiveMin	90	100	120	ns

Figure 4. $\overline{BYTE}$/VPP TIMING WAVEFORMS



AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS

SYMBOL	DESCRIPTION	29F1615-90 MIN.	29F1615-90 MAX.	29F1615-10 MIN.	29F1615-10 MAX.	29F1615-12 MIN.	29F1615-12 MAX.	UNIT
tWC	Write Cycle Time	90		100		120		ns
tAS	Address Setup Time	0		0		0		ns
tAH	Address Hold Time	50		50		60		ns
tDS	Data Setup Time	50		50		60		ns
tDH	Data Hold Time	0		0		0		ns
tOES	Output Enable Setup Time	0		0		0		ns
tCES	$\overline{CE}$ Setup Time	0		0		0		ns
tGHWL	Read Recover Time Before Write	0		0		0		
tCS	$\overline{CE}$ Setup Time	0		0		0		ns
tCH	$\overline{CE}$ Hold Time	0		0		0		ns
tWP	Write Pulse Width	50		50		60		ns
tWPH	Write Pulse Width High	30		30		50		ns
tBALC	Word Address Load Cycle	0.3	30	0.3	30	0.3	30	us
tBAL	Word Address Load Time	100		100		100		us
tSRA	Status Register Access Time	70		70		90		ns
tCESR	$\overline{CE}$ Setup before S.R. Read	70		70		70		ns
tVCS	VCC Setup Time	50		50		50		us
tVPS	VPP Setup Time	2		2		2		us
tVPH	VPP Hold Time	2		2		2		us

Figure 5. COMMAND WRITE TIMING WAVEFORMS

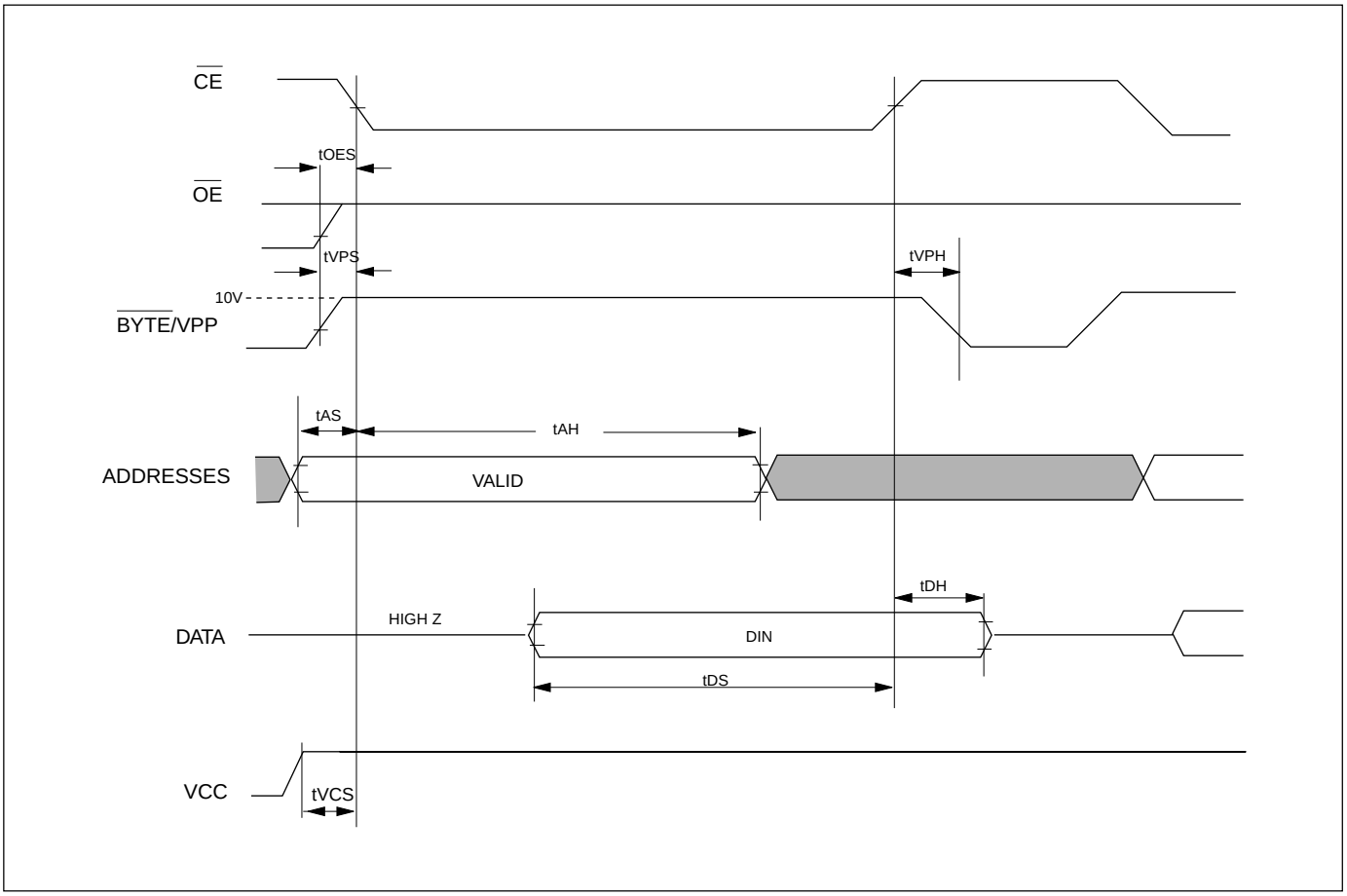
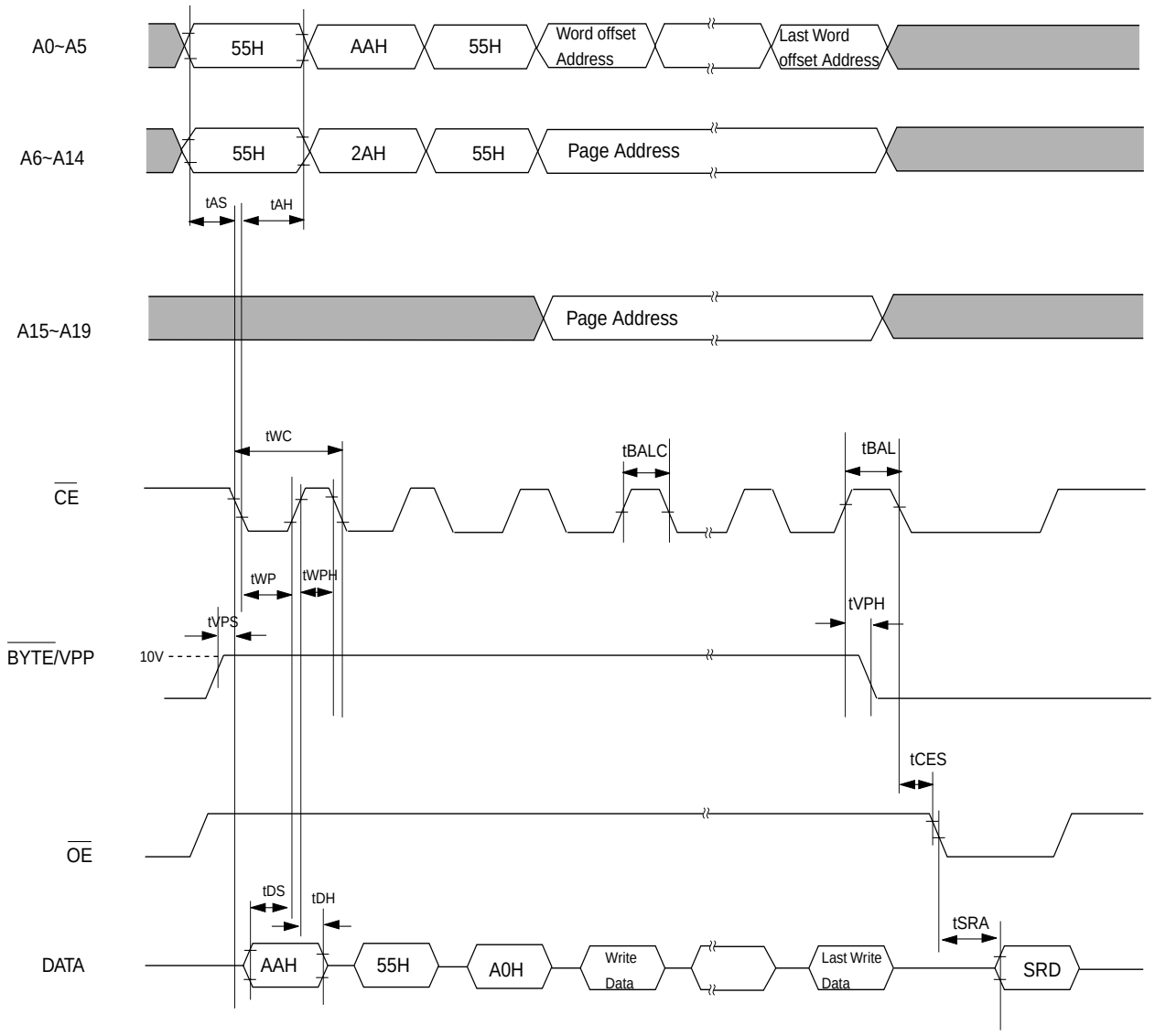


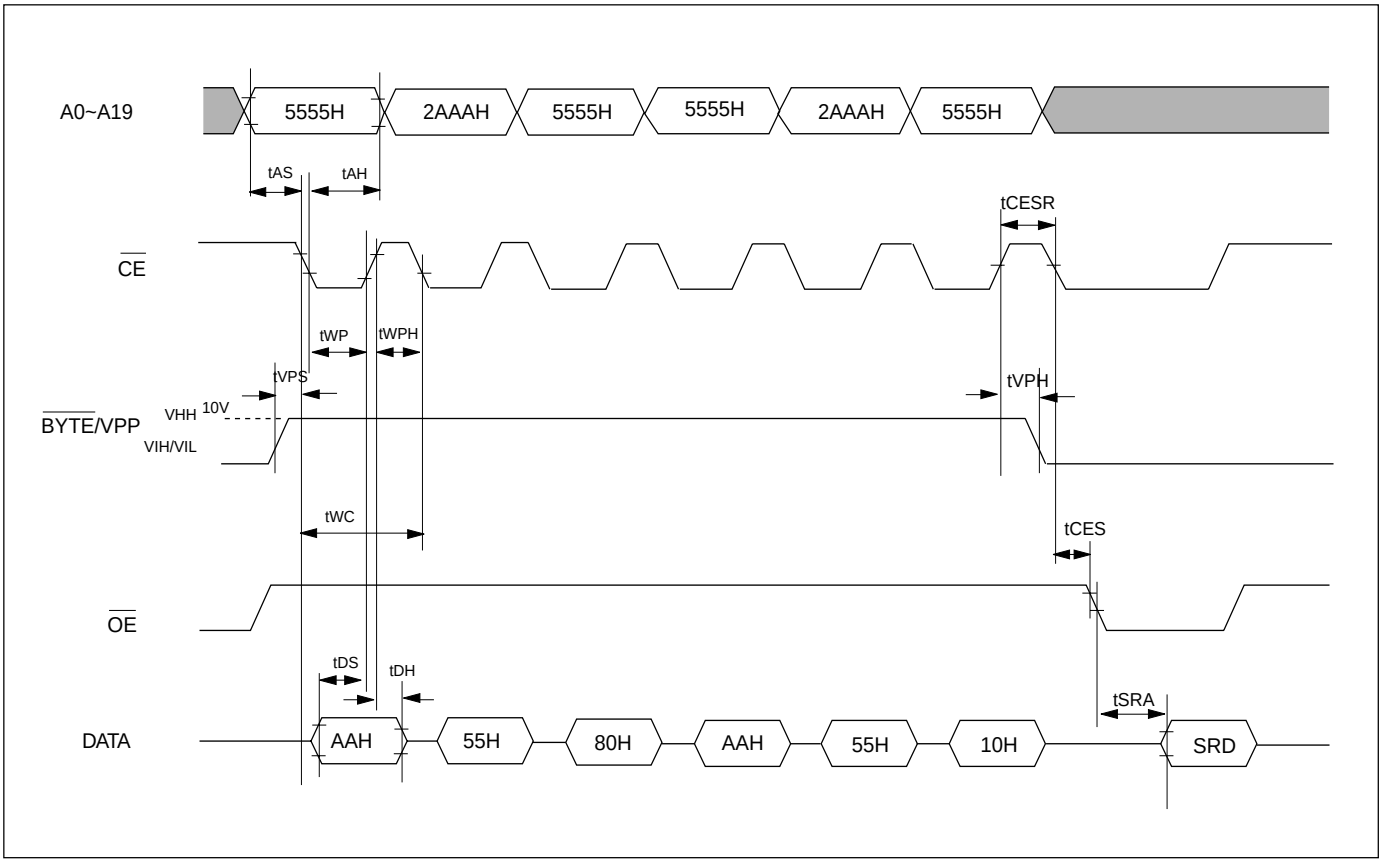
Figure 6. AUTOMATIC PAGE PROGRAM TIMING WAVEFORMS



NOTE:

1.Please refer to page 9 for detail page program operation.

Figure 7. AUTOMATIC CHIP ERASE TIMING WAVEFORMS



ERASE AND PROGRAMMING PERFORMANCE(1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.	
Chip Erase Time		32	256	sec
Page Programming Time		0.9	27	ms
Chip Programming Time		14	42	sec
Erase/Program Cycles	100			Cycles
Word Program Time		14	420	us

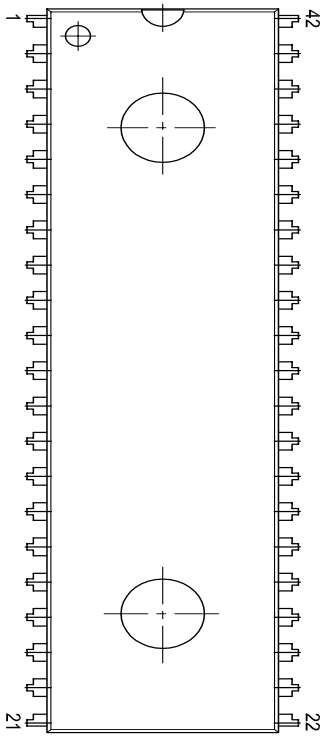
Note: 1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25℃,5V.

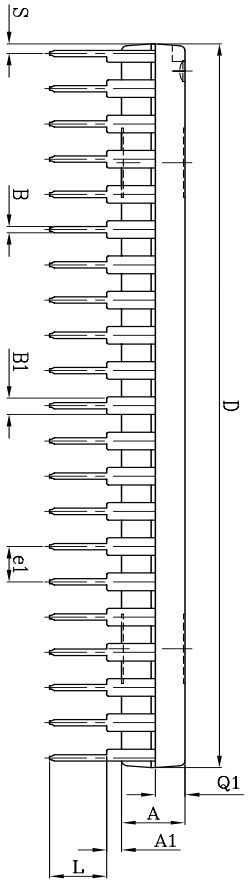
LATCHUP CHARACTERISTICS

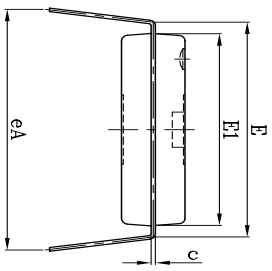
	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

PACKAGE INFORMATION

42-PIN PLASTIC DIP(600 mil)







SYMBOL / UNIT	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
c	0.010 (REF.)	0.254 (REF.)
D	2.05±0.005	52.07±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.025±0.005	0.635±0.127

MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd.				DWG. NO.	
TITLE: PACKAGE OUTLINE FOR PDIP 42L (600 MIL)				6110-0202.5	
				TOLERANCE	
				.X ± .1	ANGLE
				.XX ±.01	
				.XXX±.002	
DRAWN	APPROVED	DATE	UNIT	REVISION	
C.L.Chiang	Leo Lee	05-02-'01		4	

REVISION HISTORY

Revision	Description	Page	Date
1.1	To modify "Package Information"	P24	JUN/15/2001

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-348-8385
FAX:+65-348-8096

TAIPEI OFFICE:
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com