OKI Semiconductor

This version: Jun. 1999
Previous version: Sep. 1998

MSM54V25632A

131,072-Word × 32-Bit × 2-Bank Synchronous Graphics RAM

DESCRIPTION

The MSM54V25632A is a synchronous graphics random access memory organized as 128 K words × 32 bits × 2 banks.
This device can operate up to 100 MHz by using synchronous interface. In addition, it has 8-column Block Write function and Write per bit function which improves performance in graphics systems.

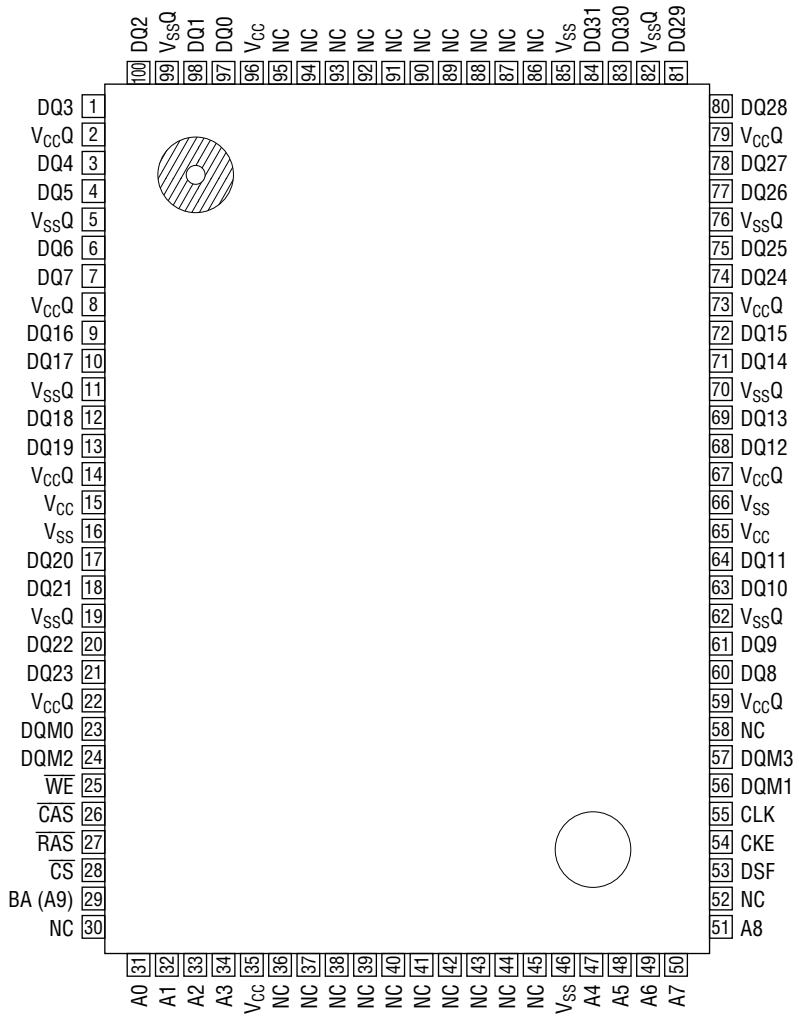
FEATURES

- 131,072 words × 32 bits × 2 banks memory
- Single 3.3 V ±0.3 V power supply
- LVTTL compatible inputs and outputs
- All input signals are latched at rising edge of system clock
- Auto precharge and controlled precharge
- Internal pipelined operation: column address can be changed every clock cycle
- Dual internal banks controlled by A9 (Bank Address: BA)
- Independent byte operation via DQM0 to DQM3
- 8-column Block Write function
- Persistent write per bit function
- Programmable burst sequence (Sequential/Interleave)
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable $\overline{\text{CAS}}$ latency (1, 2 and 3)
- Burst stop function (full-page burst)
- Power Down operation and Clock Suspend operation
- Auto refresh and self refresh capability
- 1,024 refresh cycles/16 ms
- Package:
  100-pin plastic QFP (QFP100-P-1420-0.65-BK4) (Product : MSM54V25632A-xxAGBK4)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Clock Frequency MHz (Max.)	Package
MSM54V25632A-10	100	100-pin Plastic QFP (14 × 20 mm)
MSM54V25632A-12	83	

PIN CONFIGURATION (TOP VIEW)

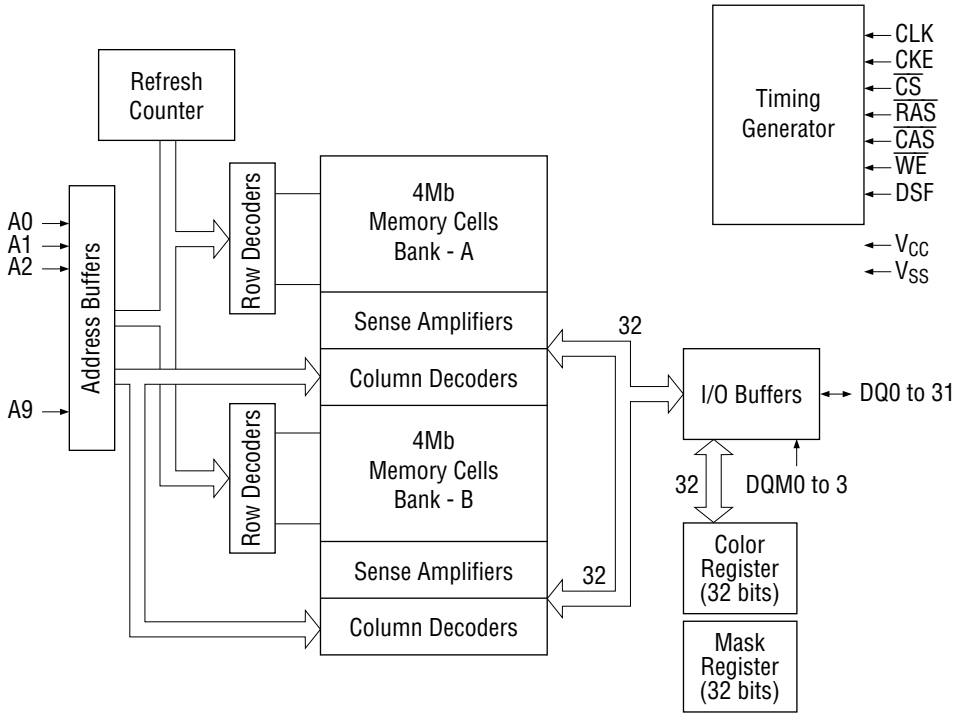


100-Pin Plastic QFP

Pin Name	Function	Pin Name	Function
A0 - A9	Address Inputs	DQM0 - DQM3	DQ Mask Enable
A0 - A8	Row Address Inputs	DSF	Special Function Enable
A0 - A7	Column Address Inputs	CKE	Clock Enable
A9	Bank Address	CLK	System Clock Input
DQ0 - DQ31	Data Inputs/Outputs	V_{CC}	Supply Voltage
$\overline{CS}$	Chip Select	V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe	$V_{CC}Q$	Supply Voltage for DQ
$\overline{CAS}$	Column Address Strobe	$V_{SS}Q$	Ground for DQ
$\overline{WE}$	Write Enable	NC	No Connection

Note: The same power supply voltage must be provided to every V_{CC} pin and $V_{CC}Q$ pin. The same GND voltage level must be provided to every V_{SS} pin and $V_{SS}Q$ pin.

BLOCK DIAGRAM



PIN DESCRIPTION

CLK	Fetches all inputs at the "H" edge.
$\overline{CS}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, DQM0, DQM1, DQM2 and DQM3.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address: RA0 – RA8 Column address: CA0 – CA7
BA (A9)	Selects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time. A9 = "L" : Bank A, A9 = "H" : Bank B
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Functionality depends on the combination. For details, see the function truth table.
DSF	DSF is part of the inputs of graphics command of the MSM54V25632A. If DSF is inactive (Low level), MSM54V25632A operates just like SDRAM.
DQM0 - DQM3	Masks the read data of two clocks later when DQM0 - DQM3 are set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM0 - DQM3 are set "H" at the "H" edge of the clock signal.
DQi	Data inputs/outputs are multiplexed on the same pin.

***Notes:** 1. When $\overline{CS}$ is set "High" at a clock transition from "Low" to "High", all inputs except CLK, CKE, DQM0, DQM1, DQM2, and DQM3 are invalid.

2. When issuing an active, read or write command, the bank is selected by A9.

A9	Active, read or write
0	Bank A
1	Bank B

3. The auto precharge function is enabled or disabled by the A8 input when the read or write command is issued.

A8	A9	Operation
0	0	After the end of burst, bank A holds the active status.
1	0	After the end of burst, bank A is precharged automatically.
0	1	After the end of burst, bank B holds the active status.
1	1	After the end of burst, bank B is precharged automatically.

4. When issuing a precharge command, the bank to be precharged is selected by the A8 and A9 inputs.

A8	A9	Operation
0	0	Bank A is precharged.
0	1	Bank B is precharged.
1	X	Both banks A and B are precharged.

COMMAND OPERATION

Mode Register Set Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF = "Low")

The MSM54V25632A has the mode register that defines the operation mode "$\overline{CAS}$ Latency, Burst Length, Burst Sequence". The mode register is composed of ten bits of memories corresponding to address inputs A0 - A8 and BA. The Mode Register Set command should be executed just after the MSM54V25632A is powered on. Before entering this command, all banks must be precharged. Next command can be issued after t_{RSC}.

Special Mode Register Set Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = "Low", DSF = "High")

The MSM54V25632A has the 32-bit color register for block write operation and the 32-bit mask register for write per bit operation. The Special Mode Register Set command performs loading mask register or color register. When A5 is "high", The mask data presented on the DQ0 - DQ31 is latched into the mask register. When A6 is "high", The color data presented on the DQ0 - DQ31 is latched into the color register. The Special Mode Register Set command must be executed before Masked Block Write and Write Per Bit operations. Next command can be issued after t_{RSC}.

Auto Refresh Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, DSF = "Low", $\overline{WE}$, CKE = "High")

The Auto Refresh command performs refresh automatically by the address counter. The refresh operation must be performed 1024 times within 16 ms and the next command can be issued after t_{RC} from last Auto Refresh command. Before entering this command, all banks must be precharged.

Self Refresh Entry/Exit Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, DSF, CKE = "Low", $\overline{WE}$ = "High")

The self refresh operation continues after the Self Refresh Entry command is entered, with CKE level left "low". This operation terminates by making CKE level "high". The self refresh operation is performed automatically by the internal address counter on the MSM54V25632A chip. In self refresh mode, no external refresh control is required. Before entering self refresh mode, all banks must be precharged. Next command can be issued after t_{RC}.

Single Bank Precharge Command ($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$, DSF, A8 = "Low", $\overline{CAS}$ = "High")

The Single Bank Precharge command triggers bank precharge operation. Precharge bank is selected by BA.

All Banks Precharge Command ($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$, DSF = "Low", $\overline{CAS}$, A8 = "High")

The All Bank Precharge command triggers precharge of both bank A and bank B.

Bank Active and Masked Write Disable Command ($\overline{CS}$, $\overline{RAS}$, DSF = "Low", $\overline{CAS}$, $\overline{WE}$ = "High")

The Bank Active command activates the bank selected by BA. The Bank Active command corresponds to conventional DRAM's $\overline{RAS}$ falling operation. Row addresses "A0 - A8 and BA" are strobed. After this command, the write command and block write command for that bank works as the no write per bit operation.

Bank Active and Masked Write Enable Command ($\overline{CS}$, $\overline{RAS}$ = "Low", $\overline{CAS}$, $\overline{WE}$, DSF = "High")

The Bank Active command activates the bank selected by BA. The Bank Active command corresponds to conventional DRAM's $\overline{RAS}$ falling operation. Row addresses "A0 - A8 and BA" are strobed. After this command, the write command and block write command for that bank works as the write per bit operation.

Write Command ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$, DSF, A8 = "Low", $\overline{RAS}$ = "High")

The Write command is required to begin burst write operation. Then burst access initial bit column address is strobed.

Write with Auto Precharge Command ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$, DSF = "Low", $\overline{RAS}$, A8 = "High")

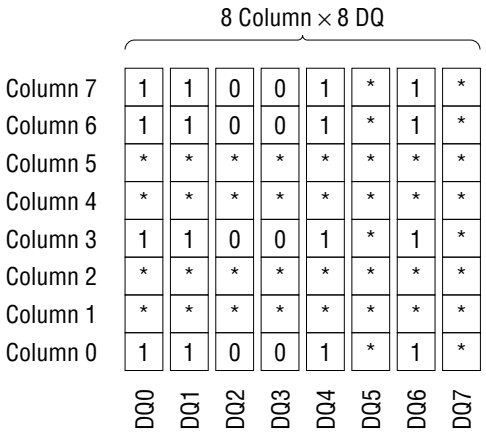
The Write with Auto Precharge command is required to begin burst write operation with automatic precharge after the burst write. Any command that interrupts this operation cannot be issued.

Masked Block Write Command ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$, A8 = "Low", $\overline{RAS}$, DSF = "High")

The Masked Block Write command is required to begin block write operation with column mask. The masked block write operation performs writing in the 8 memory cells selected by column addresses "A3 - A7". In this operation, data in color register is written to memory cells with the column mask functions. At the same time, this command can perform write per bit operation. The block write operation is not bursted.

Block Write Function

Color Register	11001110
I/O Mask	11111010
Column Mask	10010011



Note : Location "*" can not be loaded.

Remark: 1. This diagram shows only for DQ0 - 7. The other DQ is similar as this.

Column Mask

DQ0 - 7 : Column Mask for DQ0 - 7
DQ8 - 15 : Column Mask for DQ8 - 15
DQ16 - 23: Column Mask for DQ16 - 23
DQ24 - 31: Column Mask for DQ24 - 31

Write per Bit

Mask data = Mask Register + DQMi
DQMi is prior to data of Mask Register.

Masked Block Write with Auto Precharge Command ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = "Low", $\overline{RAS}$, DSF, A8 = "High")

The Masked Block Write with Auto Precharge command performs precharging at the bank selected by BA automatically after Masked Block Write.

Read Command ($\overline{CS}$, $\overline{CAS}$, DSF, A8 = "Low", $\overline{RAS}$, $\overline{WE}$ = "High")

The Read command is required to begin burst read operation. Then burst access initial bit column address is strobed.

Read with Auto Prechaege Command ($\overline{CS}$, $\overline{CAS}$, DSF = "Low", $\overline{RAS}$, $\overline{WE}$, A8 = "High")

The Read with Auto Precharge command is required to begin burst read operation with auto precharge after the burst read. Any command that interrupts this operation cannot be issued.

No Operation Command ($\overline{CS}$, DSF = "Low", $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = "High")

The No Operation command does not trigger any operation.

Device Deselect Command ($\overline{CS}$ = "High")

The Device Deselect command disables the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF and Address input. This command does not trigger any operation.

Data Write/Output Enable Command (DQMi = "Low")

The Data Write/Output Enable command enables DQ0 - DQ31 in read or write.
The each DQM0, 1, 2 and 3 corresponds to DQ0 - DQ7, DQ8 - DQ15, DQ16 - DQ23 and DQ24 - DQ31 respectively.

Data Mask/Output Disable Command (DQMi = "High")

The Data Mask/Output Disable command disables DQ0 - DQ31. In read cycle output buffers are disabled after 2 clocks . In write cycle input buffers are disabled at the same clock. The each DQM0, 1, 2 and 3 corresponds to DQ0 - DQ7, DQ8 - DQ15, DQ16 - DQ23 and DQ24 - DQ31 respectively.

Burst Stop Command ($\overline{CS}$, $\overline{WE}$, DSF = "Low", $\overline{RAS}$, $\overline{CAS}$ = "High")

The Burst Stop command stops burst access when the access is in full page. After the Burst Stop command is entered, the output buffer goes into high impedance state.

TRUTH TABLE

Command Truth Table

Function	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address		
						A9	A8	A7 - A0
Device Deselect	H	×	×	×	×	×	×	×
No Operation	L	H	H	H	L	×	×	×
Burst Stop in Full Page	L	H	H	L	L	×	×	×
Read	L	H	L	H	L	BA	L	CA
Read with Auto Precharge	L	H	L	H	L	BA	H	CA
Write	L	H	L	L	L	BA	L	CA
Write with Auto Precharge	L	H	L	L	L	BA	H	CA
Masked Block Write	L	H	L	L	H	BA	L	CA
Masked Block Write with Auto Precharge	L	H	L	L	H	BA	H	CA
Bank Activate	L	L	H	H	L	BA	RA	
Bank Activate with WPB Enable	L	L	H	H	H	BA	RA	
Precharge Select Bank	L	L	H	L	L	BA	L	×
Precharge All Banks	L	L	H	L	L	×	H	×
Mode Register Set	L	L	L	L	L	OP. CODE		
Special Register Set	L	L	L	L	H	OP. CODE		

DQM Truth Table

Function	DQMi
Data Write/Output Enable	L
Data Mask/Output Disable	H

Function Truth Table (1/5)

Note 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Action	Note
Idle	H	×	×	×	×	×	NOP or Power Down	
	L	H	H	H	×	×	NOP or Power Down	
	L	H	H	L	H	×	ILLEGAL	2
	L	H	H	L	L	×	ILLEGAL	2
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	ILLEGAL	2
	L	H	L	L	H	BA, CA, A8	ILLEGAL	2
	L	H	L	L	L	BA, CA, A8	ILLEGAL	2
	L	L	H	H	H	BA, RA	Row Active with WPB	
	L	L	H	H	L	BA, RA	Row Active	
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	NOP	3
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	Auto Refresh/Self refresh	4
	L	L	L	L	H	Op-Code	Special Register Write	
	L	L	L	L	L	Op-Code	Mode Register Write	
Row Active (ACT)	H	×	×	×	×	×	NOP	
	L	H	H	H	×	×	NOP	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	ILLEGAL	2
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	Read	
	L	H	L	L	H	BA, CA, A8	Block Write	
	L	H	L	L	L	BA, CA, A8	Write	
	L	L	H	H	H	BA, RA	ILLEGAL	2
	L	L	H	H	L	BA, RA	ILLEGAL	2
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	Precharge	
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op-Code	Special Register Write	
	L	L	L	L	L	Op-Code	ILLEGAL	

Function Truth Table (2/5)

Note 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Action	Note
Read (RD)	H	×	×	×	×	×	NOP (Continue Row Active after Burst ends)	
	L	H	H	H	×	×	NOP (Continue Row Active after Burst ends)	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	1, 2, 4, 8 Burst Length; ILLEGAL Full Page Burst; Burst Stop → Bank Active	
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	Term Burst, new Read	
	L	H	L	L	H	BA, CA, A8	Term Burst, start Block Write	
	L	H	L	L	L	BA, CA, A8	Term Burst, start Write	
	L	L	H	H	H	BA, RA	ILLEGAL	2
	L	L	H	H	L	BA, RA	ILLEGAL	2
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	Term Burst, execute Row Precharge	
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op-Code	ILLEGAL	
	L	L	L	L	L	Op-Code	ILLEGAL	
Write/Block Write (WT/BW)	H	×	×	×	×	×	NOP (Continue Row Active after Burst ends)	
	L	H	H	H	×	×	NOP (Continue Row Active after Burst ends)	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	1, 2, 4, 8 Burst Length; ILLEGAL Full Page Burst; Burst Stop → Row Active	
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	Term Burst, start Read	
	L	H	L	L	H	BA, CA, A8	Term Burst, new Block Write	
	L	H	L	L	L	BA, CA, A8	Term Burst, new Write	
	L	L	H	H	H	BA, RA	ILLEGAL	2
	L	L	H	H	L	BA, RA	ILLEGAL	2
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	Term Burst, execute Row Precharge	
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op-Code	ILLEGAL	
	L	L	L	L	L	Op-Code	ILLEGAL	

Function Truth Table (3/5)

Note 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Action	Note
Read with Auto Precharge (RAP)	H	×	×	×	×	×	NOP (Continue Burst to End and enter Row Precharge)	
	L	H	H	H	×	×	NOP (Continue Burst to End and enter Row Precharge)	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	ILLEGAL	
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	ILLEGAL	
	L	H	L	L	H	BA, CA, A8	ILLEGAL	
	L	H	L	L	L	BA, CA, A8	ILLEGAL	
	L	L	H	H	H	BA, RA	ILLEGAL	2
	L	L	H	H	L	BA, RA	ILLEGAL	2
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	ILLEGAL	2
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op- Code	ILLEGAL	
	L	L	L	L	L	Op- Code	ILLEGAL	
Write/Block Write with Auto Precharge (WAP/BWAP)	H	×	×	×	×	×	NOP (Continue Burst to End and enter Row Precharge)	
	L	H	H	H	×	×	NOP (Continue Burst to End and enter Row Precharge)	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	ILLEGAL	
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	ILLEGAL	
	L	H	L	L	H	BA, CA, A8	ILLEGAL	
	L	H	L	L	L	BA, CA, A8	ILLEGAL	
	L	L	H	H	H	BA, RA	ILLEGAL	2
	L	L	H	H	L	BA, RA	ILLEGAL	2
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	ILLEGAL	2
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op- Code	ILLEGAL	
	L	L	L	L	L	Op- Code	ILLEGAL	

Function Truth Table (4/5)

Note 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Action	Note
Precharging (PRE)	H	×	×	×	×	×	NOP → Idle after t_{RP}	
	L	H	H	H	×	×	NOP → Idle after t_{RP}	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	ILLEGAL	2
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	ILLEGAL	2
	L	H	L	L	H	BA, CA, A8	ILLEGAL	2
	L	H	L	L	L	BA, CA, A8	ILLEGAL	2
	L	L	H	H	H	BA, RA	ILLEGAL	2
	L	L	H	H	L	BA, RA	ILLEGAL	2
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	NOP → Idle after t_{RP}	3
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op-Code	Special Register Write	
	L	L	L	L	L	Op-Code	ILLEGAL	
Refreshing (REF)	H	×	×	×	×	×	NOP → Idle after t_{RC}	
	L	H	H	H	×	×	NOP → Idle after t_{RC}	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	ILLEGAL	
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	ILLEGAL	
	L	H	L	L	H	BA, CA, A8	ILLEGAL	
	L	H	L	L	L	BA, CA, A8	ILLEGAL	
	L	L	H	H	H	BA, RA	ILLEGAL	
	L	L	H	H	L	BA, RA	ILLEGAL	
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	ILLEGAL	
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op-Code	ILLEGAL	
	L	L	L	L	L	Op-Code	ILLEGAL	

Function Truth Table (5/5)

Note 1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Action	Note
Mode Register Access (MRA)	H	×	×	×	×	×	NOP	
	L	H	H	H	×	×	NOP	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	ILLEGAL	
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	ILLEGAL	
	L	H	L	L	H	BA, CA, A8	ILLEGAL	
	L	H	L	L	L	BA, CA, A8	ILLEGAL	
	L	L	H	H	H	BA, RA	ILLEGAL	
	L	L	H	H	L	BA, RA	ILLEGAL	
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	ILLEGAL	
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op-Code	ILLEGAL	
	L	L	L	L	L	Op-Code	ILLEGAL	
Special Mode Register Access (SMRA)	H	×	×	×	×	×	NOP	
	L	H	H	H	×	×	NOP	
	L	H	H	L	H	×	ILLEGAL	
	L	H	H	L	L	×	ILLEGAL	
	L	H	L	H	H	×	ILLEGAL	
	L	H	L	H	L	BA, CA, A8	ILLEGAL	
	L	H	L	L	H	BA, CA, A8	ILLEGAL	
	L	H	L	L	L	BA, CA, A8	ILLEGAL	
	L	L	H	H	H	BA, RA	ILLEGAL	
	L	L	H	H	L	BA, RA	ILLEGAL	
	L	L	H	L	H	×	ILLEGAL	
	L	L	H	L	L	BA, A8	ILLEGAL	
	L	L	L	H	H	×	ILLEGAL	
	L	L	L	H	L	×	ILLEGAL	
	L	L	L	L	H	Op-Code	ILLEGAL	
	L	L	L	L	L	Op-Code	ILLEGAL	

ABBREVIATIONS

RA = Row Address BA = Bank Address NOP = No OPeration command

CA = Column Address AP = Auto Precharge × = High or Low level (Don't care)

Notes:
1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. NOP to bank precharging or in idle state. Precharges activated bank by BA or A8.
4. Illegal if any bank is not idle.

Function Truth Table for CKE

Current State (n)	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Action	Note
Self Refresh (SREF)	H	×	×	×	×	×	×	×	INVALID	5
	L	H	H	×	×	×	×	×	Exit Self Refresh → ABI	5
	L	H	L	H	H	H	×	×	Exit Self Refresh → ABI	5
	L	H	L	H	H	L	×	×	ILLEGAL	5
	L	H	L	H	L	×	×	×	ILLEGAL	5
	L	H	L	L	×	×	×	×	ILLEGAL	5
	L	L	×	×	×	×	×	×	NOP (Maintain Self Refresh)	5
Power Down (PD)	H	×	×	×	×	×	×	×	INVALID	5
	L	H	H	×	×	×	×	×	Exit Power Down → ABI	5
	L	H	L	H	H	H	×	×	Exit Power Down → ABI	5
	L	H	L	H	H	L	×	×	ILLEGAL	5
	L	H	L	H	L	×	×	×	ILLEGAL	5
	L	H	L	L	×	×	×	×	ILLEGAL	5
	L	L	×	×	×	×	×	×	NOP (Continue power down mode)	5
All Banks Idle (ABI)	H	H	×	×	×	×	×	×	Refer to Table	6
	H	L	H	×	×	×	×	×	Enter Power Down	6
	H	L	L	H	H	H	×	×	Enter Power Down	6
	H	L	L	H	H	L	×	×	ILLEGAL	6
	H	L	L	H	L	×	×	×	ILLEGAL	6
	H	L	L	L	H	L	×	×	ILLEGAL	6
	H	L	L	L	L	H	L	×	Enter Self Refresh	6
	H	L	L	L	L	L	×	×	ILLEGAL	6
	L	L	×	×	×	×	×	×	NOP	6
Any State Other than Listed Above	H	H	×	×	×	×	×	×	Refer to Operations in Table	
	H	L	×	×	×	×	×	×	Begin Clock Suspend Next Cycle	
	L	H	×	×	×	×	×	×	Enable Clock of Next Cycle	
	L	L	×	×	×	×	×	×	Continue Clock Suspension	

Notes: 5. If the minimum set-up time t_{PDE} is satisfied when CKE transitions from "L" to "H", CKE operates asynchronously so that a command can be input in the same internal clock cycle.
6. Power-down and self refresh can be entered only when all the banks are in an idle state.

Mode Set Address Keys

Operation Code			$\overline{CAS}$ Latency (CL)				Burst Type (BT)		Burst Length (BL)				
A8	A7	TM	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Setting	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Full Page	Reserved

Special Mode Set Address Keys

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	LC	LM	0	0	0	0	0

Load Color (LC)		Load Mask (LM)	
A6	Function	A5	Function
0	Disable	0	Disable
1	Enable	1	Enable

Note : If LC and LM are both high (1), data of Mask and Color register will be unknown.

POWER ON SEQUENCE

1. With CKE = "H", DQM = "H" and the other inputs in NOP state, turn on the power supply and start the system clock.
2. After the V_{CC} voltage has reached the specified level, pause for 200 µs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply an Auto-refresh eight or more times.
5. Enter the mode register setting command.

Burst Length and Sequence

BL = 2

Starting Address (column address A0, binary)	Sequential Type	Interleave Type
0	0, 1	Not supported
1	1, 0	Not supported

BL = 4

Starting Address (column address A1 - A0, binary)	Sequential Type	Interleave Type
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

BL = 8

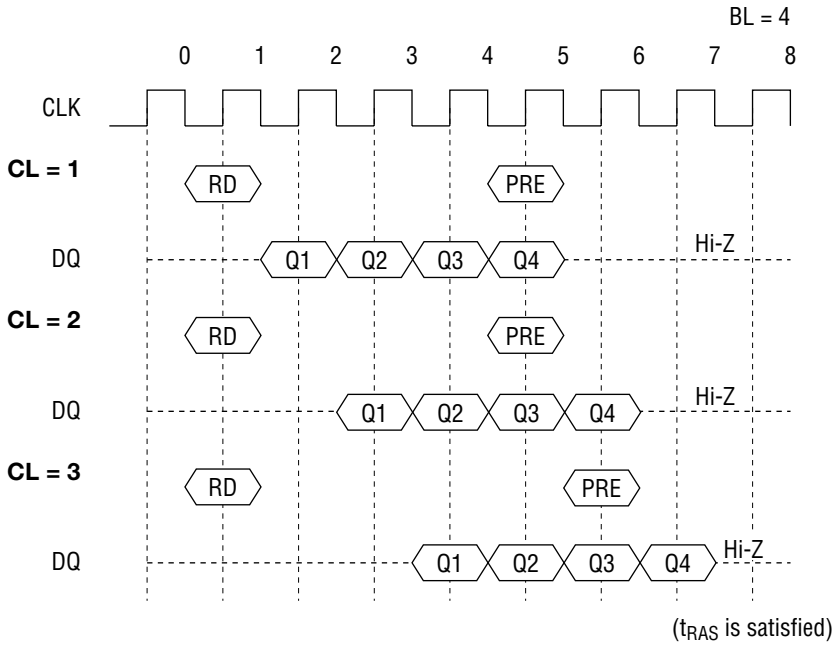
Starting Address (column address A2 - A0, binary)	Sequential Type	Interleave Type
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4 ,5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

BL = Full : Sequential only

PRECHARGE

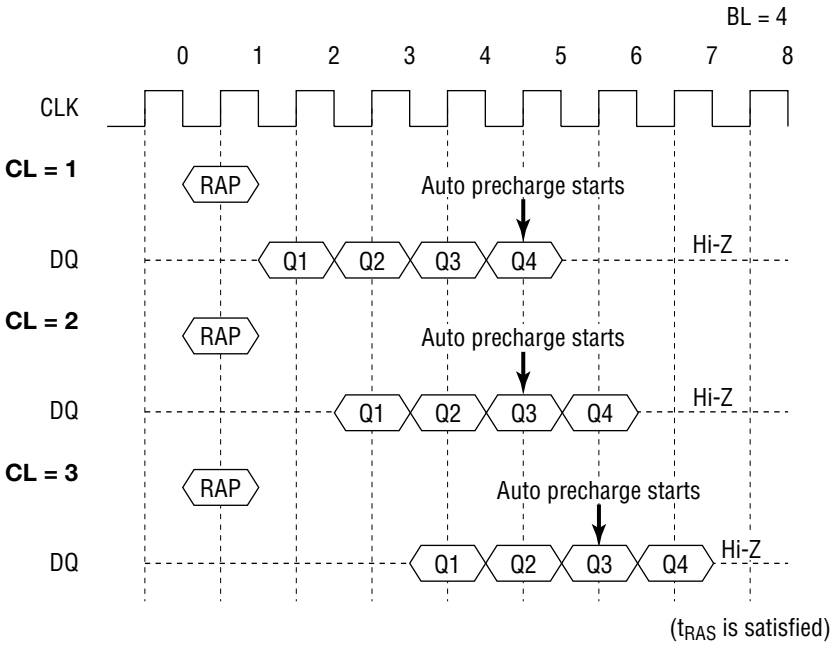
Read Interrupted by Precharge

CL = 1 : At the same clock as the last read data.
CL = 2 or 3 : One clock earlier than the last read data.

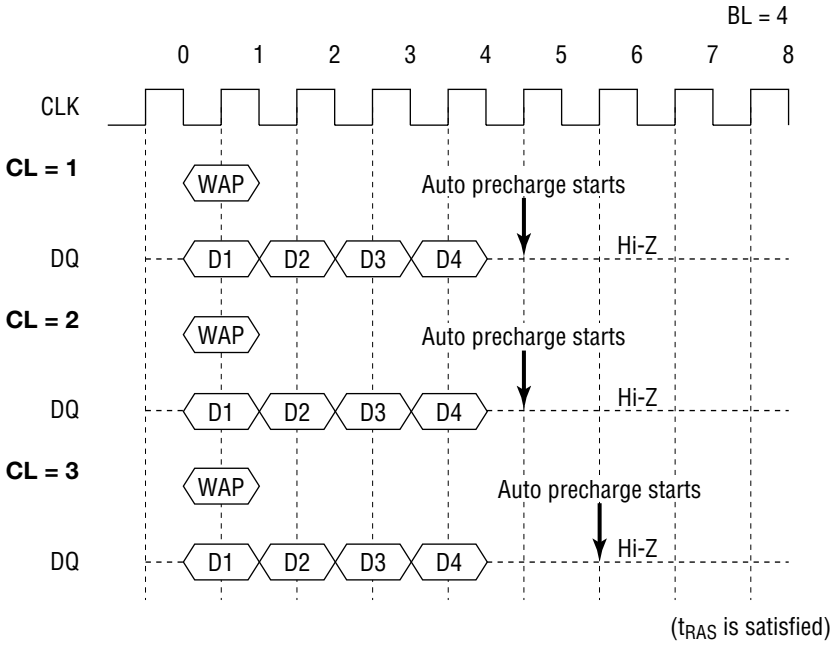


AUTO PRECHARGE

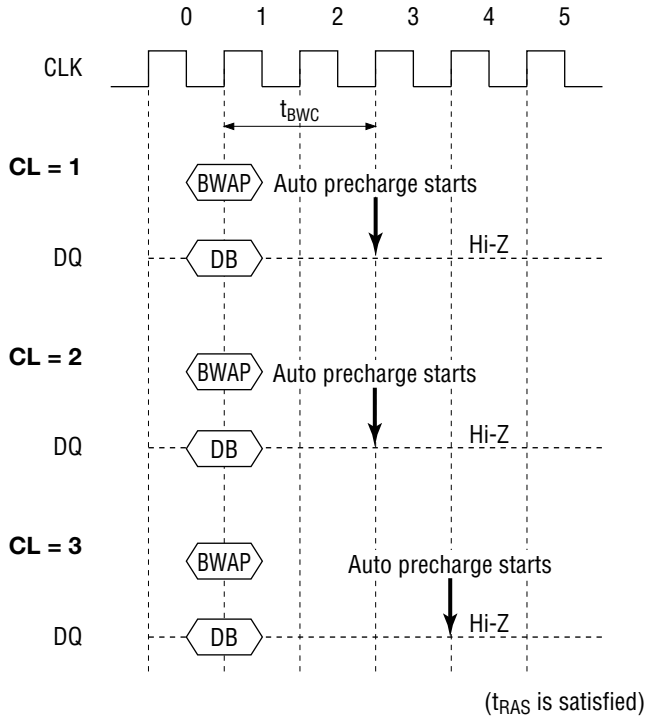
Read with Auto Precharge



Write with Auto Precharge

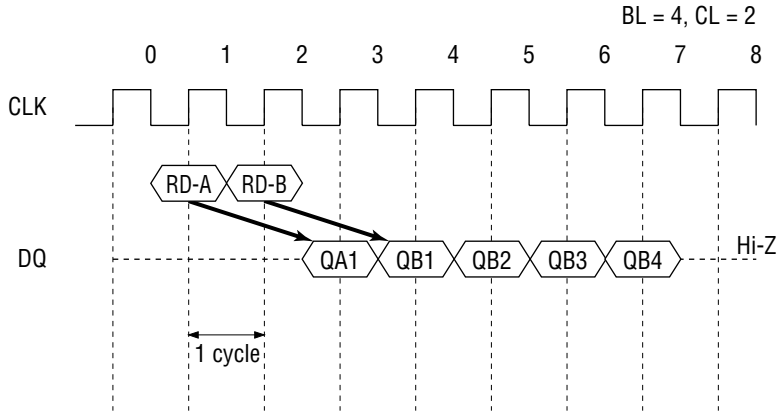


Block Write with Auto Precharge

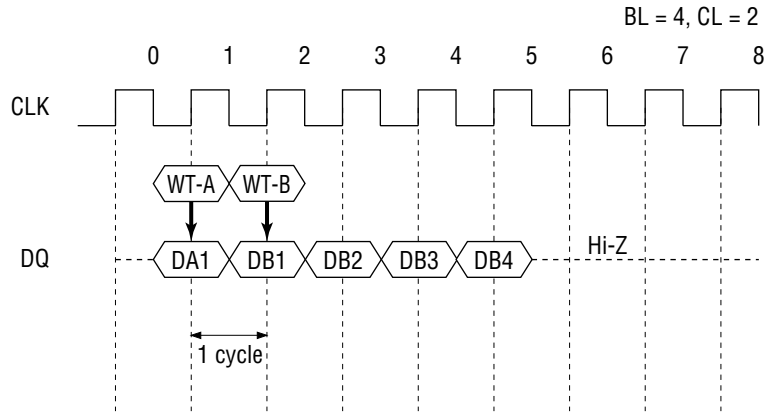


READ/WRITE COMMAND INTERVAL

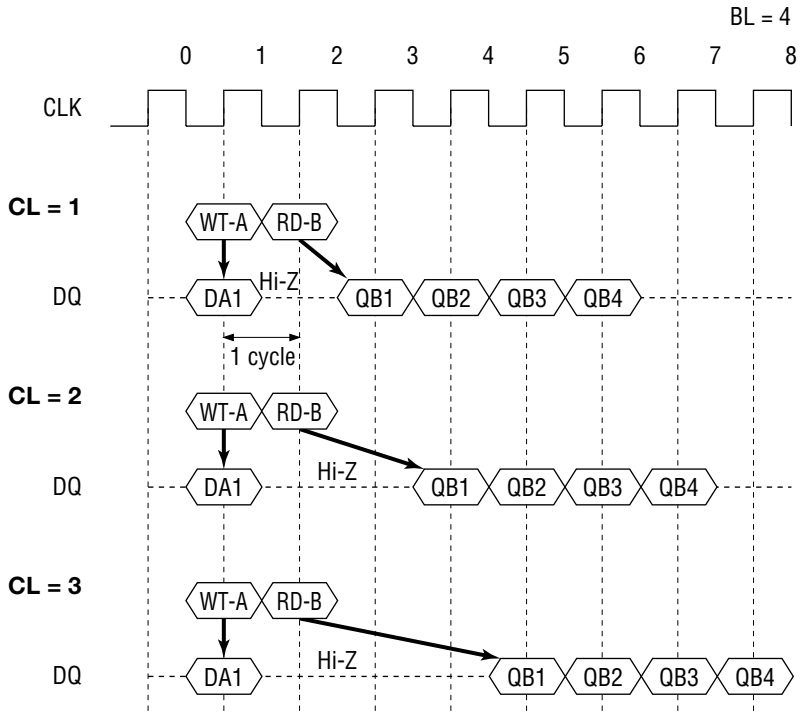
Read to Read Command Interval



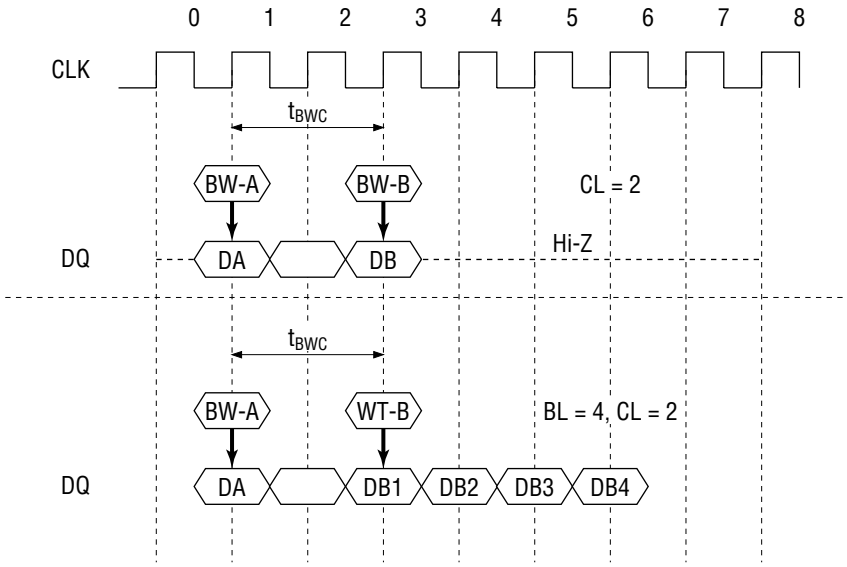
Write to Write Command Interval



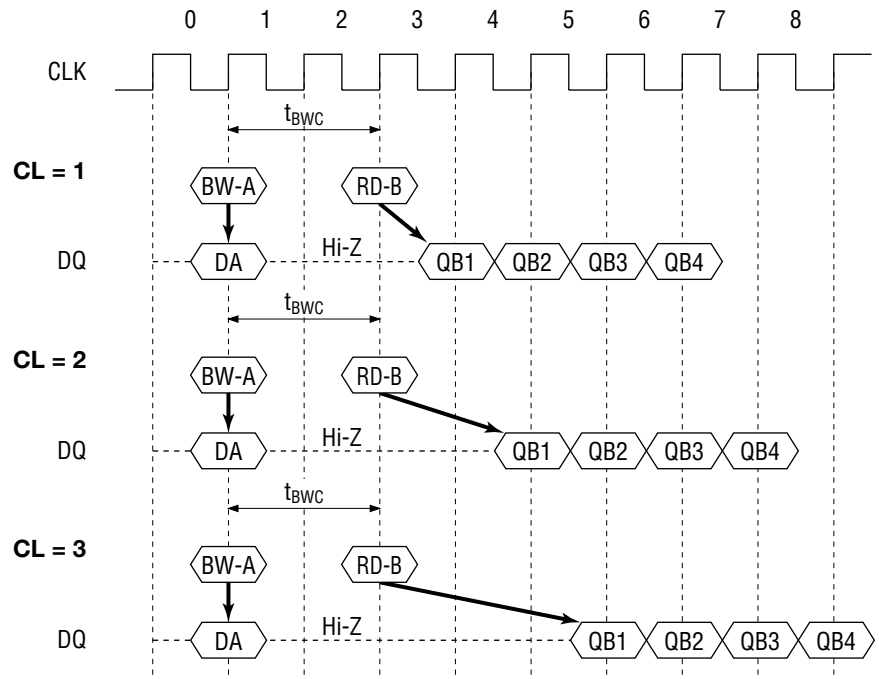
Write to Read Command Interval



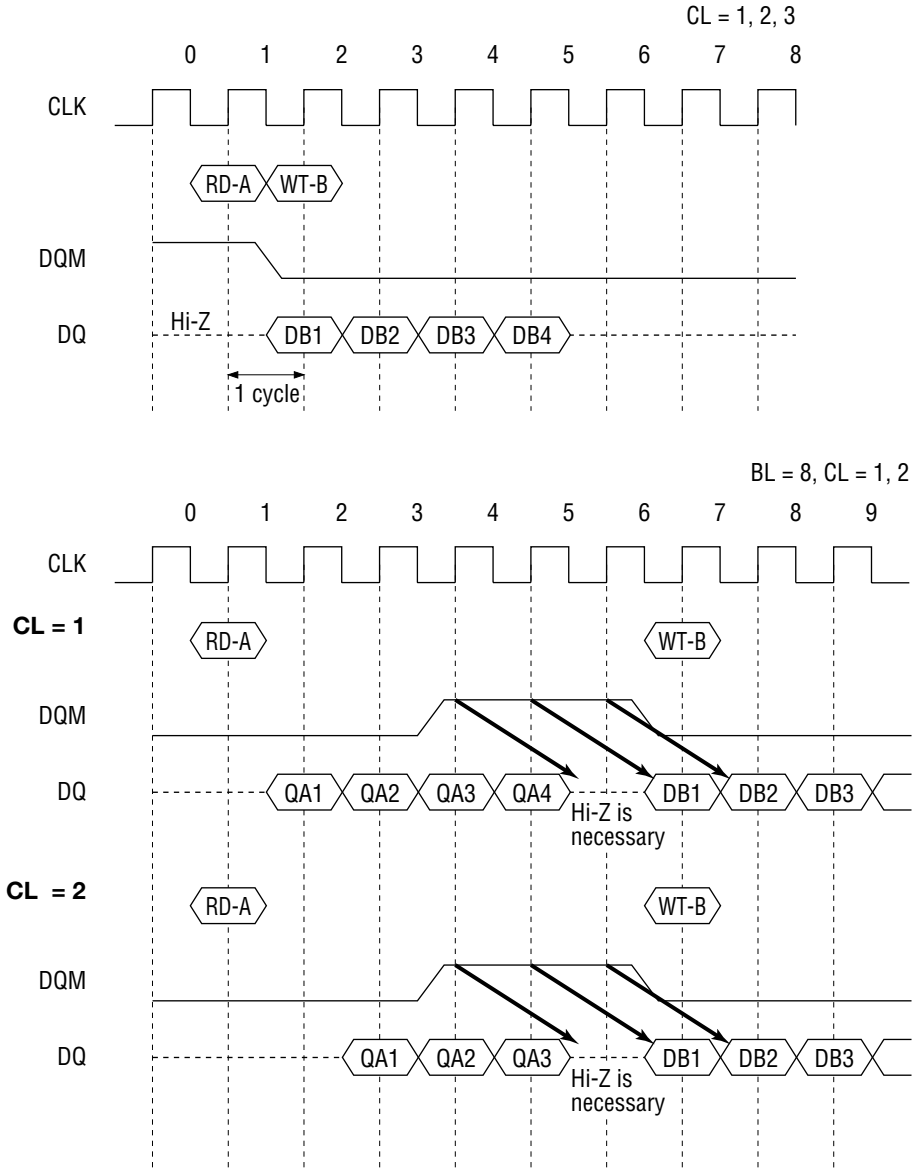
Block Write to Write/Block Write Command Interval

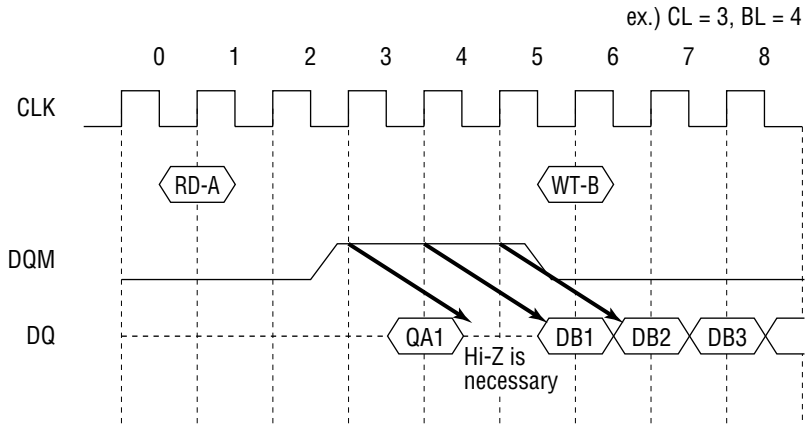


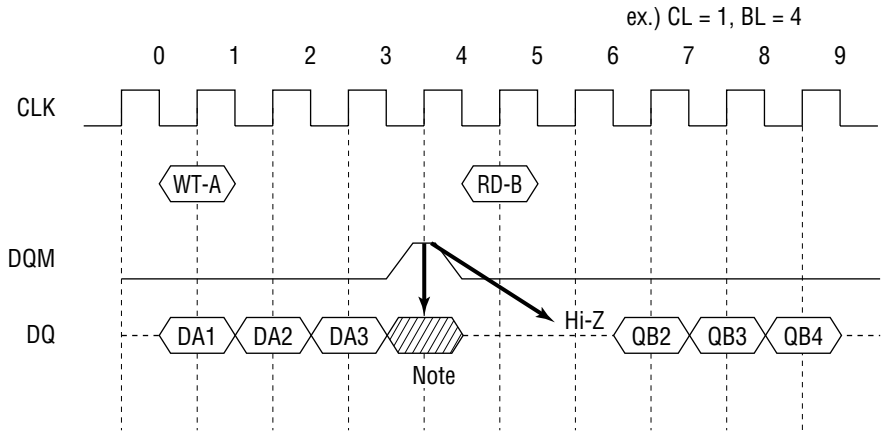
Block Write to Read Command Interval



Read to Write/Block Write Command Interval



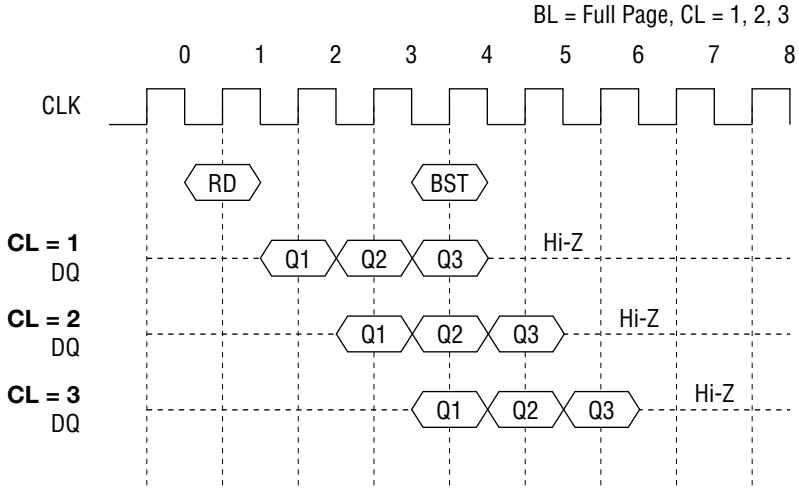


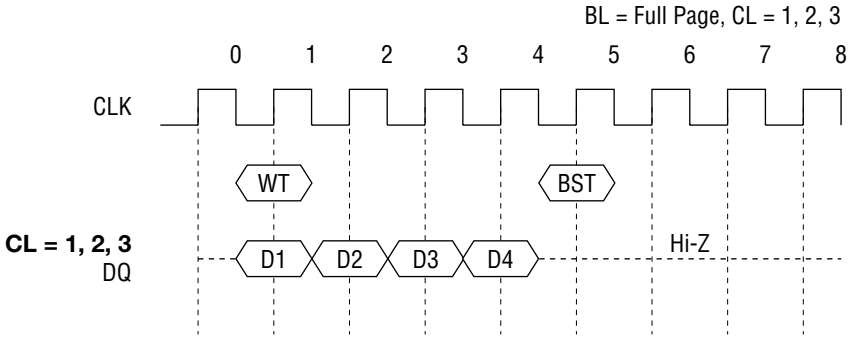


Note : DQM can mask both data-in and data-out in this special case.

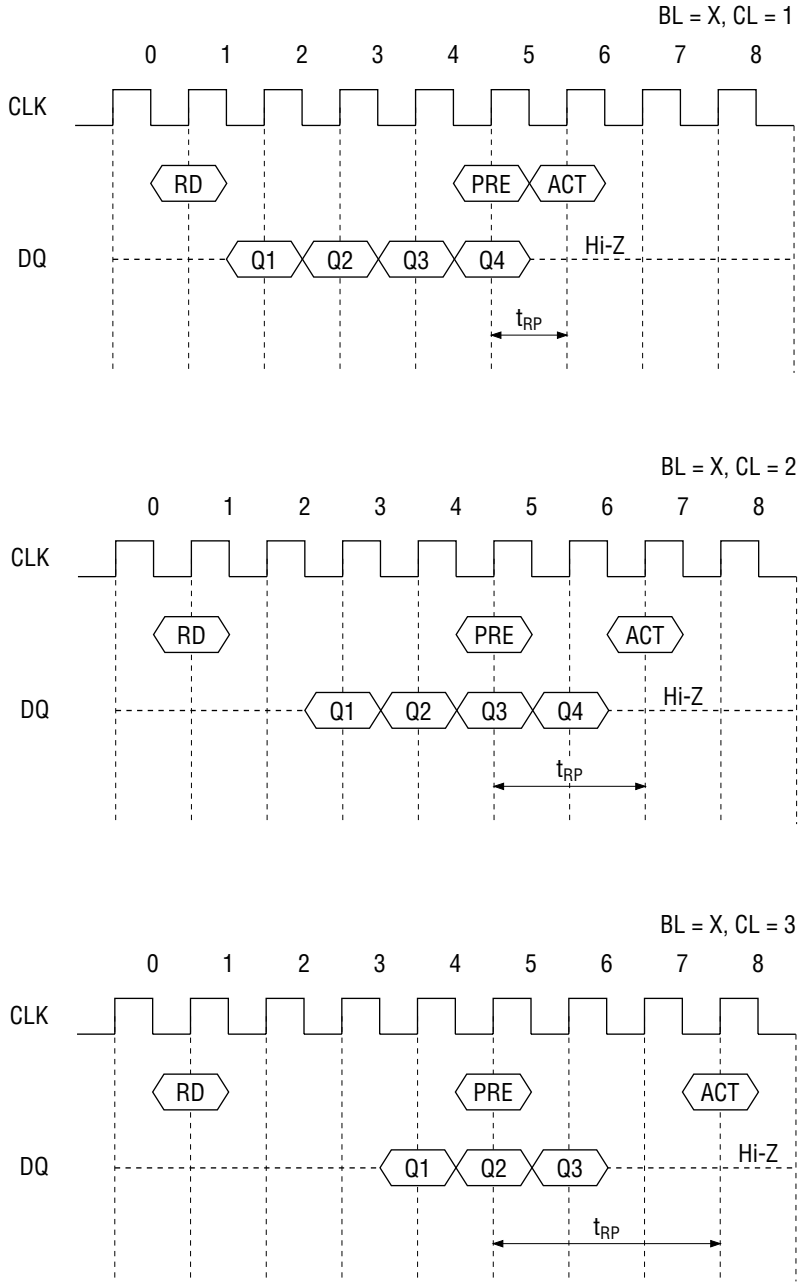
BURST TERMINATION

Burst Stop Command in Full Page

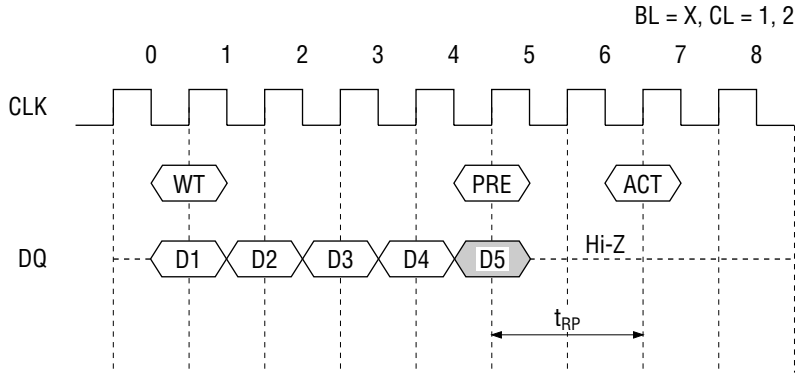




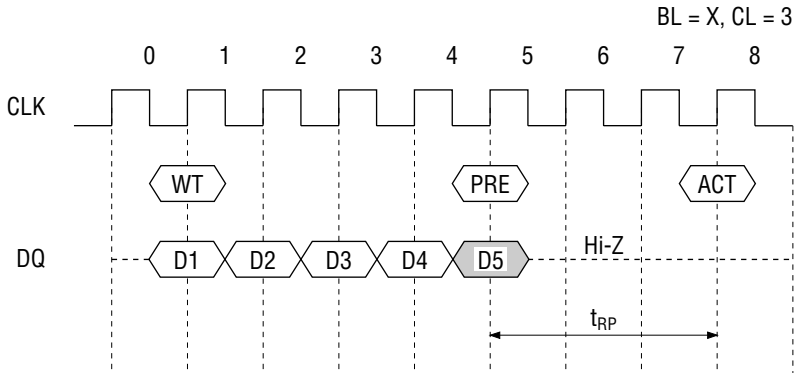
Precharge Termination in READ Cycle



Precharge Termination in WRITE Cycle



Note : D5 data will not be written



Note : D5 data will not be written

ELECTRICAL CHARACTERISTICS

Note : All voltages are referenced to V_{SS}.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Power Supply Pin Relative to GND	V_{CC}, $V_{CC}Q$	—	–1.0 to 4.6	V
Voltage on Input Pin Relative to GND	V_T	—	–1.0 to V_{CC} + 0.5 ≤ 4.6	V
Short Circuit Output Current	I_{OS}	—	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–55 to 150	°C

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Capacitance

(V_{CC} = 3.3 V ±0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 - A9)	C_{I1}	—	6	pF
Input Capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM)	C_{I2}	—	6	pF
Input/Output Capacitance (DQ0 - DQ31)	$C_{I/O}$	—	7	pF

DC Characteristics 1

Parameter	Symbol	Test Condition	Min.	Max.	Unit
Output High Voltage	V_{OH}	I_{OH} = –2 mA	2.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA	—	0.4	V
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 3.6 V; All other pins not under test = 0 V	–10	10	µA
Output Leakage Current	I_{LO}	D_{OUT} is disabled, 0 V ≤ V_O ≤ 3.6 V	–10	10	µA

DC Characteristics 2

Parameter	Symbol	Test Condition		-10 Max.	-12 Max.	Unit	Note
Operating Current	I_{CC1}	Burst length = 1, $t_{RAS} \geq t_{RAS\ (MIN.)}$, $t_{RP} \geq t_{RP\ (MIN.)}$, I_O = 0 mA		175	155	mA	1
Precharge Standby Current in Power Down Mode	$I_{CC2}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns		4	4	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞		3	3		
Precharge Standby Current in Non Power Down Mode	$I_{CC2}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, $\overline{CS} \geq V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.		60	60	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞, Input signals are stable.		30	30		
Active Standby Current in Power Down Mode	$I_{CC3}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns		4	4	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞		3	3		
Active Standby Current in Non Power Down Mode	$I_{CC3}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, $\overline{CS} \geq V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.		70	70	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞, Input signals are stable.		35	35		
Operating Current (Burst Mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, I_O = 0 mA	$\overline{CAS}$ Latency = 1	130	120	mA	2
			$\overline{CAS}$ Latency = 2	180	170		
			$\overline{CAS}$ Latency = 3	240	230		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC\ (MIN.)}$		165	145	mA	3
Self Refresh Current	I_{CC6}	CKE ≤ 0.2 V		3	3	mA	
Operating Current (Block Write Mode)	I_{CC7}	$t_{CK} \geq t_{CK\ (MIN.)}$, I_O = 0 mA, $\overline{CAS}$ cycle = 20 ns		240	240	mA	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

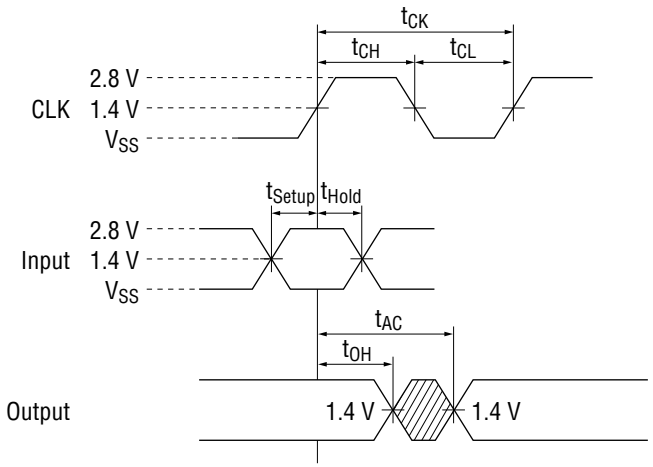
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

AC Characteristics

Test conditions

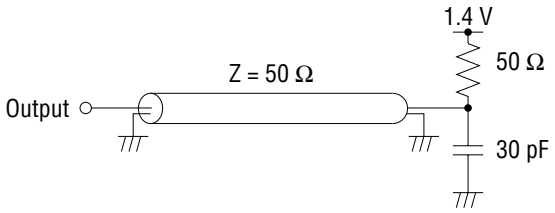
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics

Parameter		Symbol	MSM54V25632A -10		MSM54V25632A -12		Unit	Note
			Min.	Max.	Min.	Max.		
Clock Cycle Time	$\overline{CAS}$ Latency = 3	t_{CK3}	10	(100 MHz)	12	(83 MHz)	ns	
	$\overline{CAS}$ Latency = 2	t_{CK2}	15	(66 MHz)	18	(55 MHz)	ns	
	$\overline{CAS}$ Latency = 1	t_{CK1}	30	(33 MHz)	36	(28 MHz)	ns	
Access Time from CLK	$\overline{CAS}$ Latency = 3	t_{AC3}	—	9	—	10	ns	1
	$\overline{CAS}$ Latency = 2	t_{AC2}	—	13	—	15	ns	1
	$\overline{CAS}$ Latency = 1	t_{AC1}	—	27	—	32	ns	1
CLK High Level Width		t_{CH}	3.5	—	4	—	ns	
CLK Low Level Width		t_{CL}	3.5	—	4	—	ns	
Data-out Hold Time		t_{OH}	3	—	3	—	ns	
Data-out Low-impedance Time		t_{LZ}	0	—	0	—	ns	
Data-out High-impedance Time	$\overline{CAS}$ Latency = 3	t_{HZ3}	3	8	3	8	ns	
	$\overline{CAS}$ Latency = 2	t_{HZ2}	3	12	3	12	ns	
	$\overline{CAS}$ Latency = 1	t_{HZ1}	3	26	3	26	ns	
Data-in Setup Time		t_{DS}	3	—	3.5	—	ns	
Data-in Hold Time		t_{DH}	1	—	1.5	—	ns	
Address Setup Time		t_{AS}	3	—	3.5	—	ns	
Address Hold Time		t_{AH}	1	—	1.5	—	ns	
CKE Setup Time		t_{CKS}	3	—	3.5	—	ns	
CKE Hold Time		t_{CKH}	1	—	1.5	—	ns	
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM) Setup Time		t_{CMS}	3	—	3.5	—	ns	
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM) Hold Time		t_{CMH}	1	—	1.5	—	ns	

Note 1. Output load.

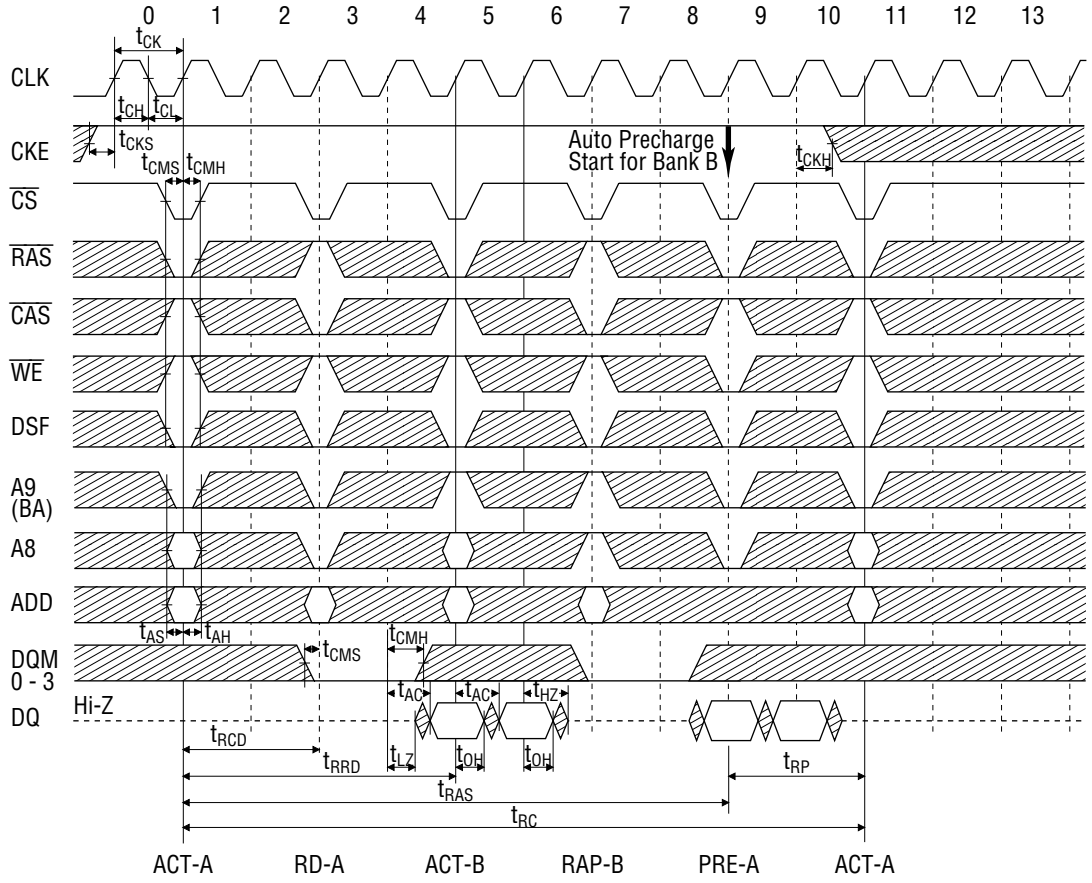


Asynchronous Characteristics

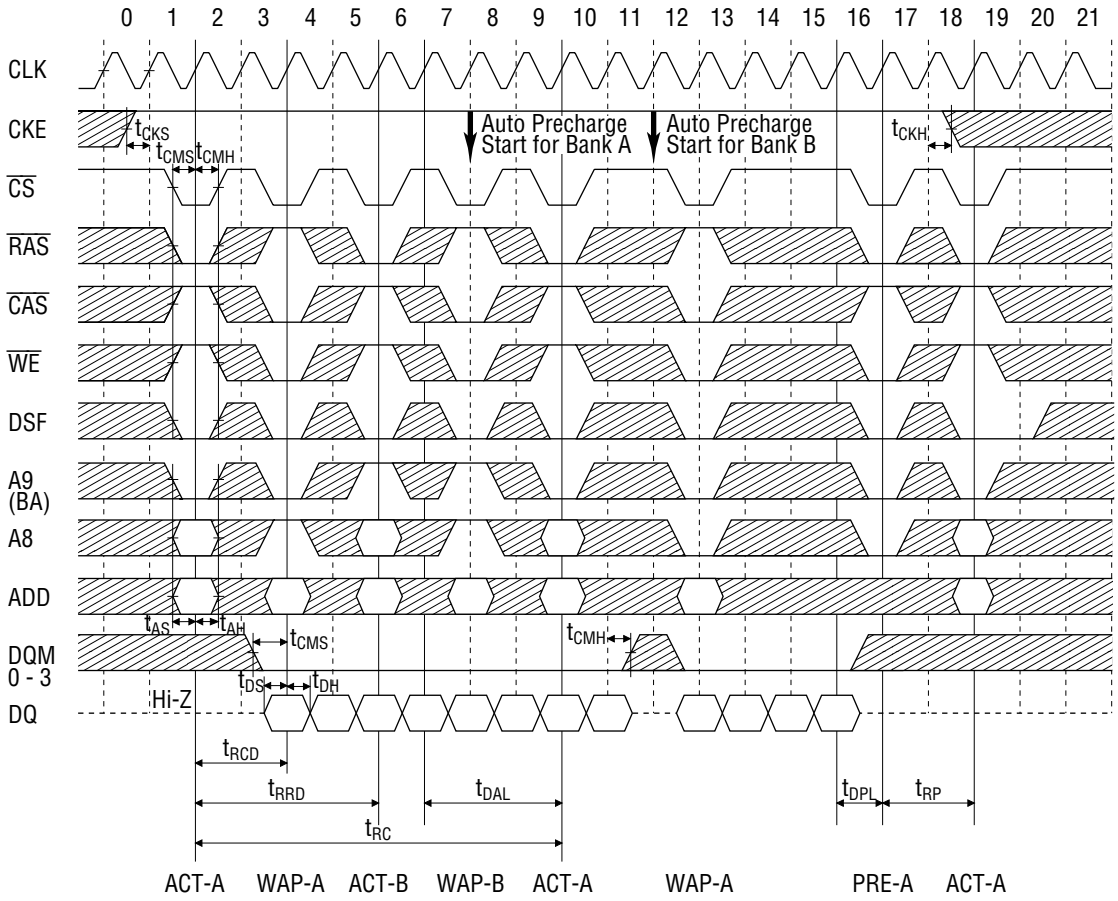
Parameter		Symbol	MSM54V25632A -10		MSM54V25632A -12		Unit	Note
			Min.	Max.	Min.	Max.		
REF to REF/ACT Command Period		t_{RC}	90	—	108	—	ns	
ACT to PRE Command Period		t_{RAS}	60	120,000	72	120,000	ns	
PRE to ACT Command Period		t_{RP}	30	—	36	—	ns	
Delay Time ACT to READ/WRITE Command		t_{RCD}	30	—	36	—	ns	
ACT (0) to ACT (1) Command Period		t_{RRD}	20	—	24	—	ns	
Data-in to PRE Command Period	$\overline{CAS}$ Latency = 3	t_{DPL3}	20	—	24	—	ns	
	$\overline{CAS}$ Latency = 2	t_{DPL2}	20	—	24	—	ns	
	$\overline{CAS}$ Latency = 1	t_{DPL1}	20	—	24	—	ns	
Data-in to ACT (REF) Command Period (Auto Precharge)	$\overline{CAS}$ Latency = 3	t_{DAL3}	5	—	5	—	CLK	
	$\overline{CAS}$ Latency = 2	t_{DAL2}	3	—	3	—	CLK	
	$\overline{CAS}$ Latency = 1	t_{DAL1}	2	—	2	—	CLK	
Block Write Cycle Time		t_{BWC}	20	—	24	—	ns	
Block Write Data-in to PRE Command Period	$\overline{CAS}$ Latency = 3	t_{BPL3}	30	—	36	—	ns	
	$\overline{CAS}$ Latency = 2	t_{BPL2}	30	—	36	—	ns	
	$\overline{CAS}$ Latency = 1	t_{BPL1}	30	—	36	—	ns	
Block Write Data-in Active (REF) Command Period (Auto Precharge)	$\overline{CAS}$ Latency = 3	t_{BAL3}	6	—	6	—	CLK	
	$\overline{CAS}$ Latency = 2	t_{BAL2}	4	—	4	—	CLK	
	$\overline{CAS}$ Latency = 1	t_{BAL1}	2	—	2	—	CLK	
Mode Register Set Cycle Time		t_{RSC}	20	—	20	—	ns	
CKE Setup Time (Precharge Power Down Exit)		t_{PDE}	8	—	10	—	ns	
Transition Time		t_T	1	30	1	30	ns	
Refresh Time		t_{REF}	—	16	—	16	ms	

TIMING WAVEFORM

AC Parameters for Read Timing (BL = 2, CL = 2)



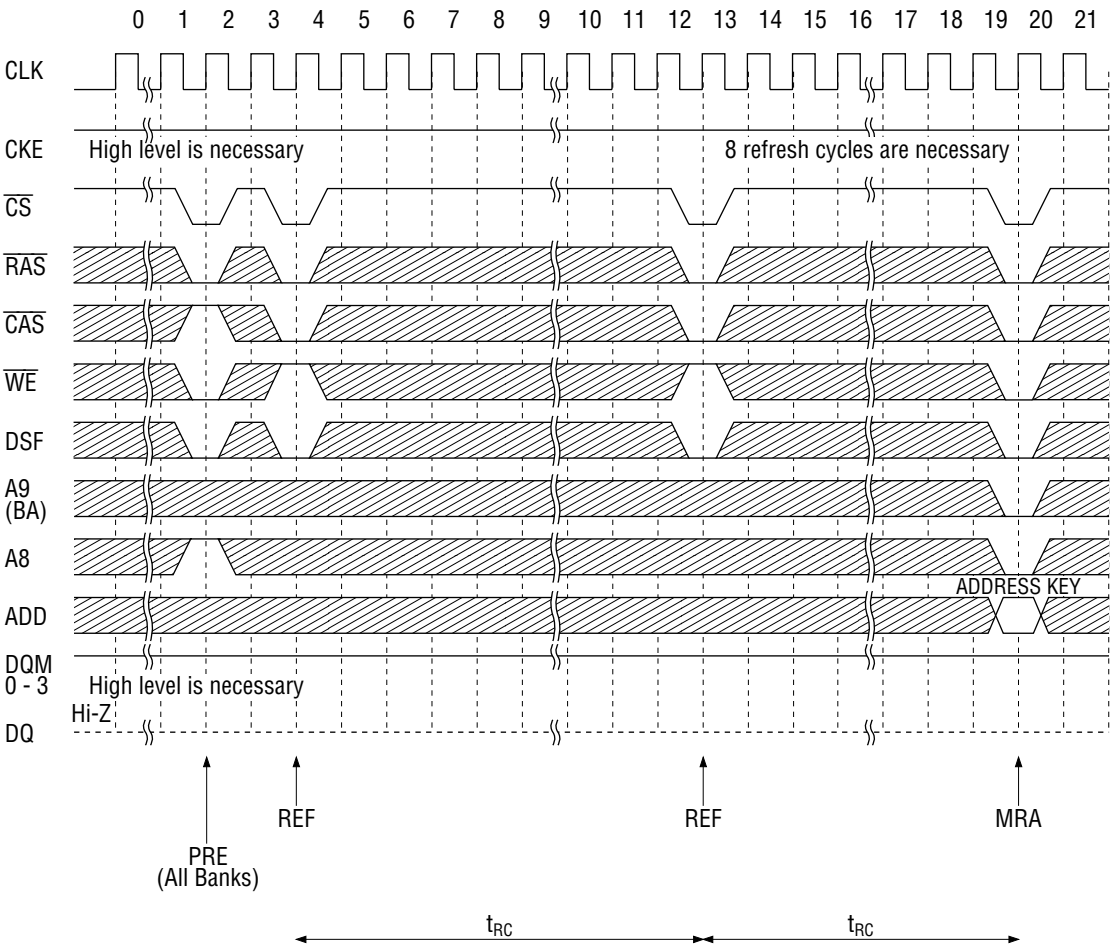
AC Parameters for Write Timing (BL = 4, CL = 2)



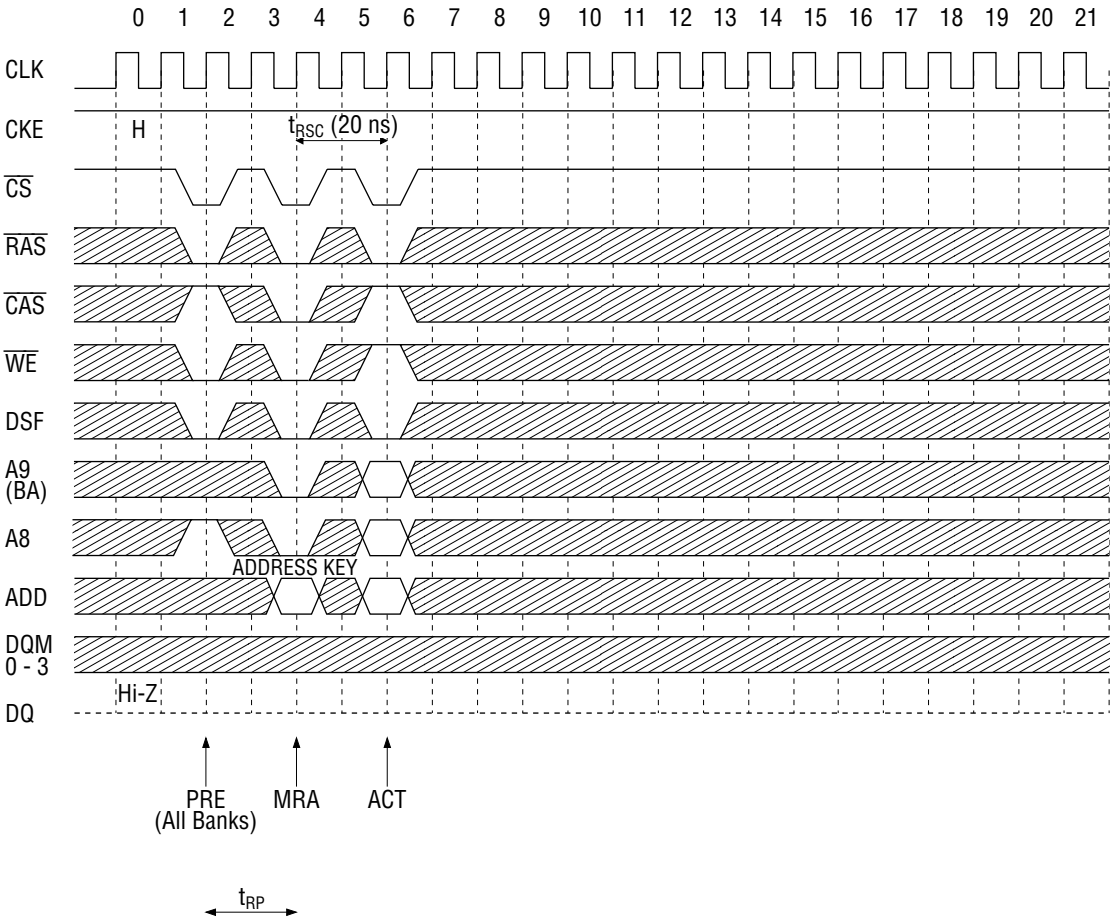
Relationship between Frequency and Latency

Rate	MSM54V25632A-10			MSM54V25632A-12		
Clock Cycle Time [ns]	10	15	30	12	18	36
Frequency [MHz]	100	66	33	83	55	28
$\overline{CAS}$ Latency	3	2	1	3	2	1
[t_{RCD}]	3	2	1	3	2	1
$\overline{RAS}$ Latency ($\overline{CAS}$ Latency + [t_{RCD}])	6	4	2	6	4	2
[t_{RC}]	9	6	3	9	6	3
[t_{RAS}]	6	4	2	6	4	2
[t_{RRD}]	2	2	1	2	2	1
[t_{RP}]	3	2	1	3	2	1
[t_{DPL}]	2	2	1	2	2	1
[t_{DAL}]	5	3	2	5	3	2

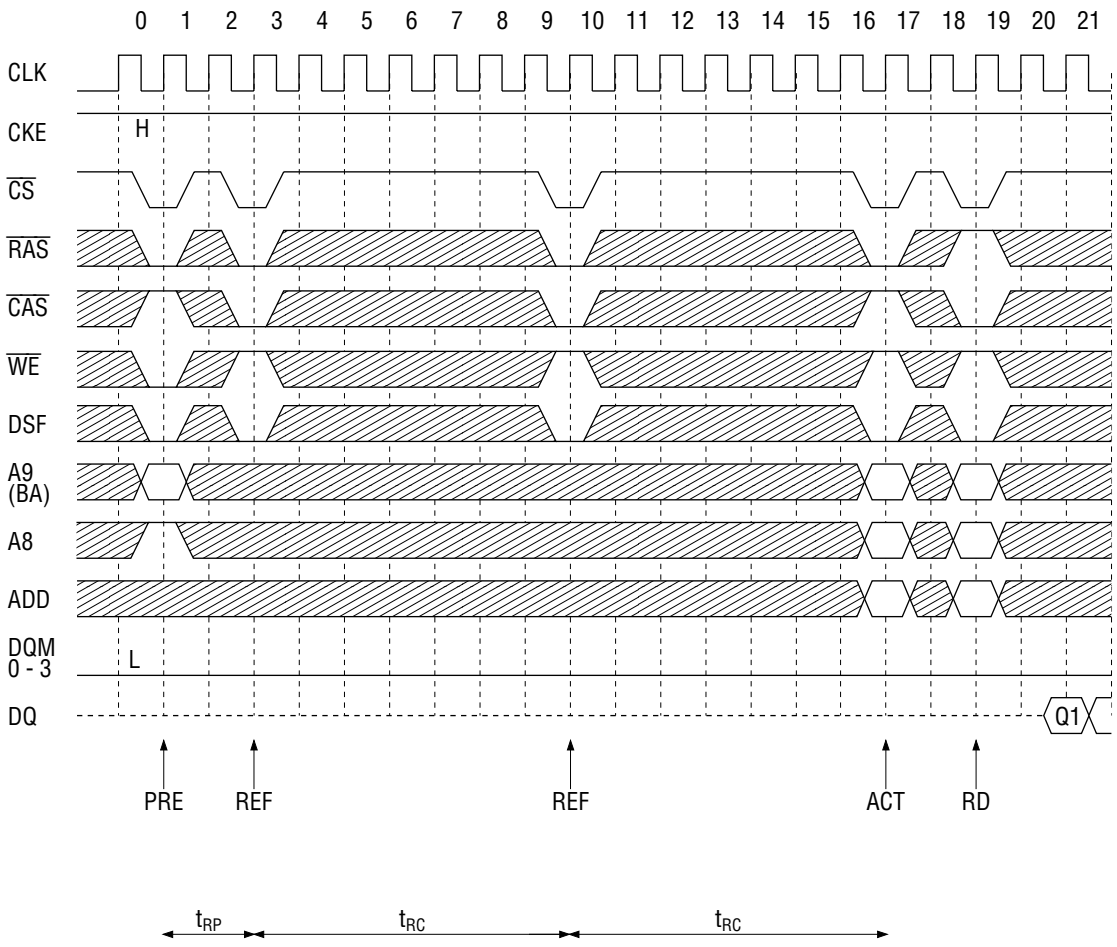
Power on Sequence and Auto Refresh (Initialization)



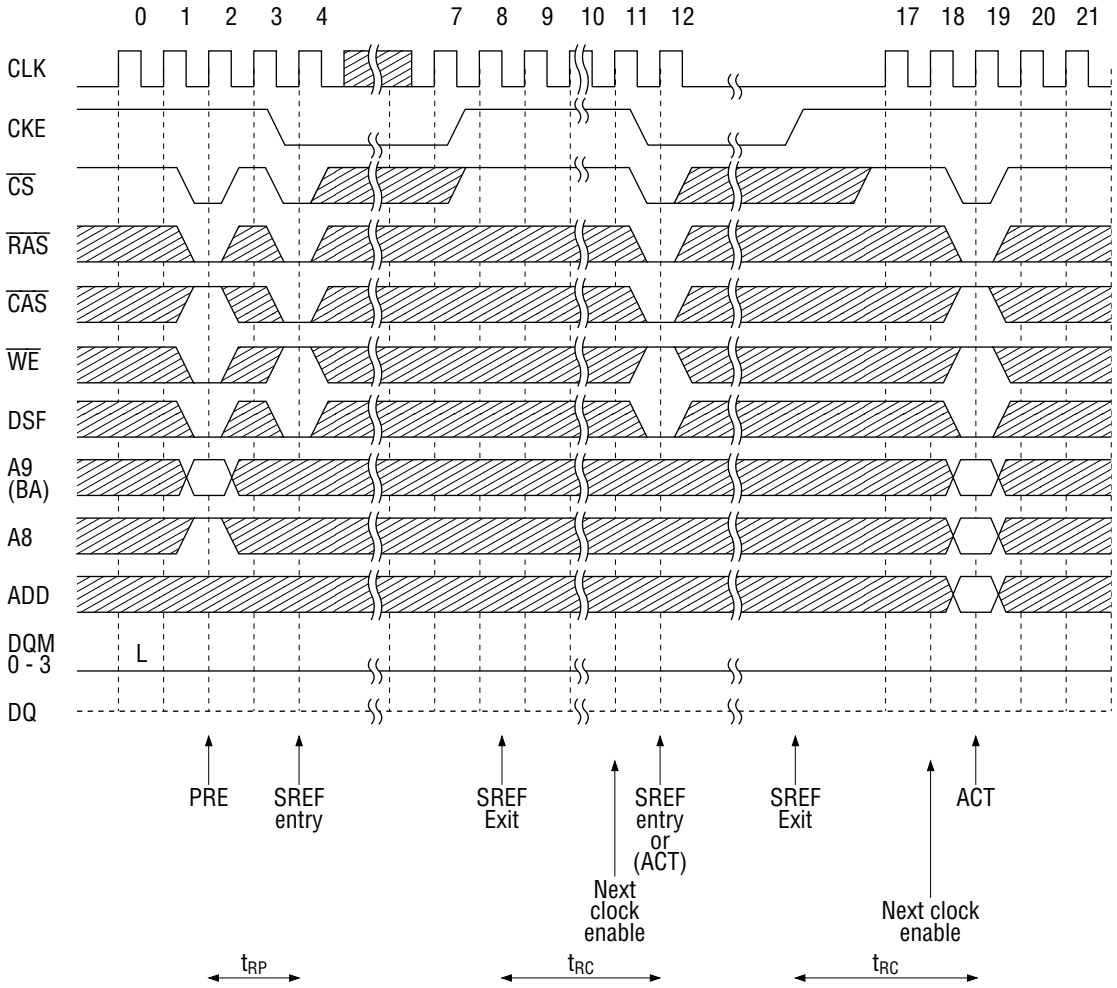
Mode Register Set (BL = 4, CL = 2)



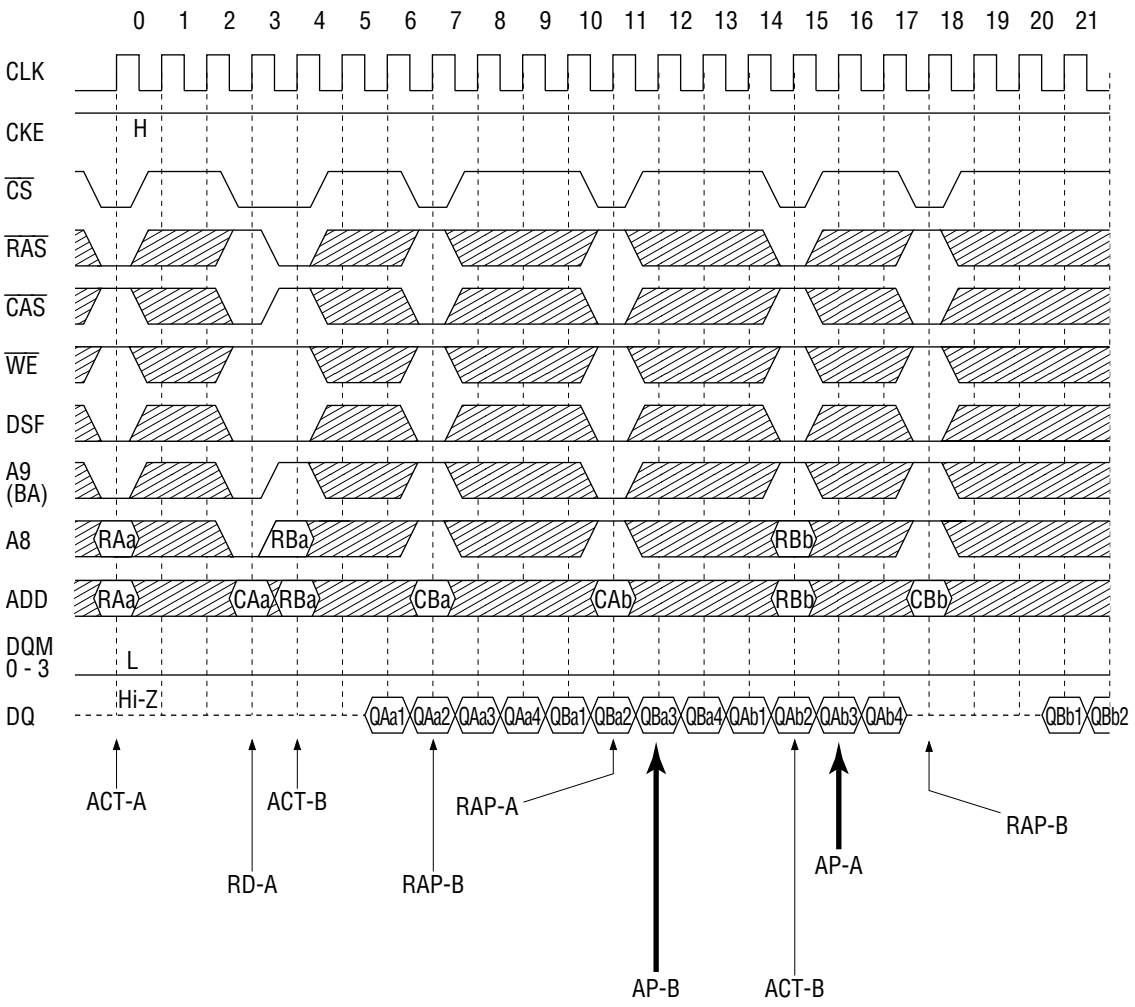
Auto Refresh (CL = 2)



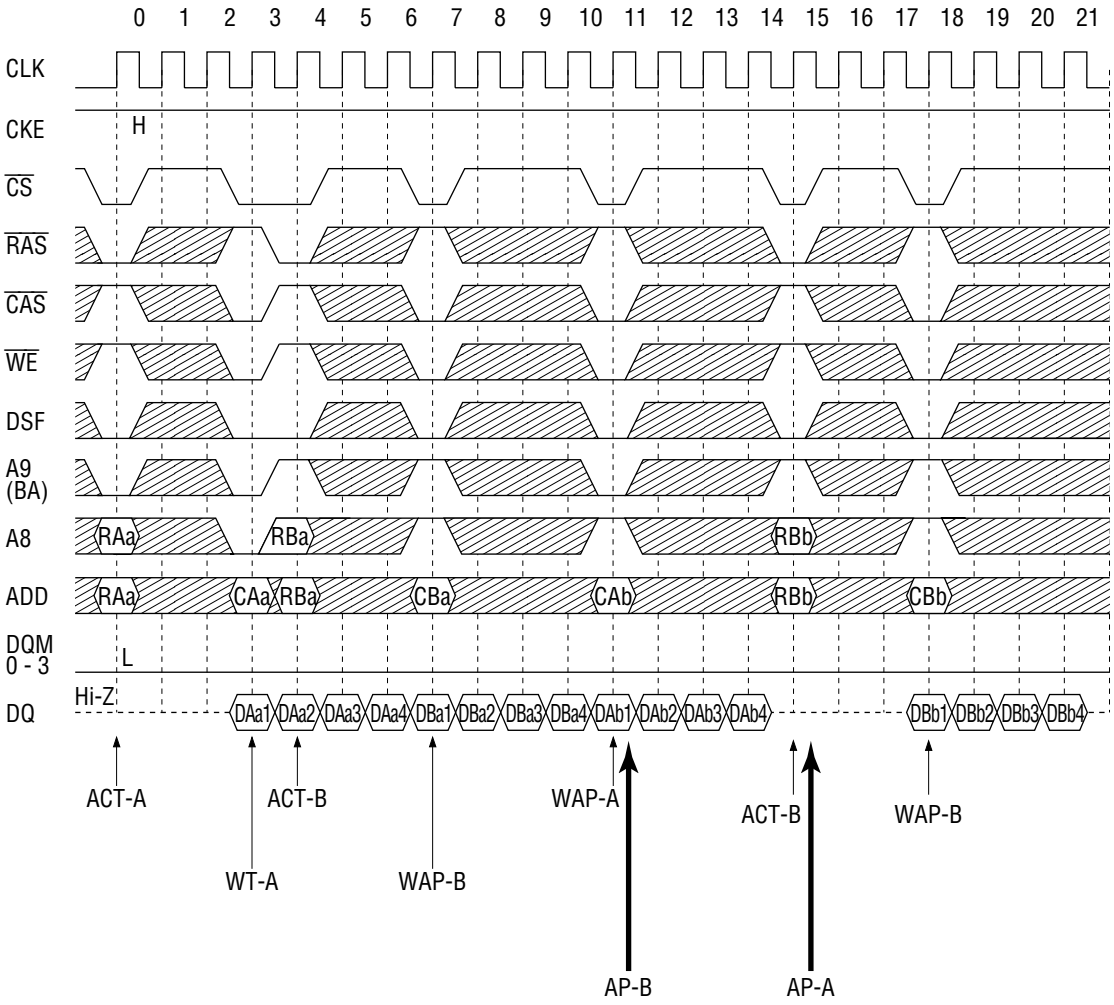
Self Refresh (Entry and Exit)



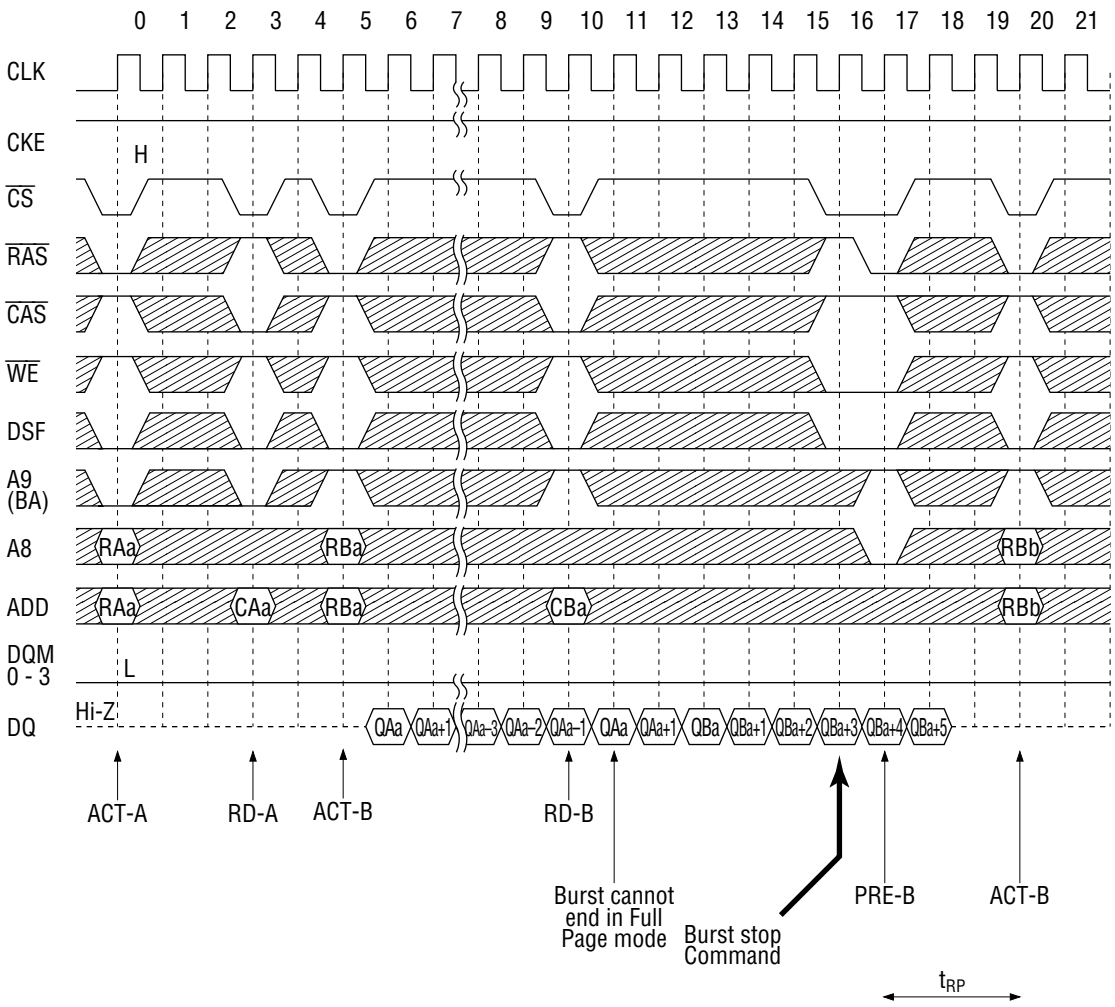
Auto Precharge after Read Burst (BL = 4, CL = 3)



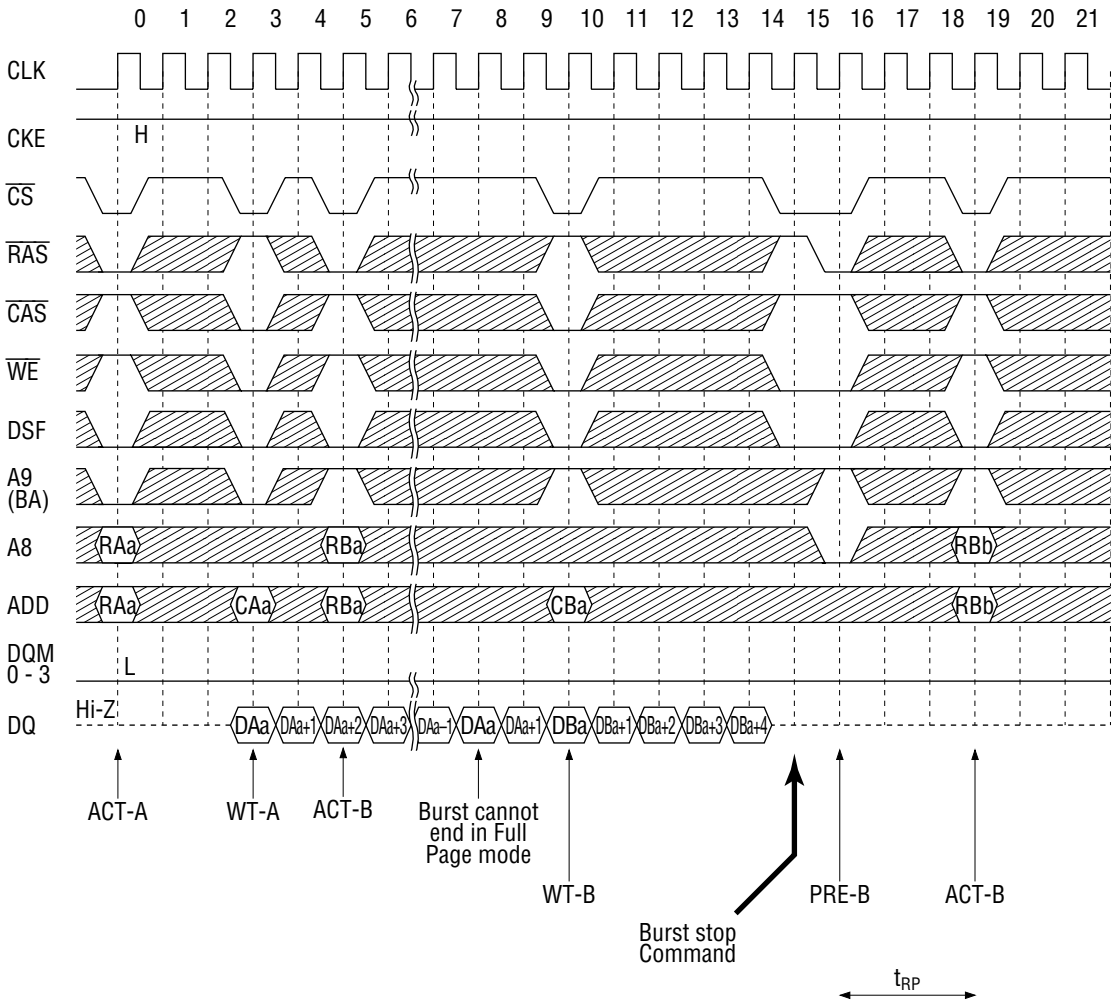
Auto Precharge after Write Burst (BL = 4, CL = 3)



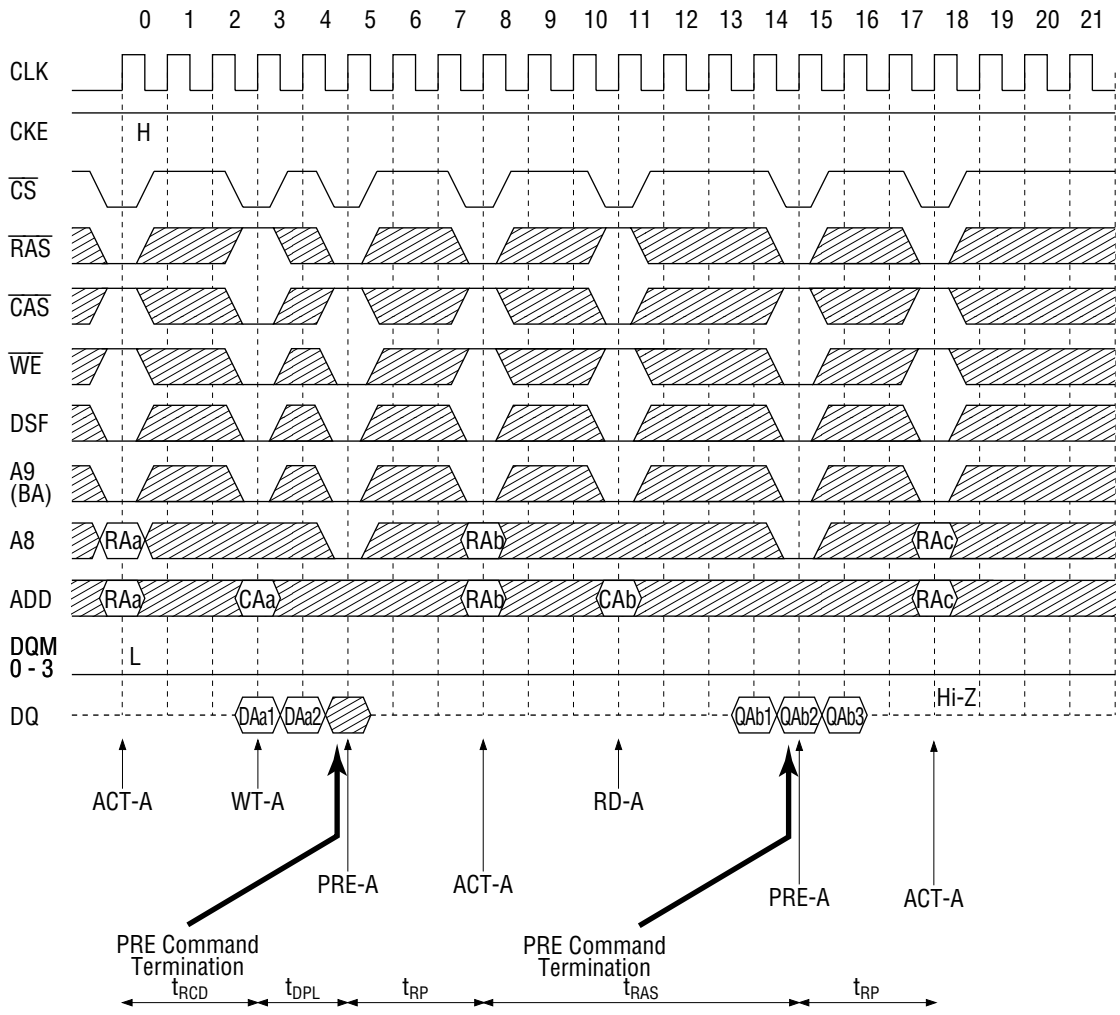
Full Page READ Cycle (CL = 3)



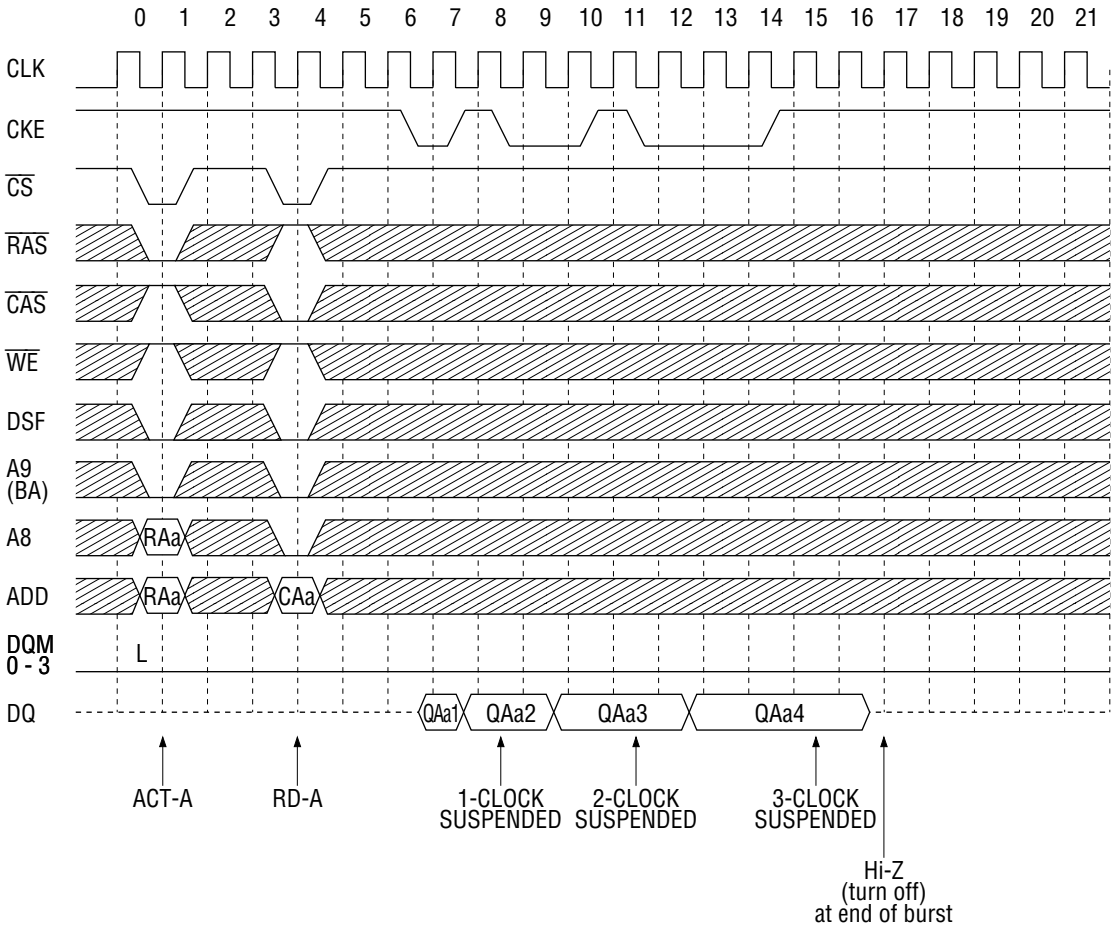
Full Page WRITE Cycle (CL = 3)



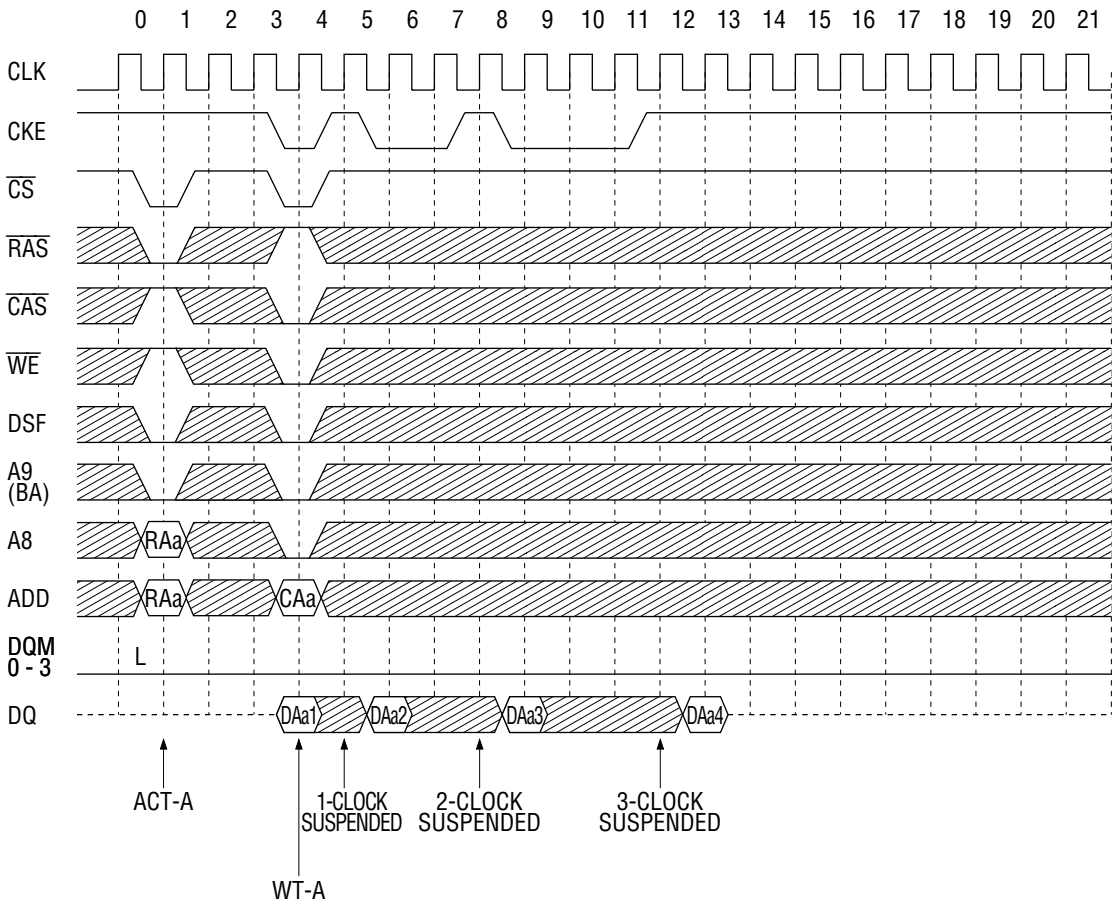
PRE (Precharge) Termination of Burst (BL = 2, 4, 8, Full, CL = 3)



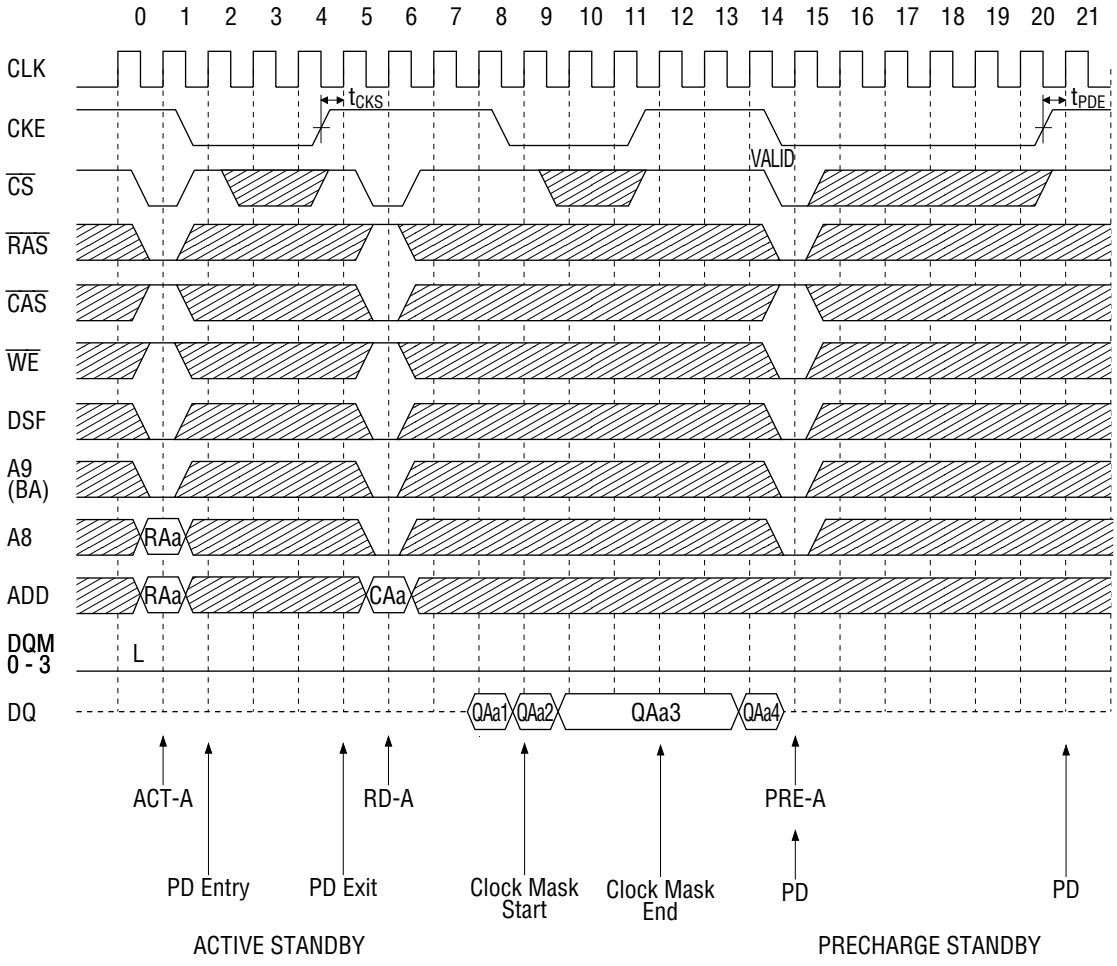
Clock Suspension during Burst Read (using CKE Function) (BL = 4, CL = 3)



Clock Suspension during Burst Write (using CKE Function) (BL = 4, CL = 3)

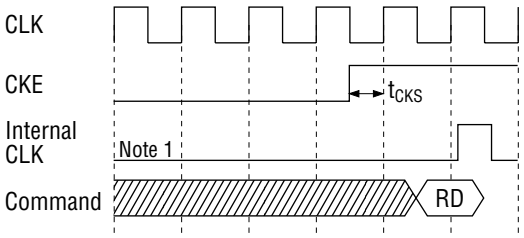


Power Down Mode and Clock Suspension (BL = 4, CL = 2)

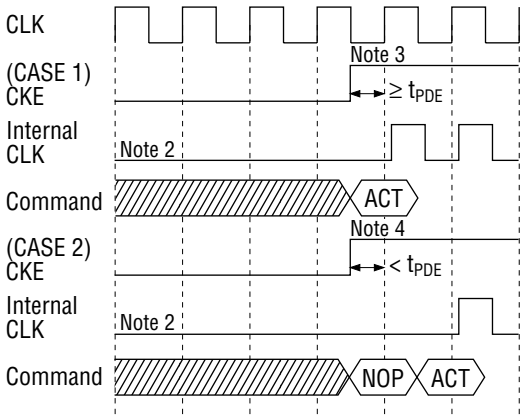


CLOCK Suspend Exit & Power Down Exit

1) Clock Suspend (= Active Power Down) Exit

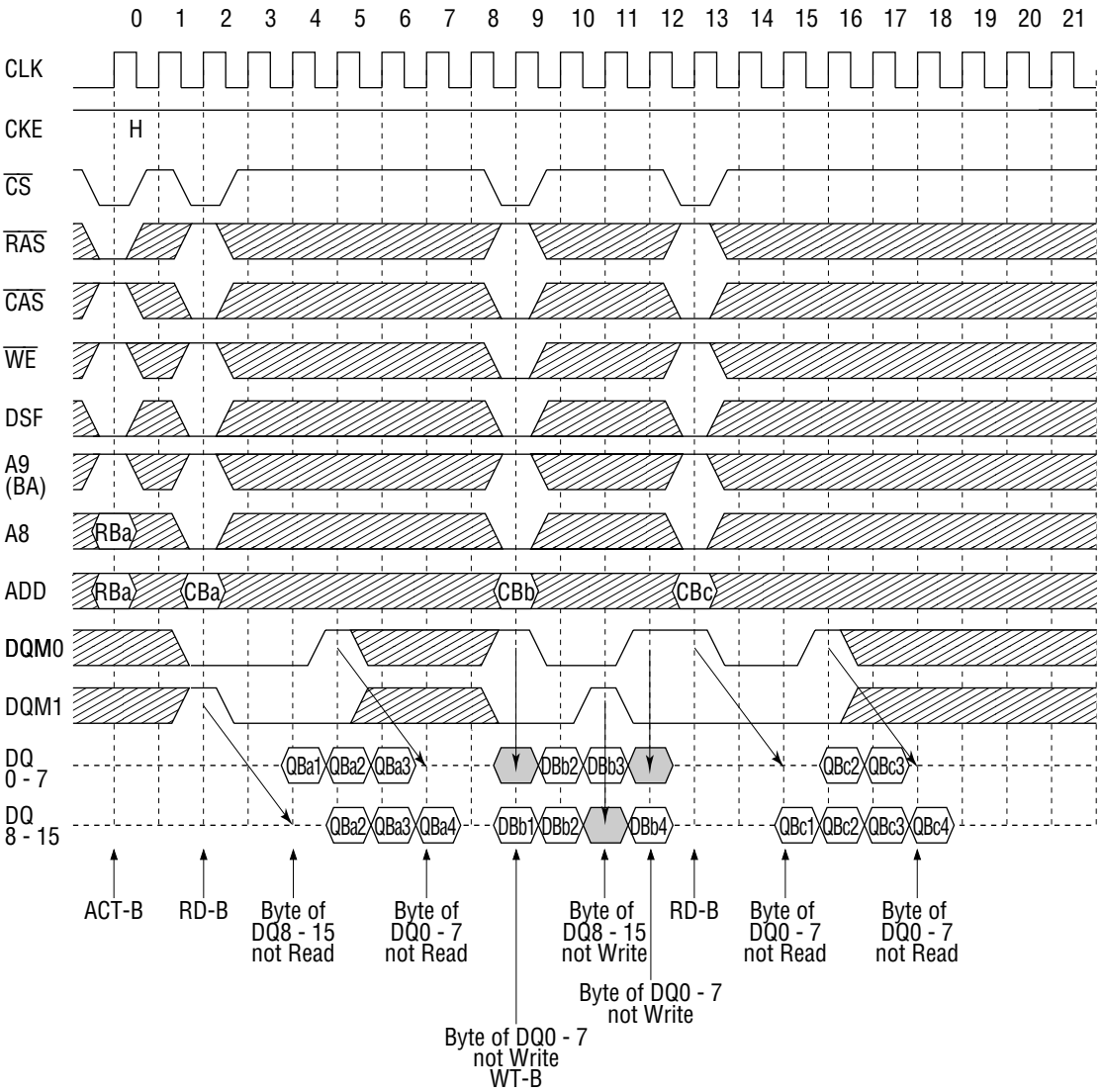


2) Power Down (= Precharge Power Down) Exit

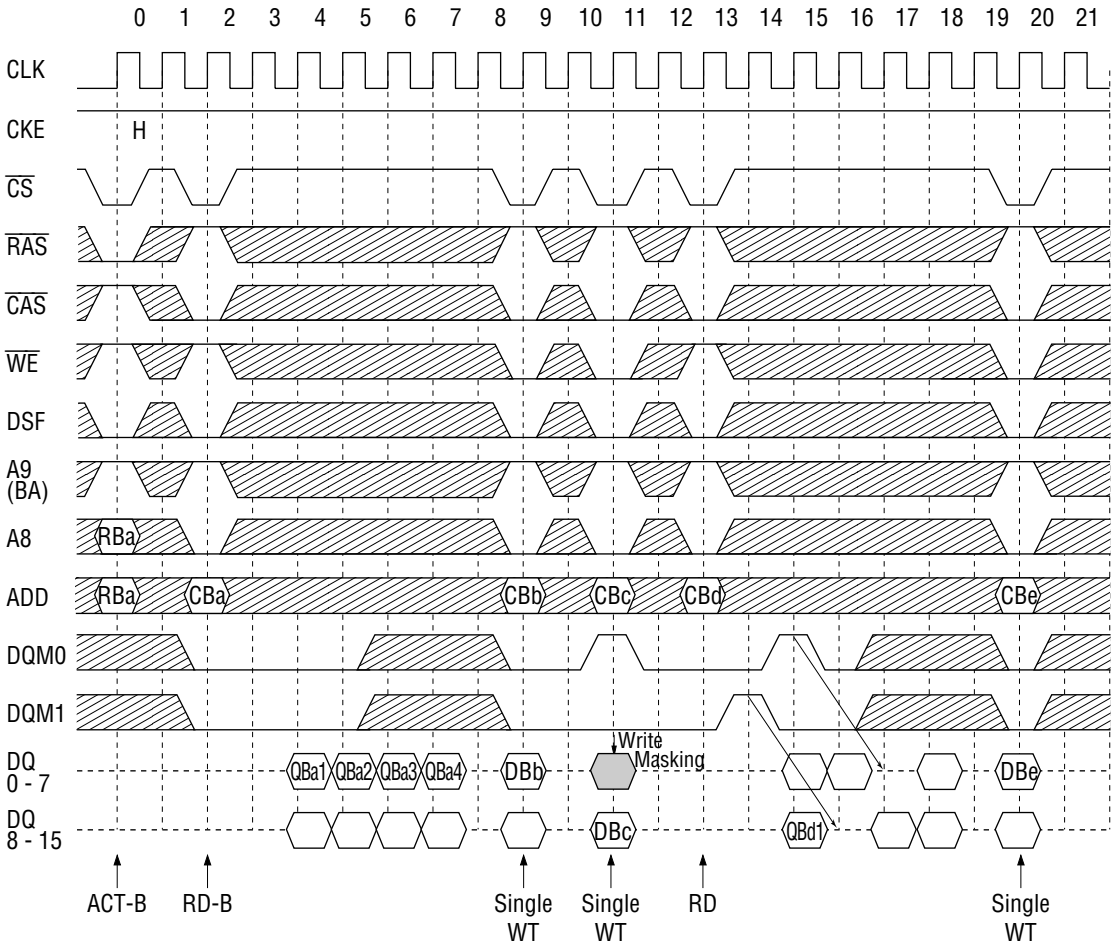


Notes: 1. Active power down: one or both bank active state.
2. Precharge power down: both bank precharge state.
3. t_{PDE}: Asynchronous AC parameter. Time for Power Down Exit Setup Time. Only valid at precharge power down exit.
4. $t_{CKS} < t_{PDE}$, NOP should be issued. And new command can be issued after 1 Clock.

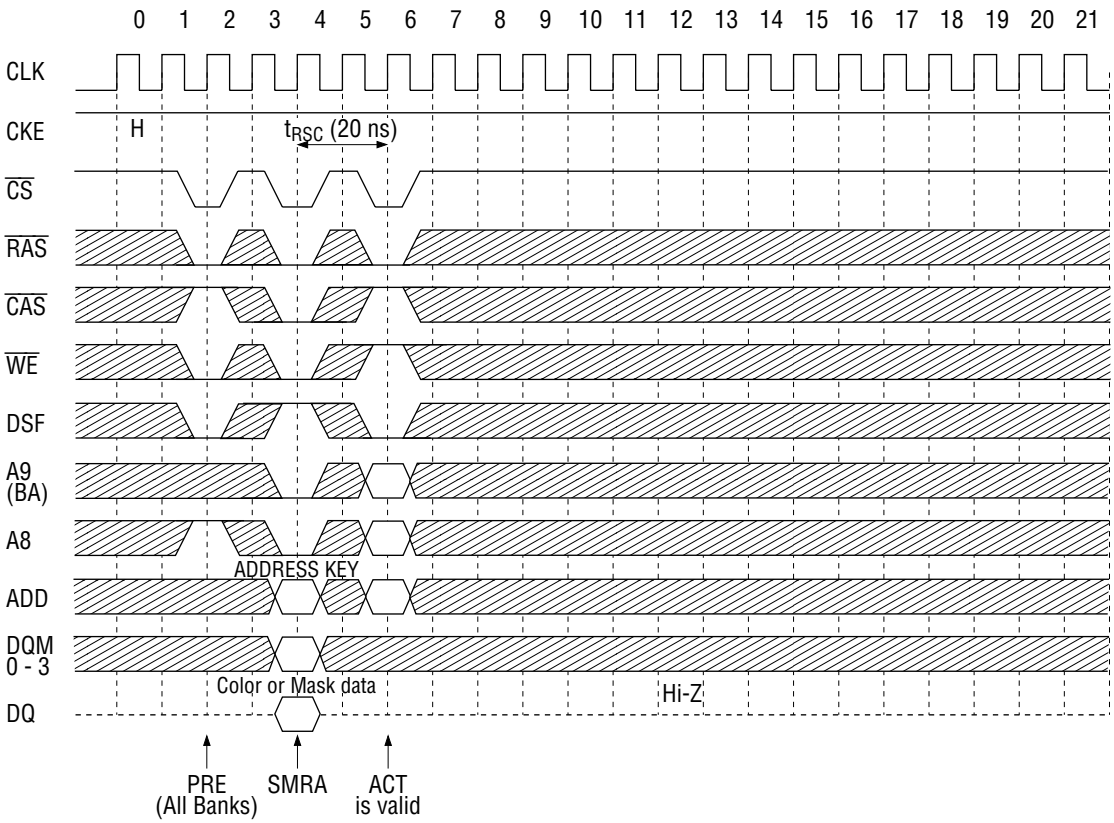
Byte Read/Write Operation (by DQM) (BL = 4, CL = 2)



Burst Read and Single Write (BL = 4, CL = 2)

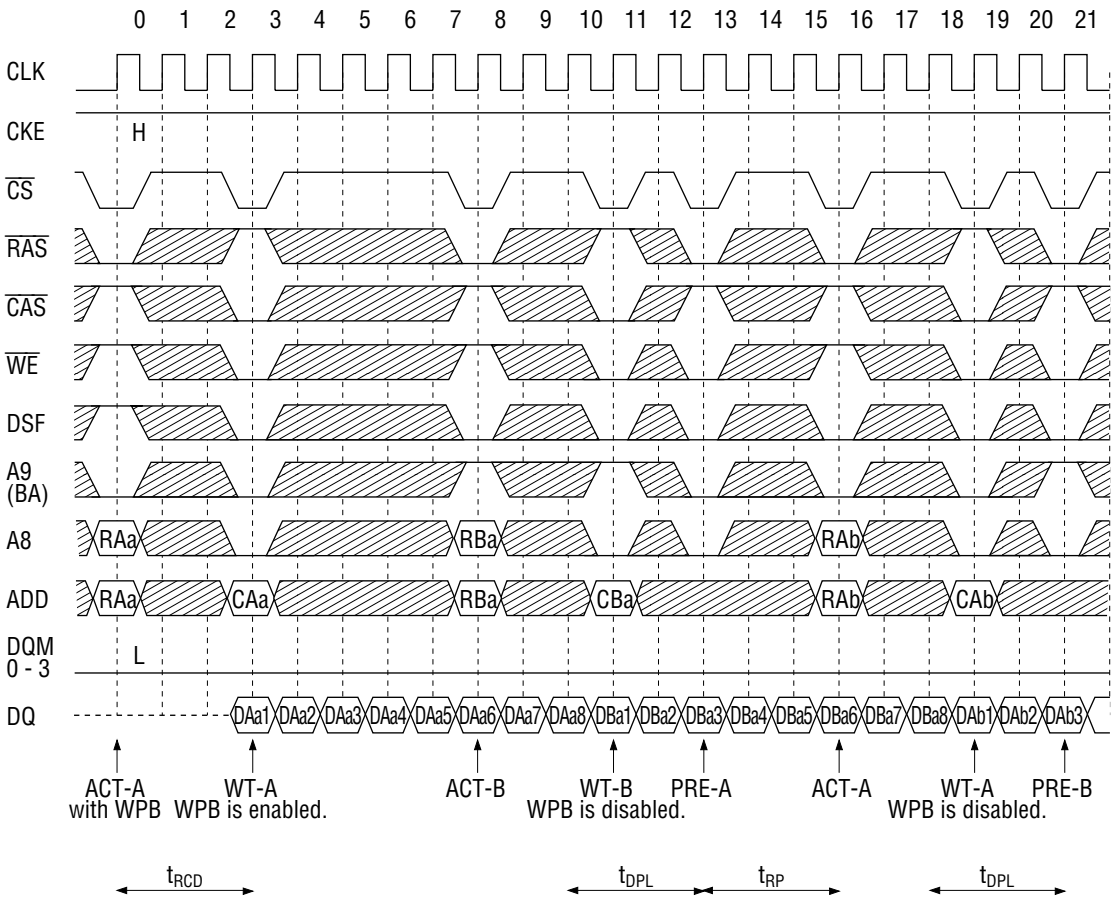


Special Mode Register Set (BL = 4, CL = 2)

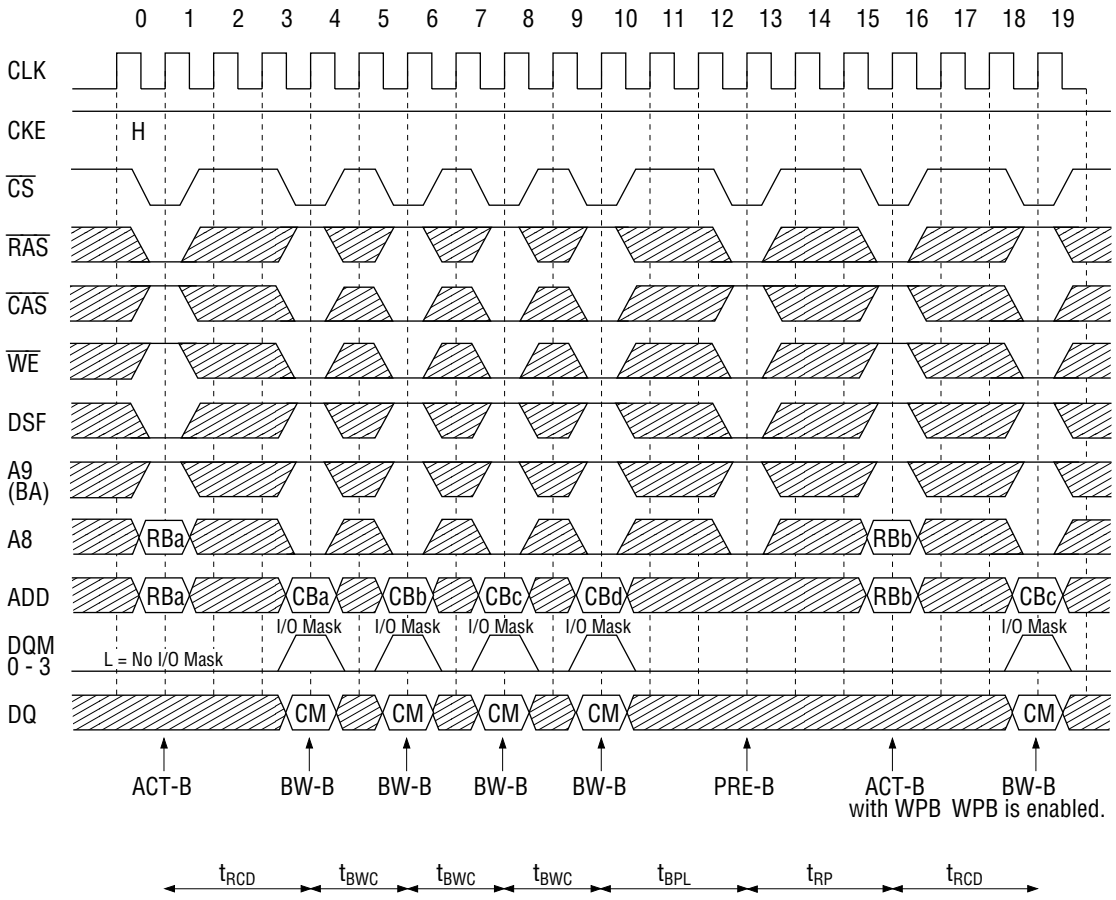


Remark Special Register Set command can be input at any state.

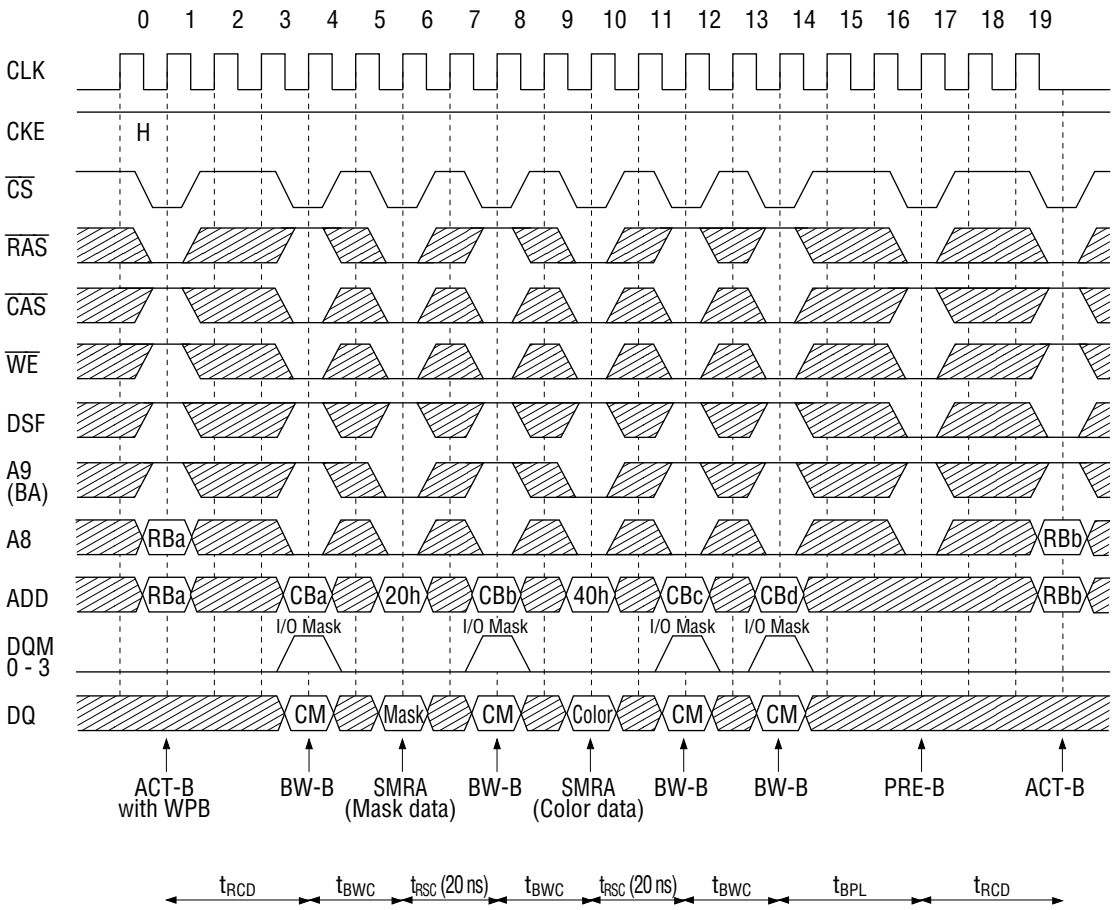
Random Row Write with WPB (BL = 8, CL = 3)



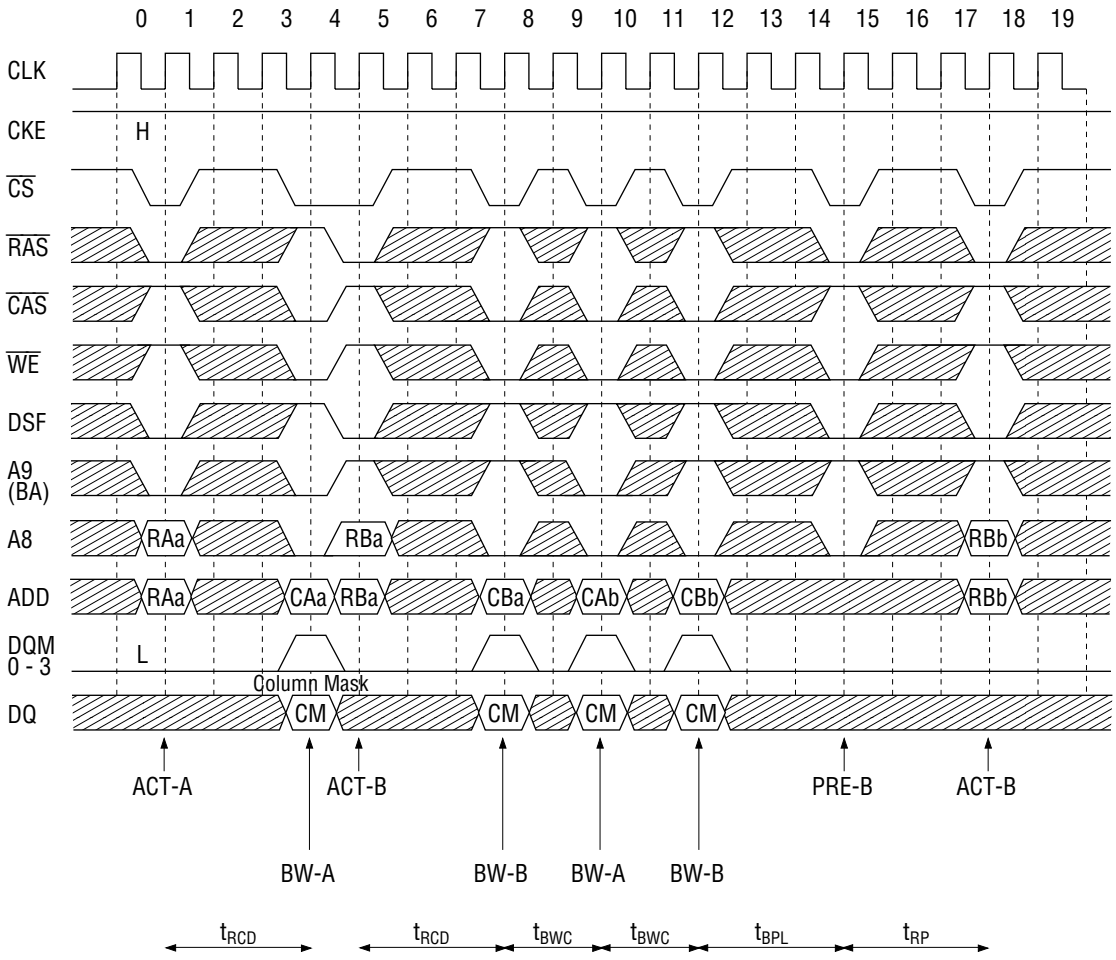
Block Write (Page at Same Bank) (CL = 3)



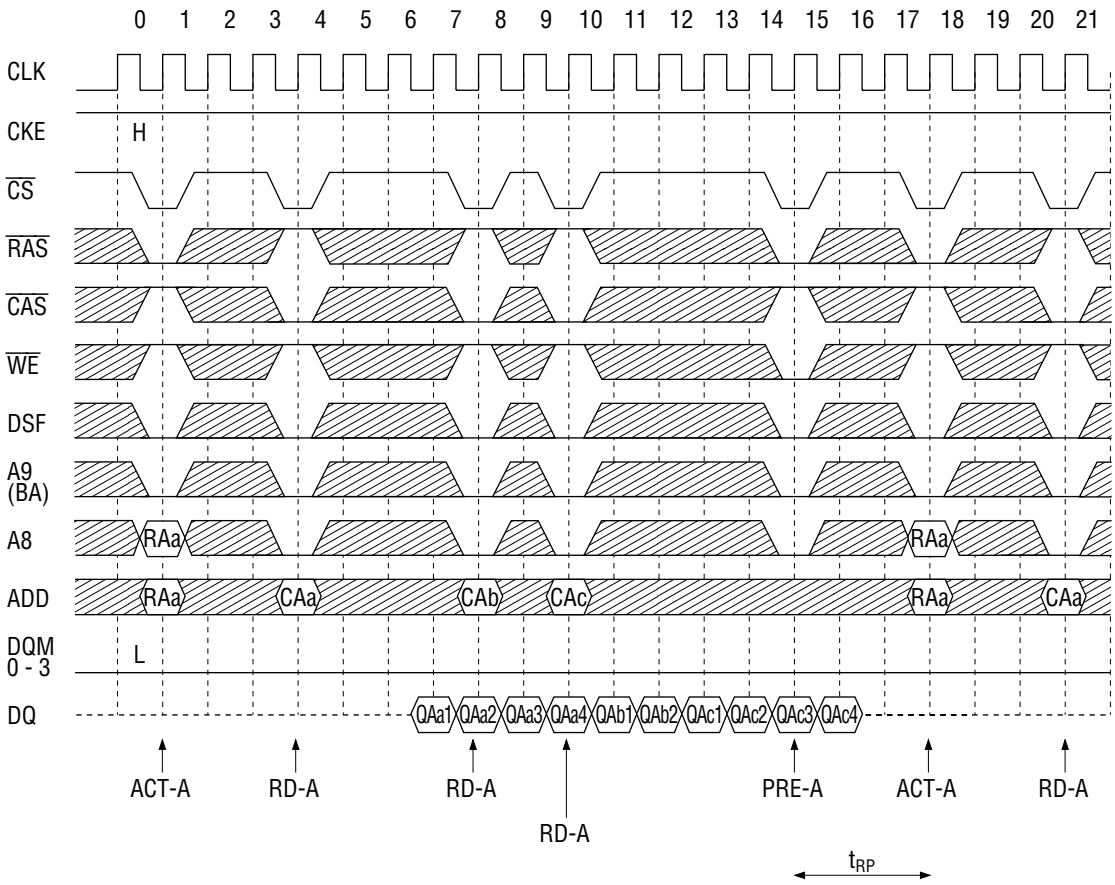
Block Write (Page at Same Bank) Changing Color and Mask Data (CL = 3)



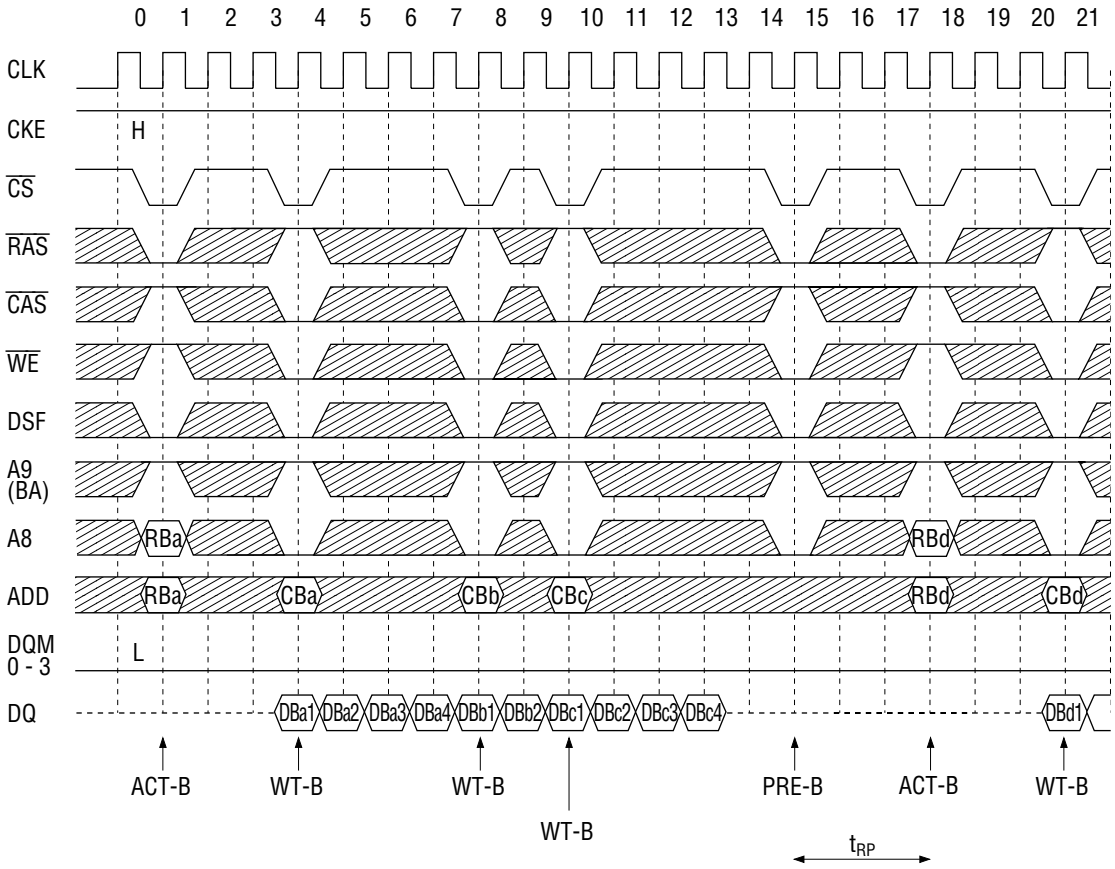
Interleaved Block Write (CL = 3)



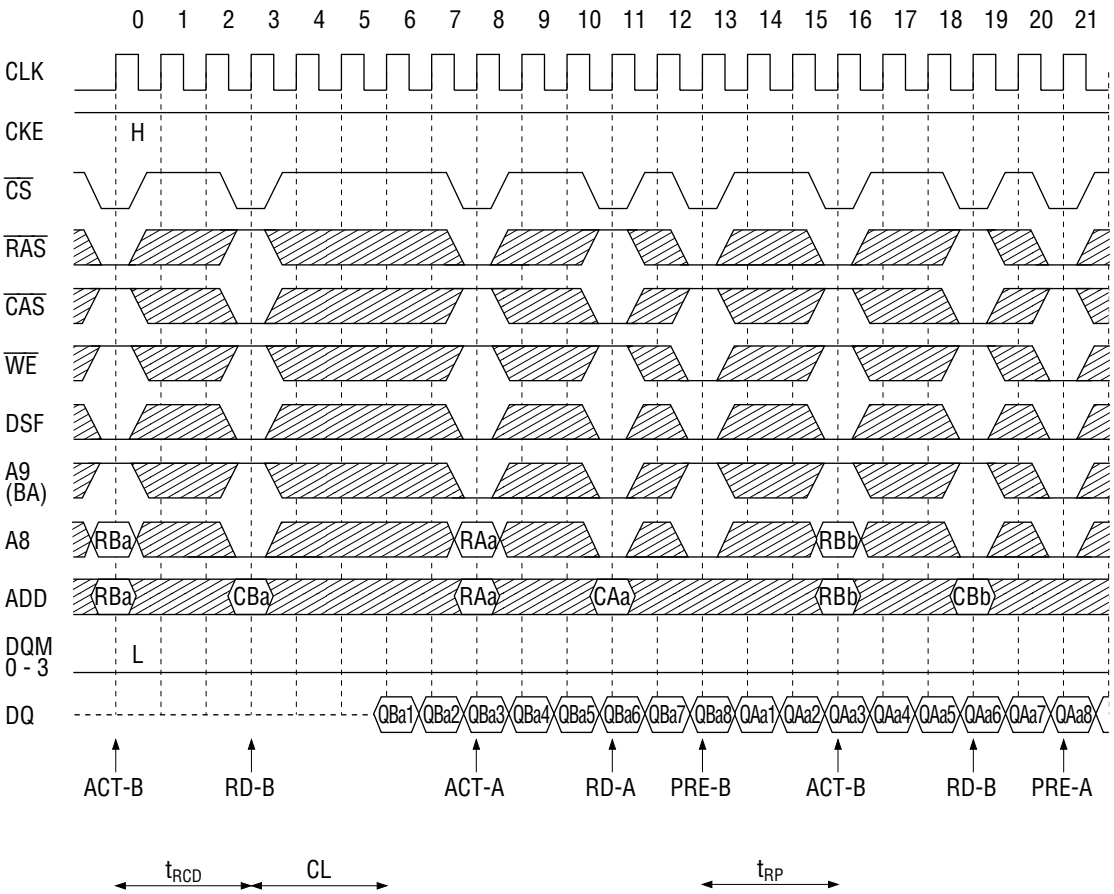
Random Column Read (Page with Same Bank) (BL = 4, CL = 3)



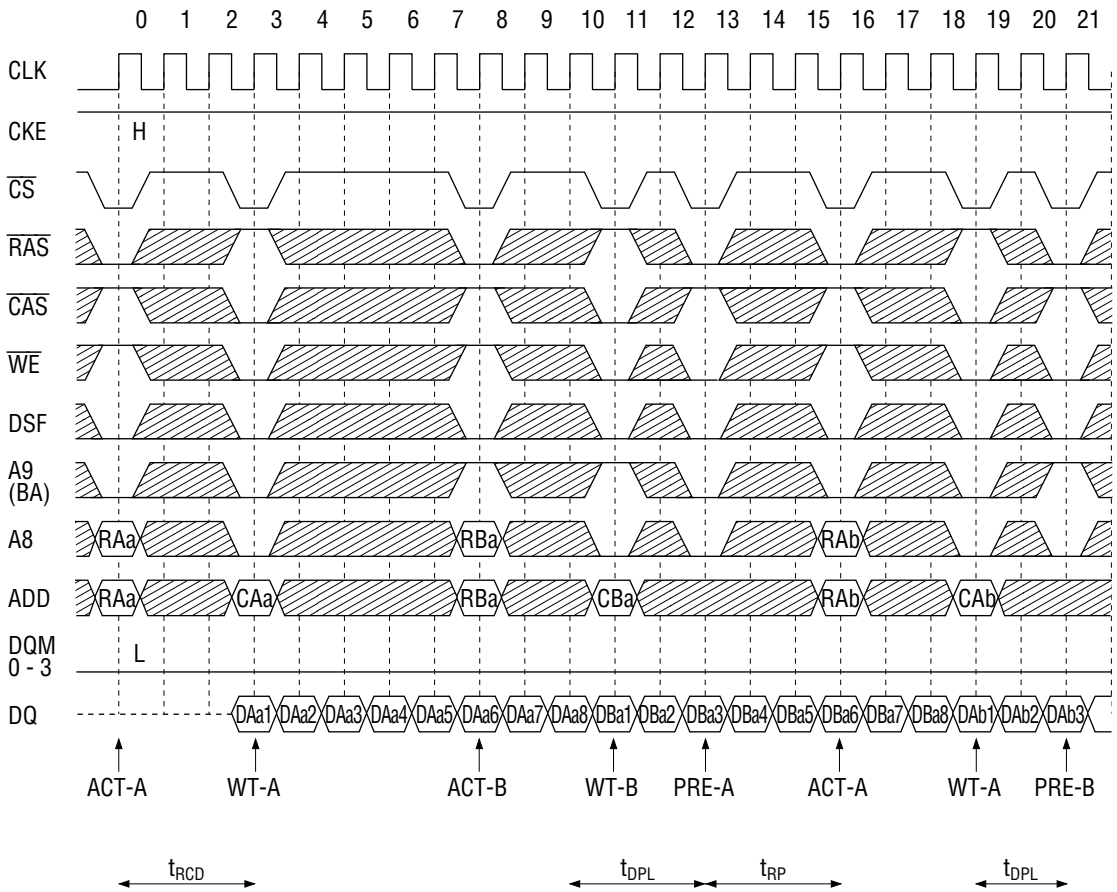
Random Column Write (Page with Same Bank) (BL = 4, CL = 3)



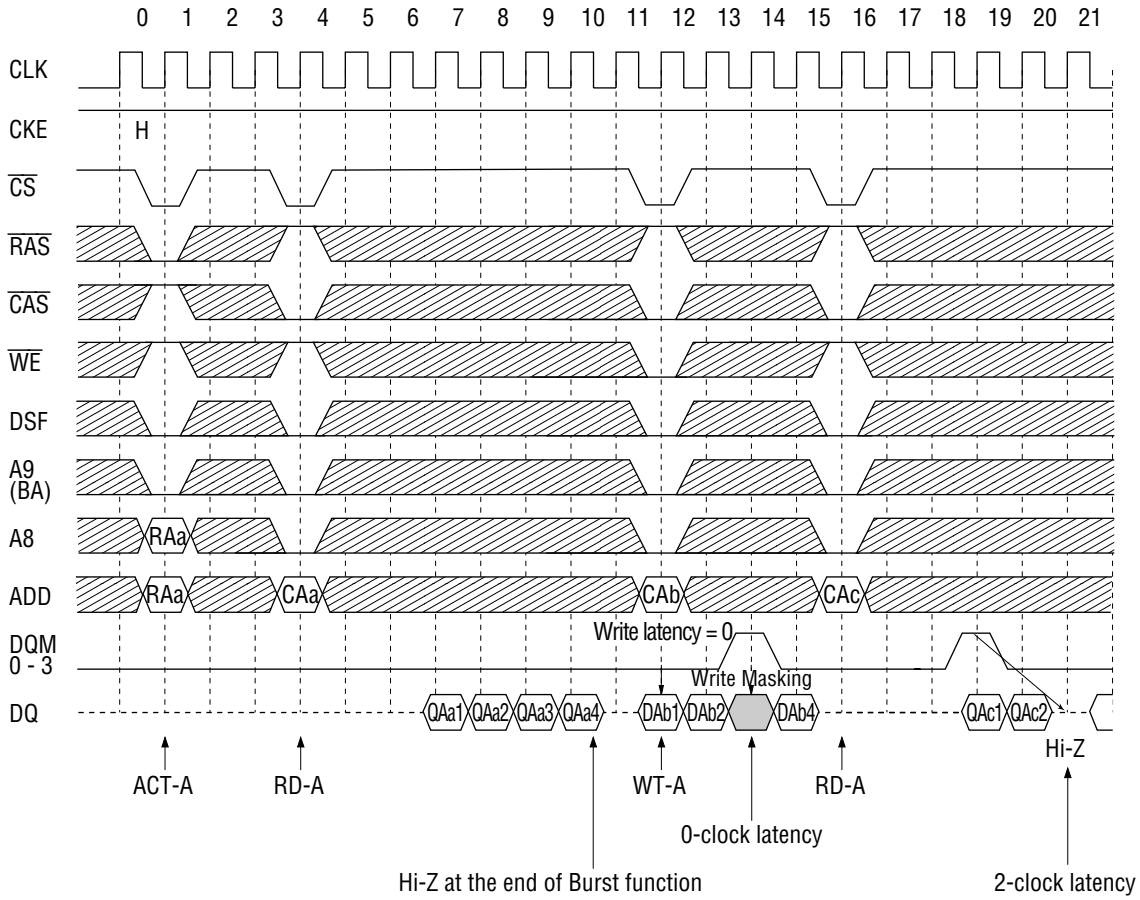
Random Row Read (BL = 8, CL = 3)



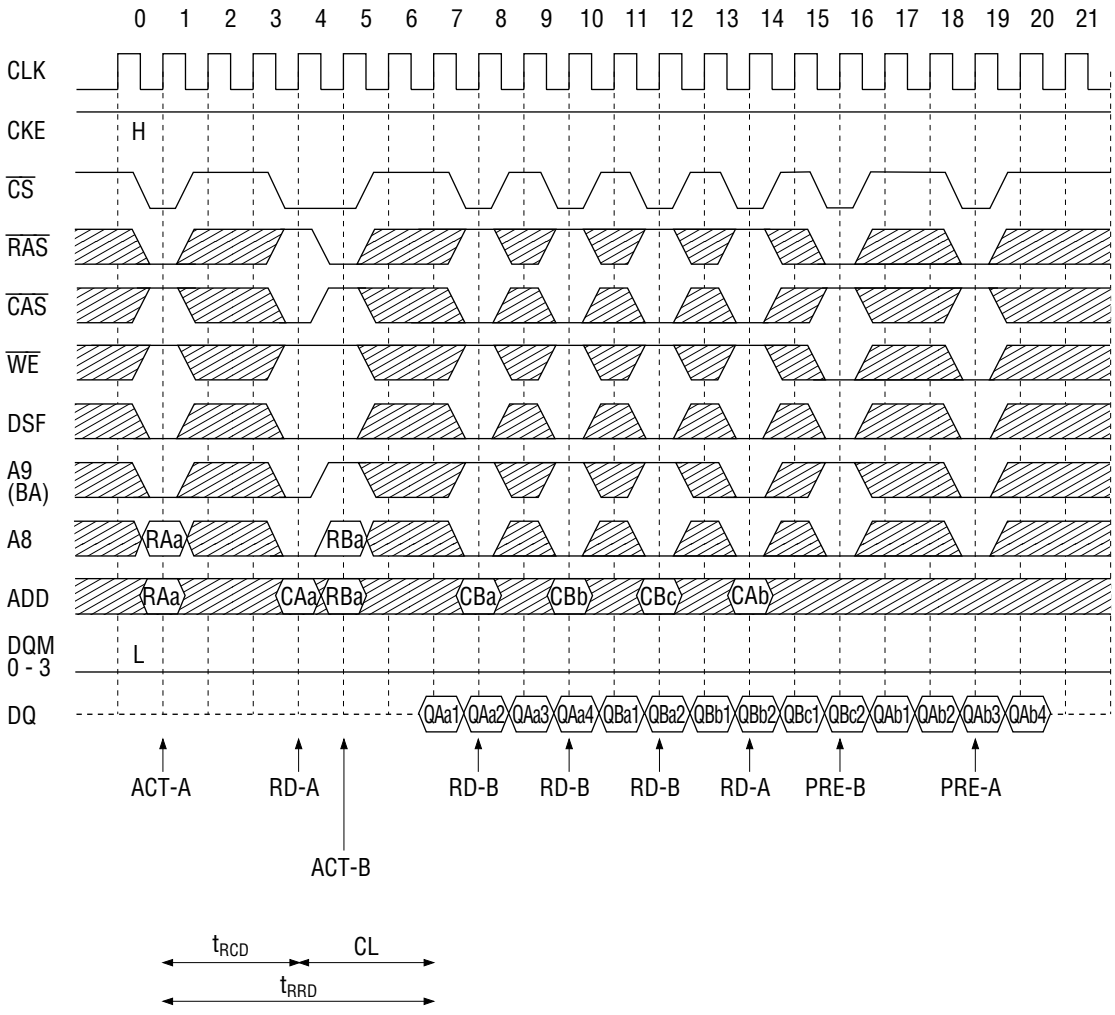
Random Row Write (BL = 8, CL = 3)



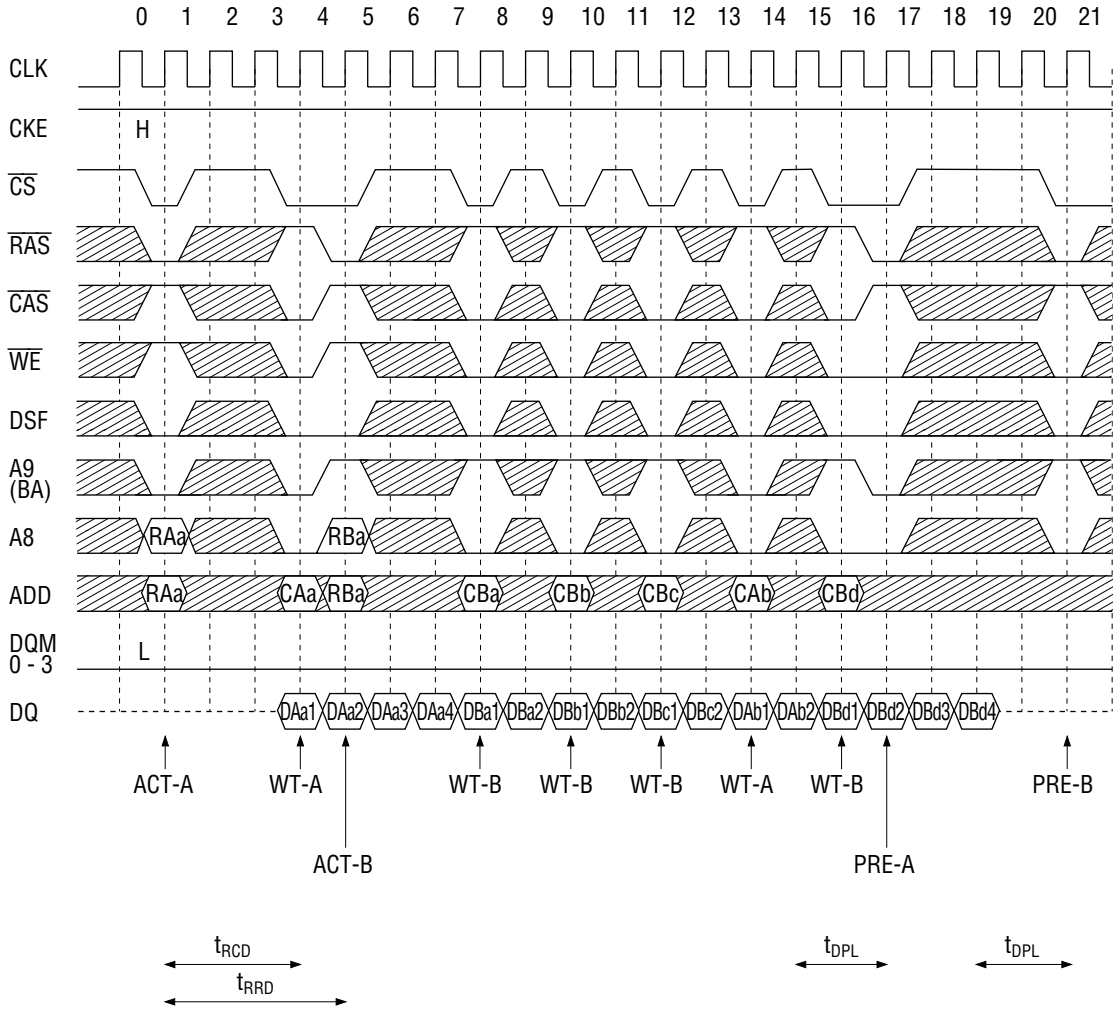
READ and WRITE (BL = 4, CL = 3)



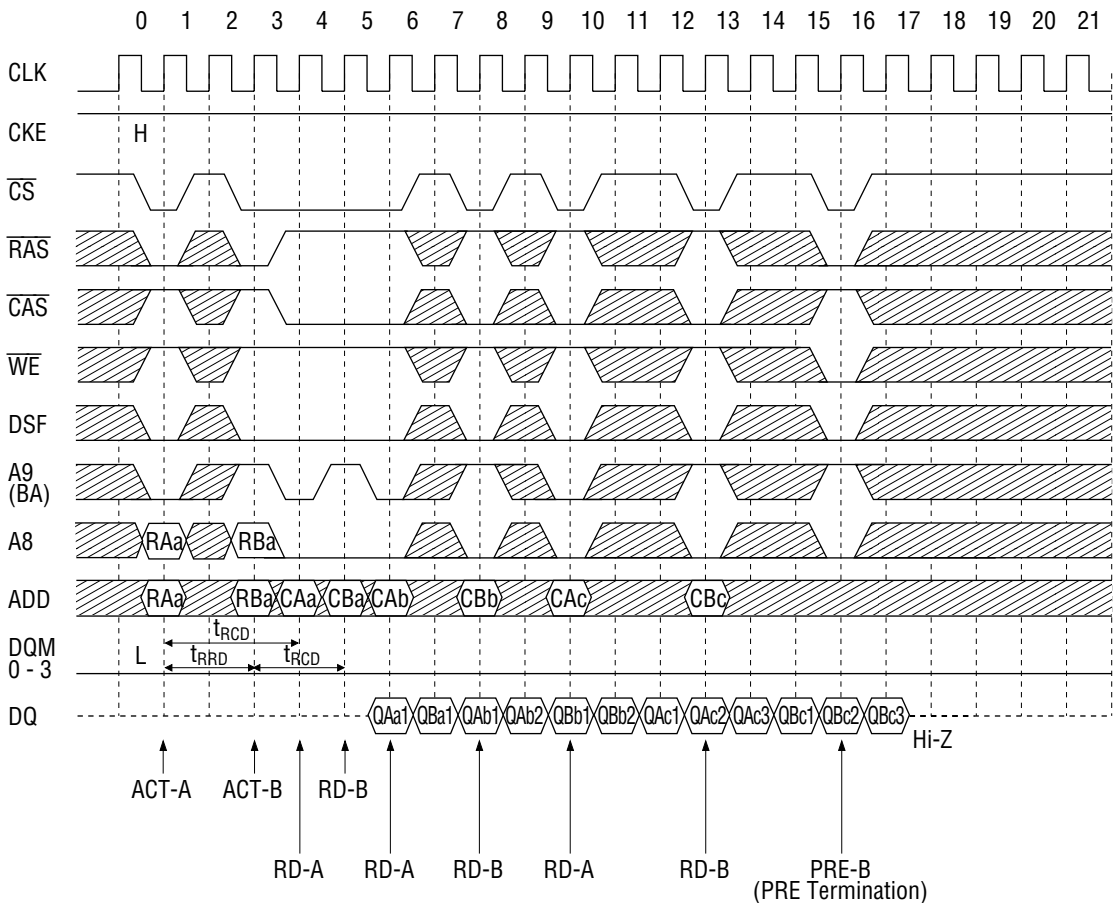
Interleaved Column READ Cycle (BL = 4, CL = 3)



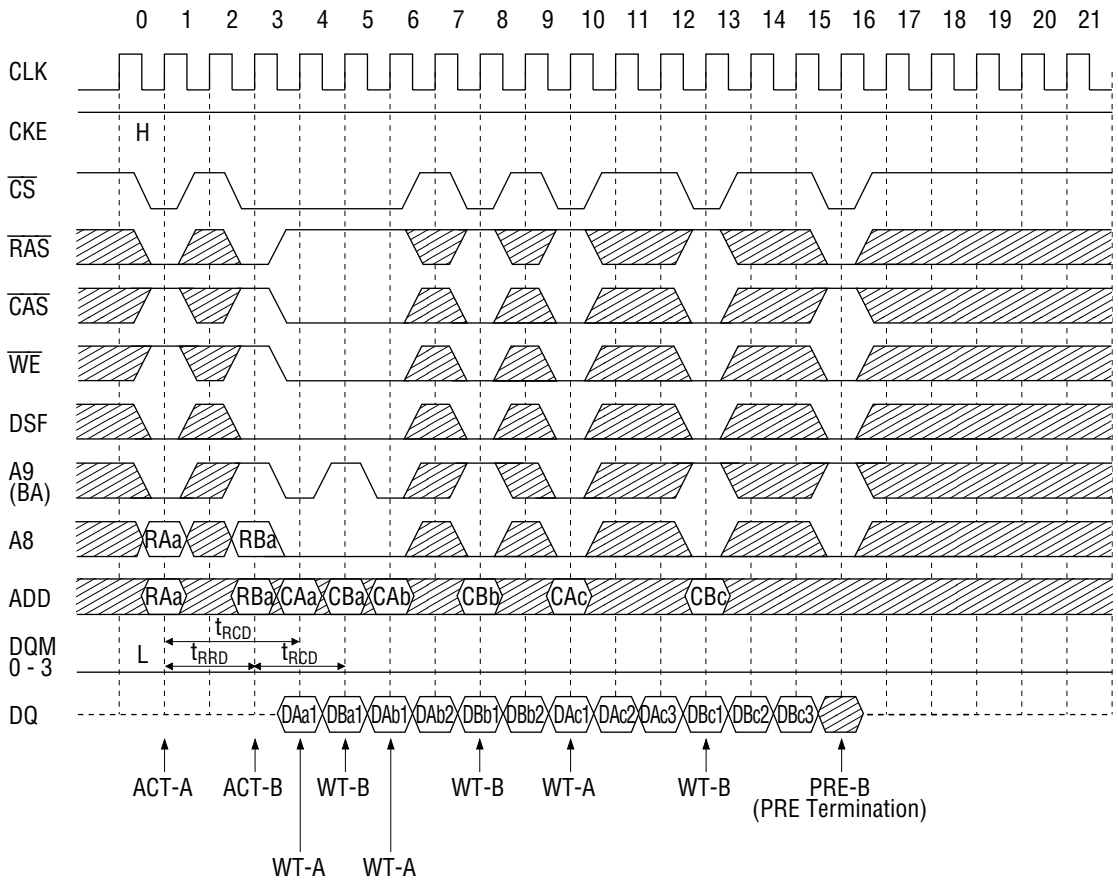
Interleaved Column WRITE Cycle (BL = 4, CL = 3)



Full Page Random Column Read (BL = Full Page, CL = 2)



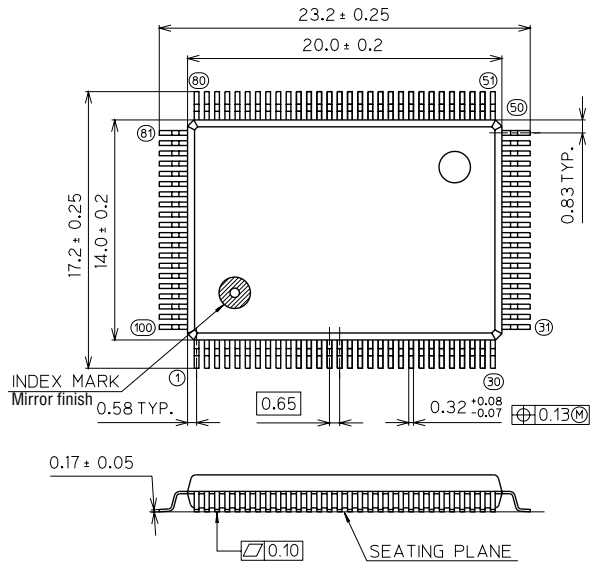
Full Page Random Column Write (BL = Full Page, CL = 2)



PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-BK4



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.54 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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