

MSM5416258B

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM5416258B is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM5416258B achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM5416258B is available in a 40-pin plastic SOJ.

FEATURES

- 262,144-word by 16-bit configuration
- Single 5V power supply, $\pm 10\%$ tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 512 cycles/8ms
- Fast page mode with EDO, read modify write capability
- Byte wide control: 2 CAS control
- CAS before RAS refresh, Hidden refresh, RAS only refresh capability
- Package : 40-Pin 400 mil plastic SOJ (SOJ40-P-400)
(Product : MSM5416258B-xxJS) xx : indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	t _{RAC}	t _{AA}	t _{CAC}	t _{OE}	t _{RC}	t _{HPC}	
MSM5416258B-28	28ns	15ns	9ns	9ns	48ns	12ns	1485mW
MSM5416258B-30	30ns	16ns	9ns	9ns	55ns	13ns	1458mW
MSM5416258B-35	35ns	19ns	10ns	10ns	60ns	13ns	1430mW

PIN CONFIGURATION (TOP VIEW)

Vcc	1	40	Vss
DQ0	2	39	DQ15
DQ1	3	38	DQ14
DQ2	4	37	DQ13
DQ3	5	36	DQ12
Vcc	6	35	Vss
DQ4	7	34	DQ11
DQ5	8	33	DQ10
DQ6	9	32	DQ9
DQ7	10	31	DQ8
NC	11	30	NC
NC	12	29	LCAS
WE	13	28	UCAS
RAS	14	27	OE
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

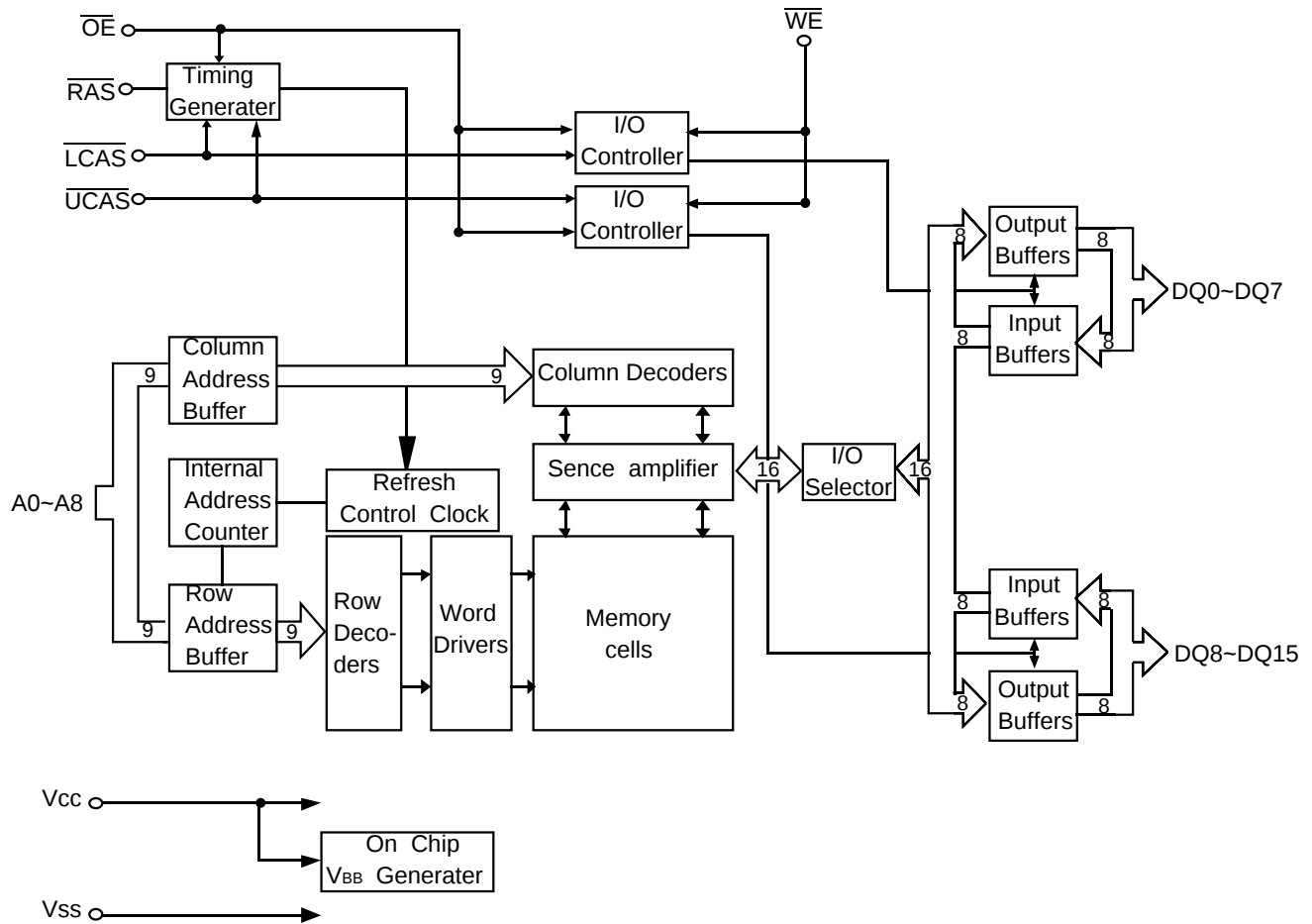
Pin Names	Function
A0-A8	Address Input
RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
WE	Write Enable
OE	Output Enable
Vcc	Power Supply (+5V)
Vss	Ground (0V)
NC	No Connection

Note1 : The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must be provided to every Vss pin.

40Pin 400mil SOJ

REVISION-2 1997.11.10, specification are subject to change without advanced notice.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQPin		Functional Mode
RAS	LCAS	UCAS	WE	OE	DQ0-DQ7	DQ8-DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	Dout	Upper Byte Read
L	L	L	H	L	Dout	Dout	Word Read
L	L	H	L	H	Din	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	Din	Upper Byte Write
L	L	L	L	H	Din	Din	Word Write
L	L	L	H	H	High-Z	High-Z	-

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25°C	-1.0 ~ +7.0	V
Short circuit output current	Ios	Ta=25°C	50	mA
Power dissipation	Pd	Ta=25°C	1.5	W
Operating temperature	Topr	—	0 ~ +70	°C
Storage temperature	Tstg	—	-55 ~ +150	°C

Recommended Operating Conditions

(Ta=0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	4.5	5.0	5.5	V
	Vss	—	0	0	0	V
Input high voltage	V _{IH}	—	2.4	—	6.5	V
Input low voltage	V _{IL}	—	-1.0	—	0.8	V

Capacitance

(Vcc=5V±10%, Ta=25°C, f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0~A8)	C _{IN1}	—	—	8	pf
Input capacitance (RAS, LCAS, UCAS, WE, OE)	C _{IN2}	—	—	8	pf
Input / output capacitance (DQ0~DQ15)	C _{I/O}	—	—	9	pf

DC CHARACTERISTICS

($V_{CC}=5V\pm10\%$, $T_a=0$ to 70°C)

Parameter	Symbol	Condition	MSM5416258B -28		MSM5416258B -30		MSM5416258B -35		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2.0\text{mA}$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0V \leq V_{IN} \leq V_{CC}$	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQI Disable $0V \leq V_o \leq 5.5V$	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = \text{Min.}$	-	270	-	265	-	260	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}, \overline{CAS} = V_{IH}$	-	3	-	3	-	3	mA	1
Average Power Supply Current ($\overline{RAS}$ only Refresh)	I_{CC3}	$\overline{RAS} = \text{Cycling}$ $\overline{CAS} = V_{IH}$ $t_{RC} = \text{Min.}$	-	270	-	265	-	260	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{RAS} = V_{IL}$ $\overline{CAS}$ Cycling $t_{HPC} = \text{Min.}$	-	270	-	265	-	260	mA	1,3
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS} = \text{Cycling}$ $\overline{CAS}$ Before $\overline{RAS}$	-	270	-	265	-	260	mA	1,2

- Notes :
1. I_{CC} Max. is specified as I_{CC} for the output open condition.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

AC CHARACTERISTICS (1/2)

(V_{CC} =5V±10%, T_a =0~70°C)

Parameter	Symbol	MSM5416258B -28		MSM5416258B -30		MSM5416258B -35		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t _{RC}	48	—	55	—	60	—	ns	
Read/Write cycle time	t _{RMW}	70	—	75	—	85	—	ns	
Hyper page mode cycle time	t _{HPC}	12	—	13	—	13	—	ns	
Fast page mode read/write cycle time	t _{PRMW}	34	—	35	—	45	—	ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}	—	28	—	30	—	35	ns	7,12,13
Access time from $\overline{\text{CAS}}$	t _{CAC}	—	9	—	9	—	10	ns	7,12
Access time from column address	t _{AA}	—	15	—	16	—	19	ns	7,13
Access time from $\overline{\text{OE}}$	t _{OEA}	—	9	—	9	—	10	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	17	—	18	—	21	ns	7,12
Data hold after $\overline{\text{CAS}}$ low	t _{COH}	3	—	3	—	3	—	ns	17
Output buffer turn-off delay time	t _{OFF}	3	7	3	8	3	8	ns	8
$\overline{\text{OE}}$ to data output buffer turn-off delay time	t _{OEZ}	3	7	3	8	3	8	ns	8
$\overline{\text{RAS}}$ to data output buffer turn-off delay time	t _{REZ}	3	7	3	8	3	8	ns	8
$\overline{\text{WE}}$ to data output buffer turn-off delay time	t _{WEZ}	3	7	3	8	3	8	ns	8
Transition time	t _T	2	35	2	35	2	35	ns	
Refresh period	t _{REF}	—	8	—	8	—	8	ms	
$\overline{\text{RAS}}$ precharge time	t _{RP}	17	—	18	—	20	—	ns	
RAS pulse width	t _{RAS}	28	10,000	30	10,000	35	10,000	ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	t _{RASP}	28	100,000	30	100,000	35	100,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	7	—	7	—	8	—	ns	
$\overline{\text{RAS}}$ hold time reference to $\overline{\text{OE}}$	t _{ROH}	7	—	7	—	8	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	4	—	4	—	4	—	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	5	10,000	5	10,000	5	10,000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	22	—	25	—	30	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	10	19	11	22	13	26	ns	12
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	8	13	8	15	10	16	ns	
Row address set-up time	t _{ASR}	0	—	0	—	0	—	ns	13
Row address hold time	t _{RAH}	6	—	6	—	7	—	ns	
Column address set-up time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	5	—	5	—	5	—	ns	
Column address hold time from $\overline{\text{RAS}}$	t _{AR}	21	—	22	—	25	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	15	—	18	—	20	—	ns	
Read command set-up time	t _{RCS}	0	—	0	—	0	—	ns	9
Read command hold time	t _{RCH}	0	—	0	—	0	—	ns	
Read command hold time reference to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	9
$\overline{\text{WE}}$ pulse width	t _{WEP}	10	—	10	—	10	—	ns	

AC CHARACTERISTICS (2/2)

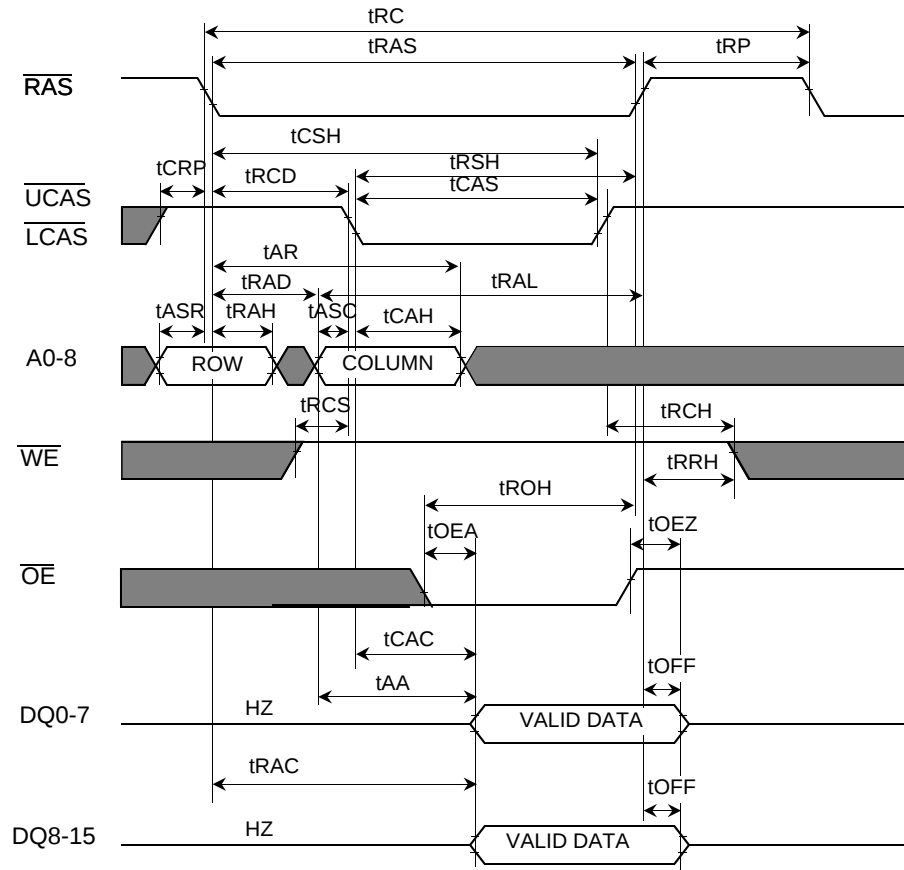
(V_{CC}=5V±10%, T_a=0~70°C)

Parameter	Symbol	MSM5416258B -28		MSM5416258B -30		MSM5416258B -35		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write command set-up time	t _{WCS}	0	—	0	—	0	—	ns	
Write command hold time	t _{WCH}	5	—	5	—	6	—	ns	
Write command pulse width	t _{WP}	5	—	5	—	6	—	ns	
Write command hold time from $\overline{\text{RAS}}$	t _{WCR}	21	—	22	—	26	—	ns	
$\overline{\text{OE}}$ command hold time	t _{OEh}	5	—	5	—	6	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	5	—	5	—	6	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	7	—	7	—	8	—	ns	
Data to $\overline{\text{CAS}}$ delay time	t _{DZC}	0	—	0	—	0	—	ns	
Data to $\overline{\text{OE}}$ delay time	t _{DZO}	0	—	0	—	0	—	ns	
Data-in set-up time	t _{DS}	0	—	0	—	0	—	ns	10
Data-in hold time	t _{DH}	5	—	5	—	6	—	ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	t _{DHR}	21	—	22	—	26	—	ns	
$\overline{\text{OE}}$ to Data-in delay time	t _{OED}	7	—	7	—	8	—	ns	
$\overline{\text{OE}}$ "L" to $\overline{\text{CAS}}$ "H" lead time	t _{OCH}	5	—	5	—	8	—	ns	
$\overline{\text{CAS}}$ "H" to $\overline{\text{OE}}$ "L" lead time	t _{CHO}	5	—	5	—	8	—	ns	
Hi-Z command pulse width	t _{OEP}	5	—	6	—	8	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	18	—	18	—	20	—	ns	11
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	24	—	27	—	30	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	37	—	40	—	45	—	ns	11
$\overline{\text{CAS}}$ active delay time from $\overline{\text{RAS}}$ precharge	t _{RPC}	0	—	0	—	0	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	5	—	6	—	8	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	6	—	6	—	8	—	ns	

Notes:

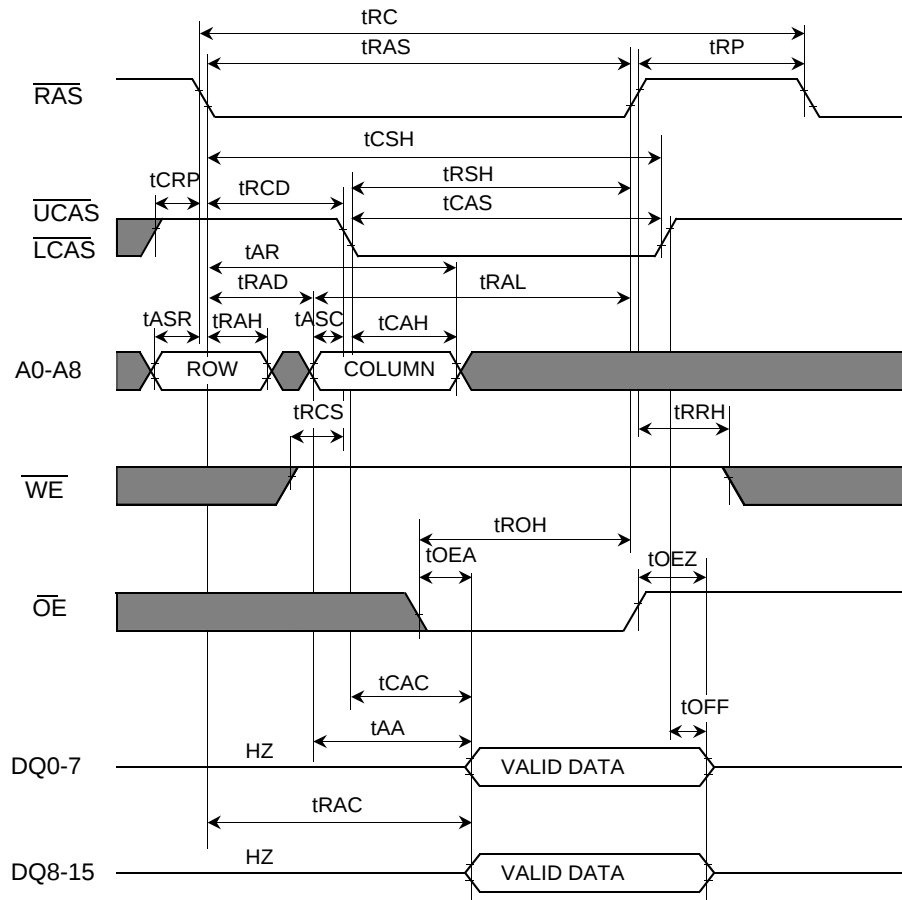
1. All voltages are referenced to V_{SS} .
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200 μ s is required after power-up, followed by any $8\overline{RAS}$ cycles. (Example: RAS-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of $8\overline{CAS}$ before $\overline{RAS}$ cycles instead of $8\overline{RAS}$ cycles are required.
5. The AC characteristics assume $t_r=5$ ns.
6. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Data outputs are measured with a load of 30 pF.
DOUT reference levels: $V_{OH}/V_{OL}=1.8V/1.4V$.
8. t_{REZ} (Max.), t_{OFF} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{OE}$ -controlled write cycles and read-modify-write cycles.
11. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{Min.})$, the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle.
If $t_{RWD} \geq t_{RWD}(\text{Min.})$, $t_{CWD} \geq t_{CWD}(\text{Min.})$ and $t_{AWD} \geq t_{AWD}(\text{Min.})$, the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indeterminate.
12. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met.
 t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CDC} .
13. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA} .
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0 - A8) may be changed two times or less while $\overline{RAS} = V_{IL}$.
16. Addresses (A0 - A8) may be changed once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
17. This is guaranteed by design. ($t_{COH}=t_{CAC}$ - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

READ CYCLE (RAS output control)



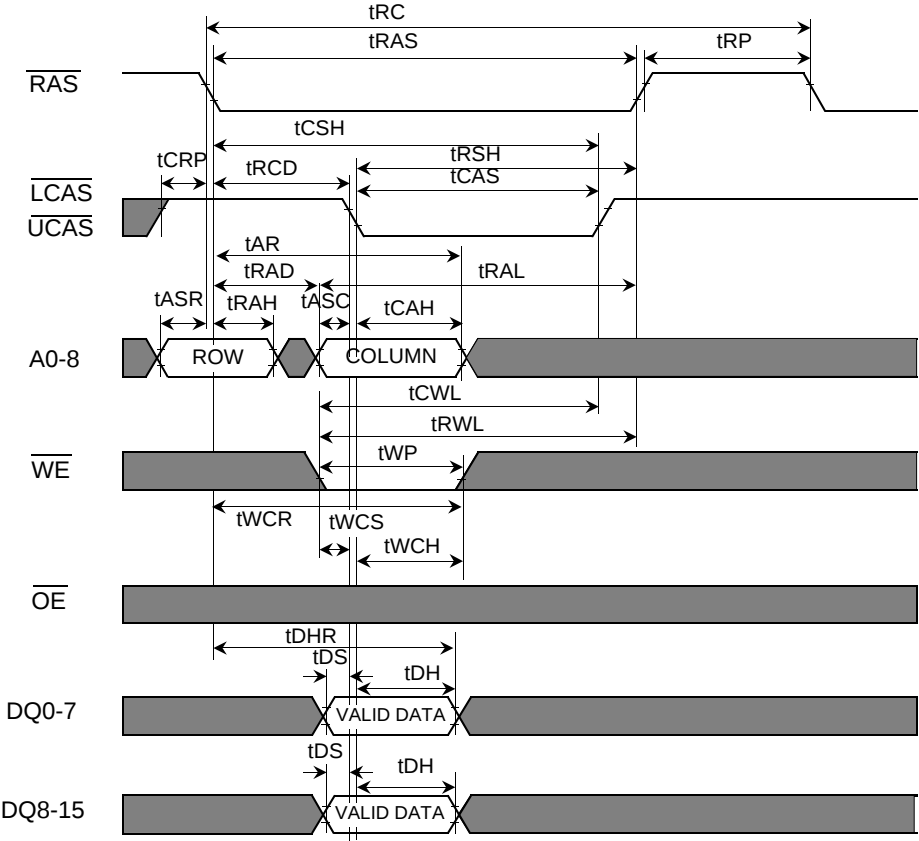
■ : "H" or "L"

READ CYCLE (CAS output control)

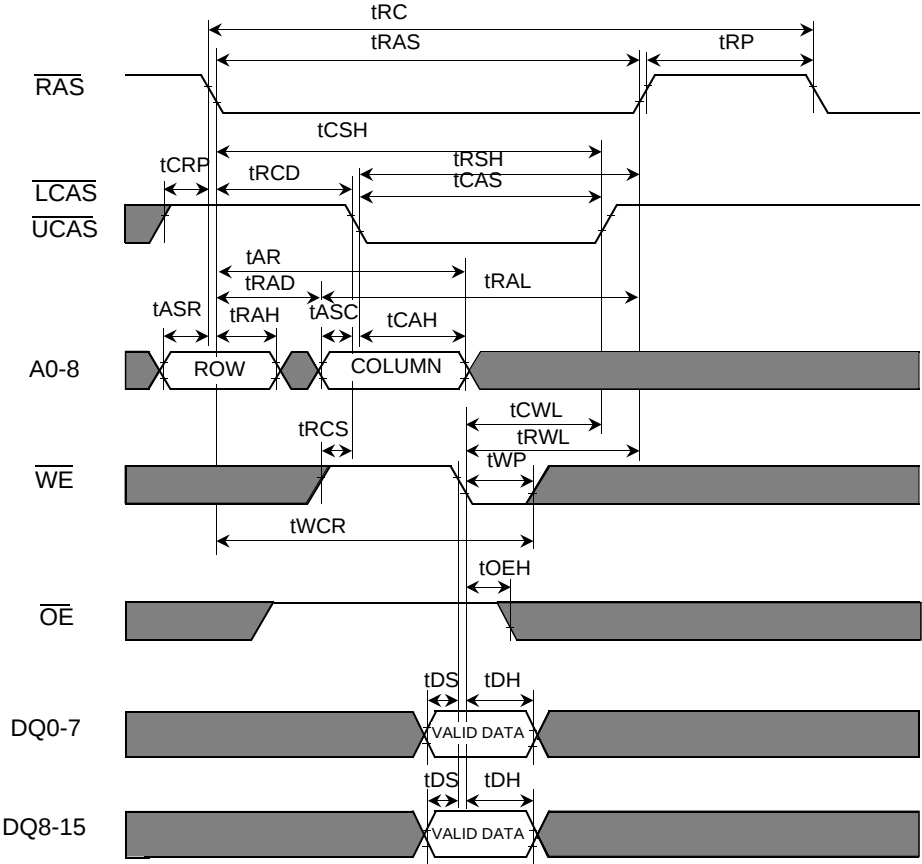


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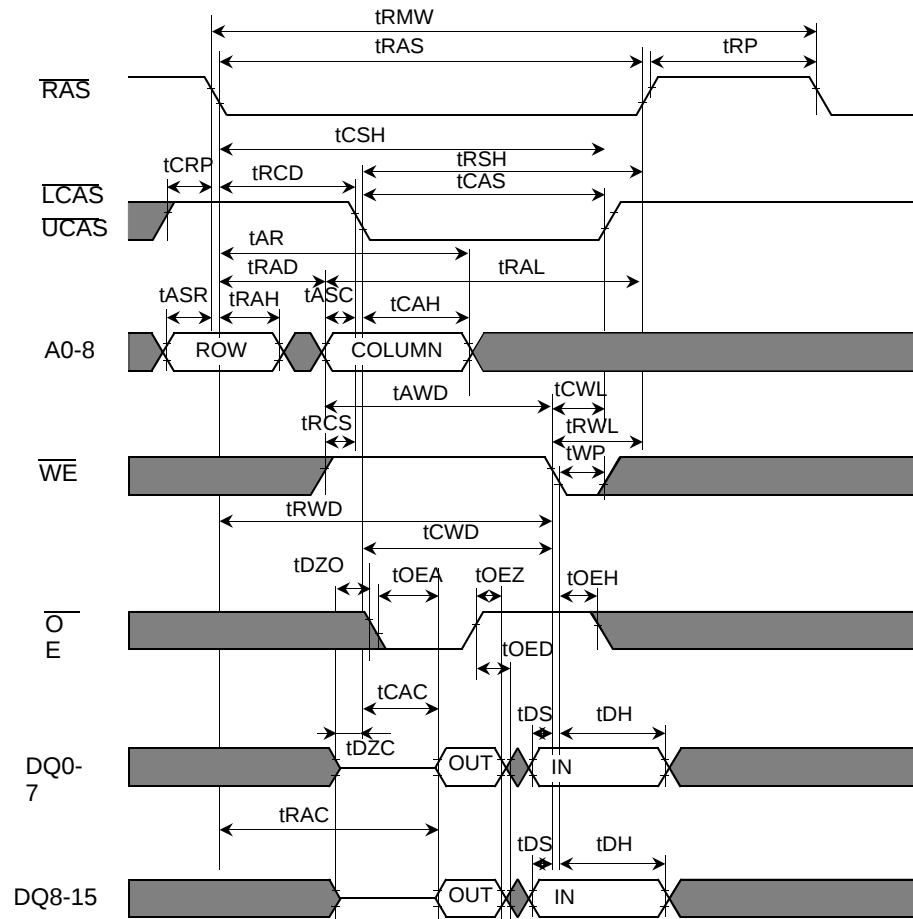
EARLY WRITE CYCLE (LCAS and UCAS active)



LATE WRITE CYCLE (LCAS and UCAS active)

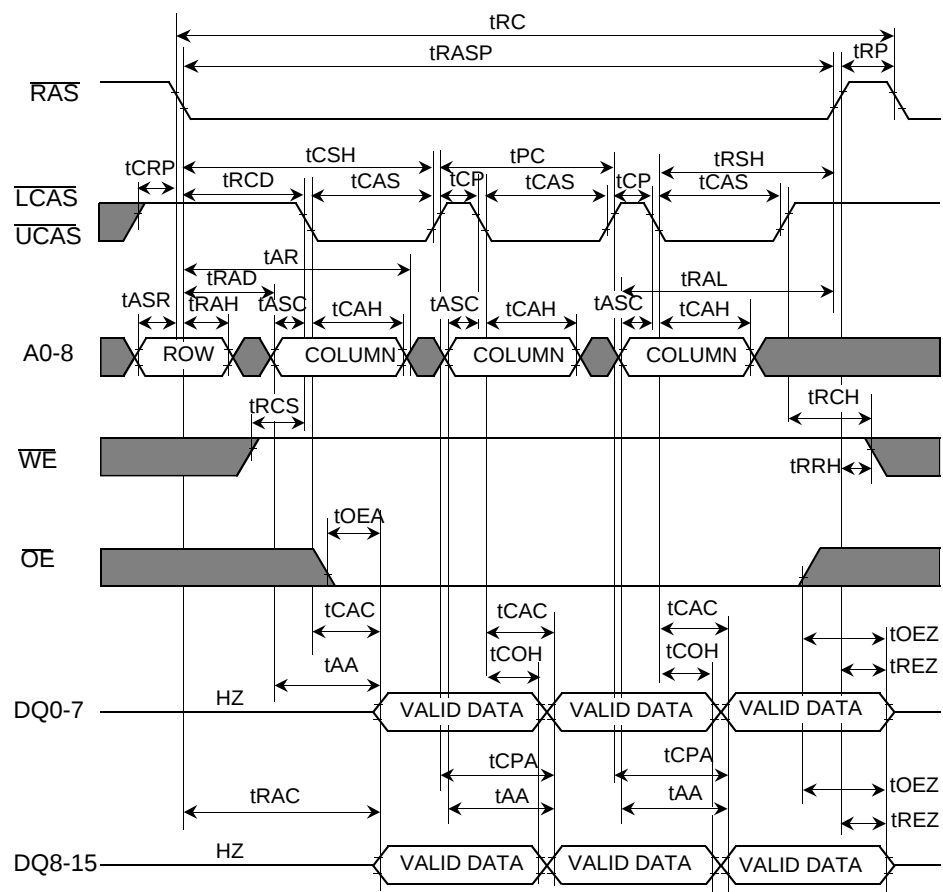


READ MODIFY WRITE CYCLE (LCAS and UCAS active)



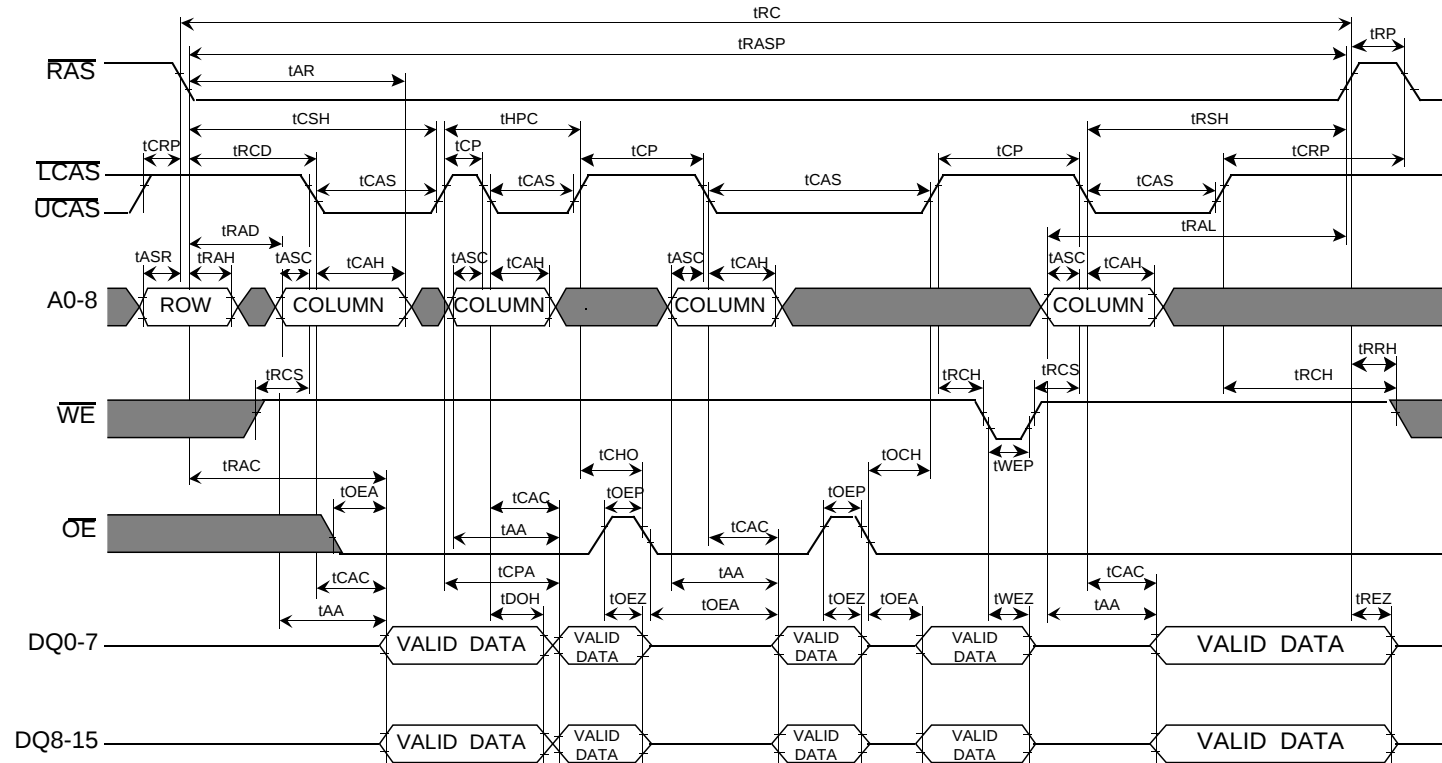
■ : "H" or "L"

FAST PAGE MODE READ CYCLE with Extended Data Out



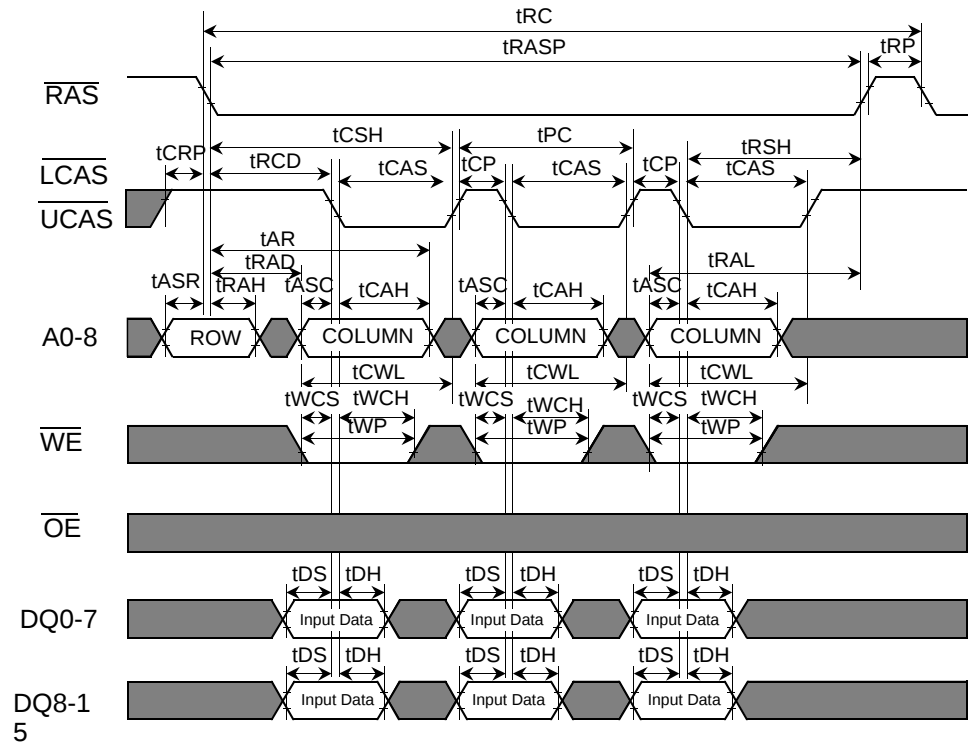
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FAST PAGE MODE READ Hi-Z OPERATION



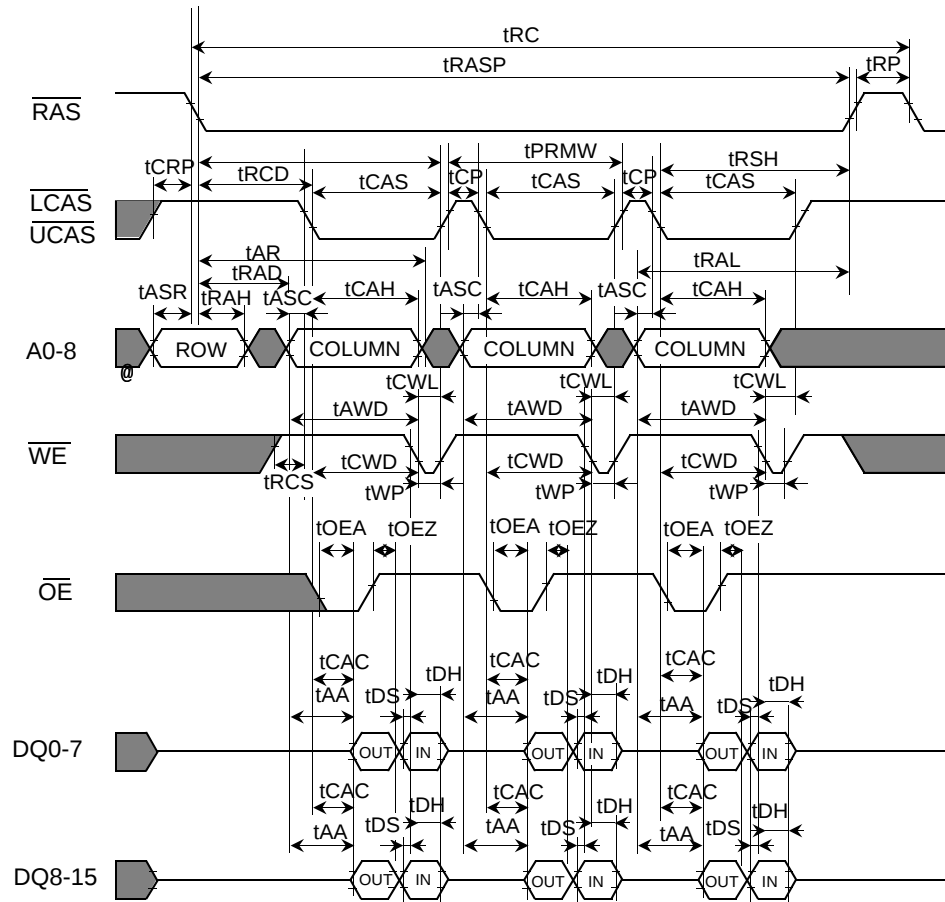
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FAST PAGE MODE EARLY WRITE CYCLE



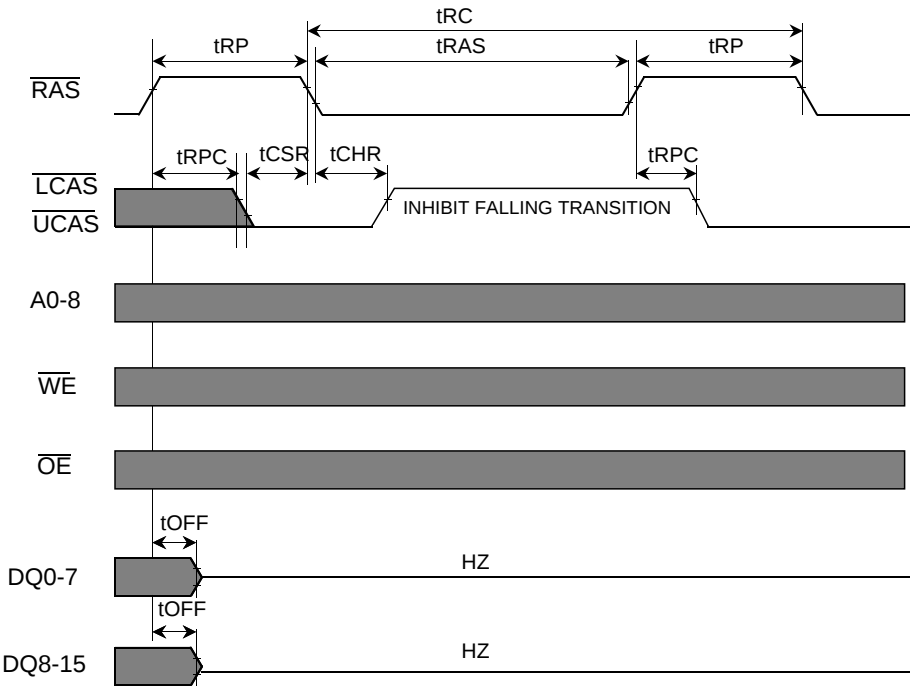
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FAST PAGE MODE READ MODIFY WRITE CYCLE



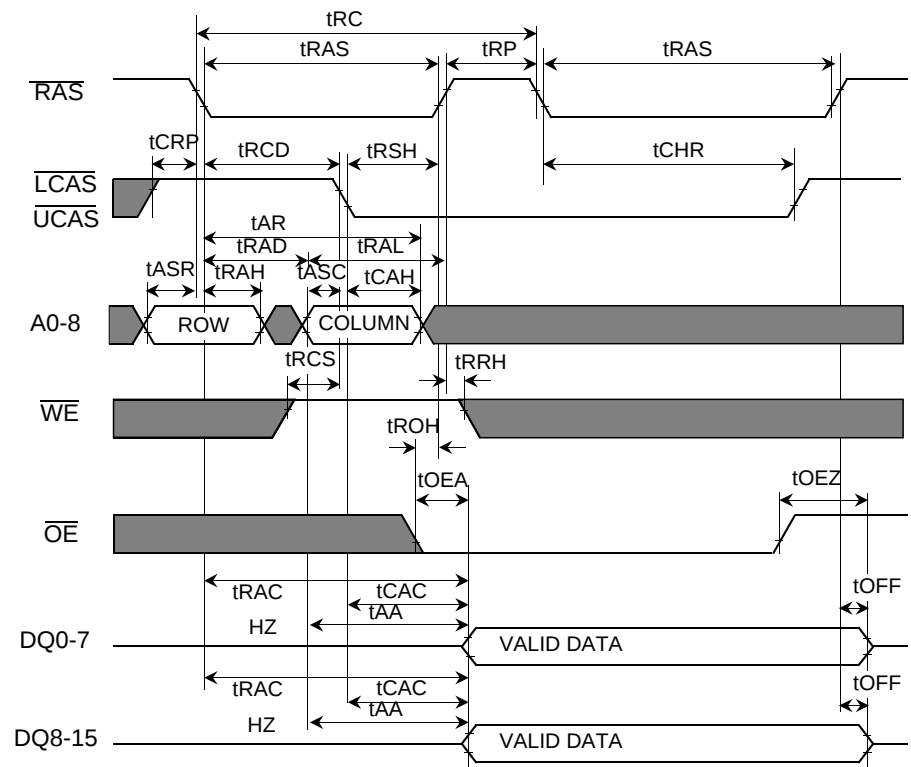
☐ : "H" or "L"

CAS BEFORE RAS REFRESH CYCLE

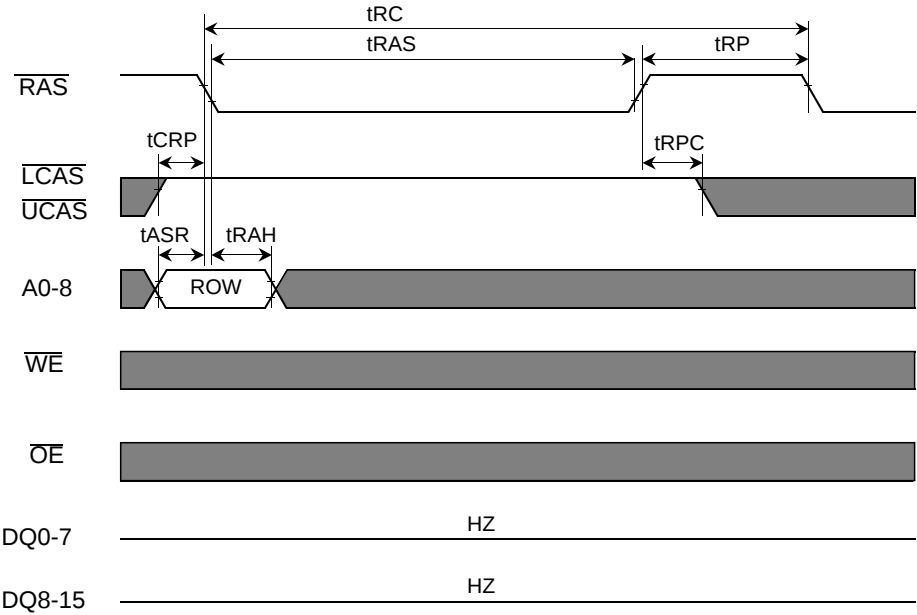


■ : "H" or "L"

HIDDEN REFRESH CYCLE



$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



■ : "H" or "L"

PACKAGE OUTLINES AND DIMENSIONS

(Unit: mm)

