OKI Semiconductor

MSM531601D

2,097,152-Word x 8-Bit Mask ROM

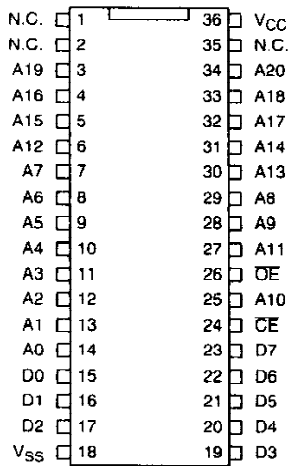
DESCRIPTION

The OKI MSM531601D is a high-speed silicon gate CMOS Mask ROM with 2,097,152-word x 8-bit capacity. The MSM531601D operates on a single 5.0 V power supply and is TTL compatible. The chip's asynchronous I/O requires no external clock assuring easy operation. A power-down mode provides low power dissipation when the chip is not selected. The $\overline{CE}$ and $\overline{OE}$ pins provide control signals permitting the output to be three-stated, allowing easy memory expansion on a system bus. The MSM531601D is suited for use as large capacity fixed memory for microcomputers and data terminals.

FEATURES

- 2 Meg x 8 bits
- Single 5.0 V power supply
- 120 ns access time (max.)
- Input/Output TTL compatible
- Pin compatible OTP available
- Three-state output
- Packages
  - 36-Pin plastic DIP

PIN CONFIGURATION

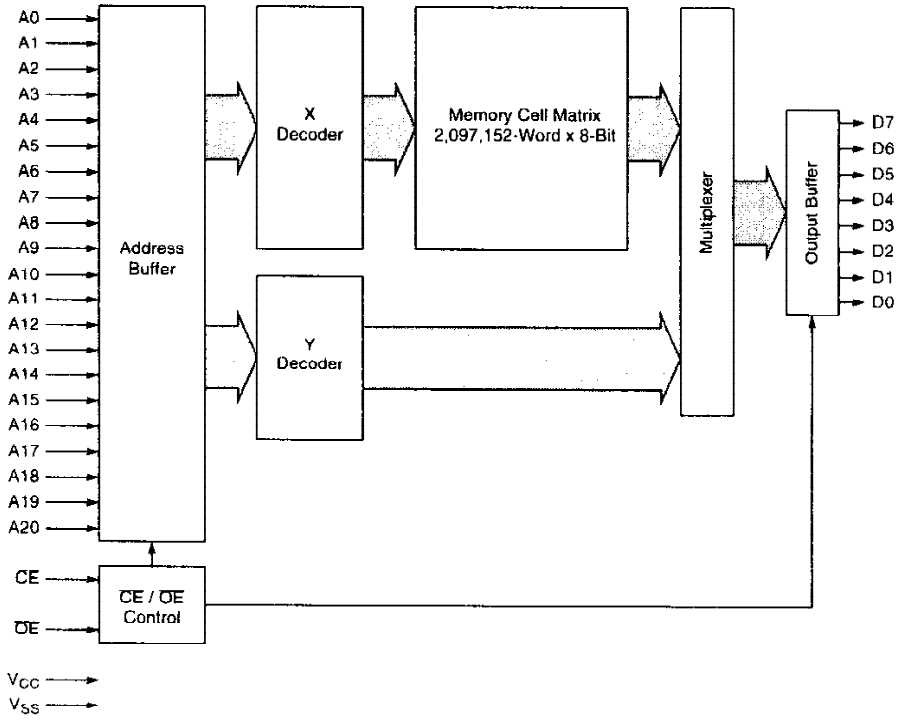


36-Pin DIP

Pin Configuration

Pin Name	Function
A0 ~ A20	Address input
D0 ~ D7	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}, V_{SS}	Power supply

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Parameter	Symbol	Value	Unit
Power supply voltage V_{CC} relative to V_{SS}	V_{CC}	-0.3 ~ +7.0	V
Input voltage relative to V_{SS}	V_{IN}	-0.3 ~ V_{CC} + 0.5	V
Output voltage relative to V_{SS}	V_{OUT}	-0.3 ~ V_{CC} + 0.5	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPR}	-0 ~ +70	°C
Storage temperature	T_{STG}	-55 ~ +150	°C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (V_{CC} = 5.0 V, T_a = 0 to +70°C)

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	5.0	V_{CC} + 0.5	V
Input low voltage	V_{IL}	-0.3	0	0.8	V

Capacitance (T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ	Max	
Input capacitance	C_I	V_{IN} = 0 V	–	–	10	pF
Output capacitance	C_O	V_{OUT} = 0 V	–	–	12	pF

DC Characteristics (V_{CC} = 5.0 V ±10%, T_a = 0°C ~ +70°C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Output high voltage	V_{OH}	I_{OH} = -400 µA	2.4	-	-	V
Output low voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.4	V
Input leakage current	I_{LI}	V_{IN} = 0 V, — V_{CC}	-10	-	10	µA
Output leakage current	I_{LO}	V_{OUT} = 0 V, — V_{CC}, $\overline{CE}$ = $V_{IH\ (MIN)}$	-10	-	10	µA
Average power supply current (Operating)	I_{CC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, t_C = 120 ns	-	-	35	mA
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, t_C = 1 µs	-	-	20	mA
Power supply current (Standby)	I_{CCS}	$\overline{CE}$ = V_{CC} - 0.2 V	-	-	50	µA
	I_{CCS1}	$\overline{CE}$ = $V_{IH\ (MIN)}$	-	-	500	µA

AC Characteristics Read Cycle (V_{CC} = 5.0 V ±10%, C_L = 100 pF+1TTL, T_a = 0°C ~ +70°C) [1]

Parameter	Symbol	Conditions	Rated Value			Unit
			Min	Typ	Max	
Address access time	t_{ACC}		-	-	120	ns
$\overline{CE}$ access time	t_{CE}		-	-	120	ns
$\overline{OE}$ access time	t_{OE}		-	-	60	ns
$\overline{CE}$ output disable time [2]	t_{CHZ}		0	-	50	ns
$\overline{OE}$ output disable time [2]	t_{OHZ}		0	-	40	ns
Output hold time	t_{OH}		0	-	-	ns

1. Input signal level: V_{IH} = 2.4 V, V_{IL} = 0.6 V. AC measurements assume $t_r = t_f$ = 5 ns. Timing reference level: V_{IN} = 1.5 V, V_{OUT} = 0.8 V & 2.0 V.
2. t_{CHZ} and t_{OHZ} define the time at which the output achieves an open circuit condition and are not referenced to output voltage levels.

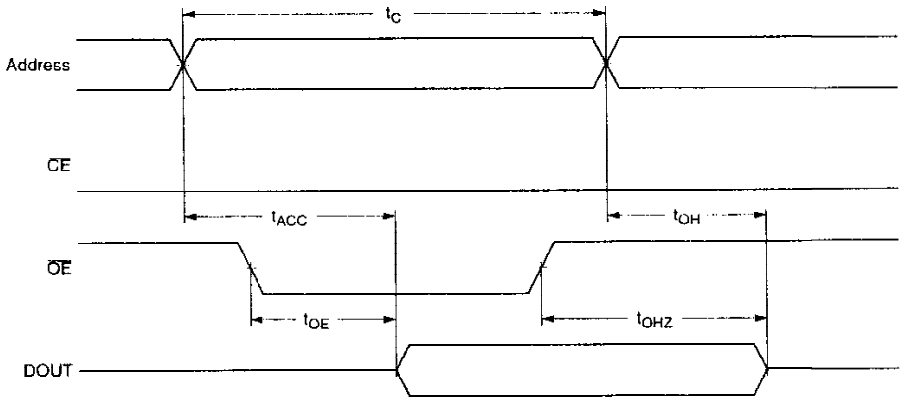


Figure 1. Read Cycle 1

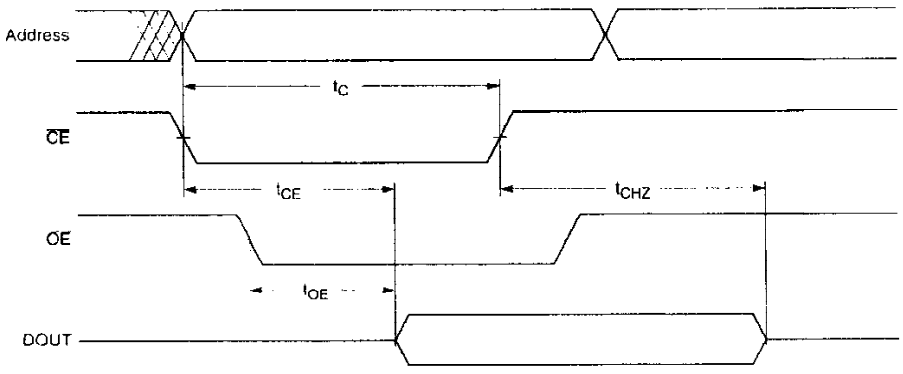


Figure 2. Read Cycle 2