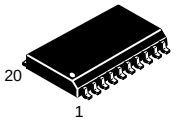
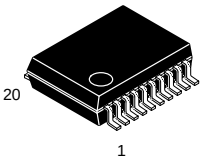
Product Preview

MC145482

5 V 13-Bit Linear PCM Codec-Filter



DW SUFFIX
SOG PACKAGE
CASE 751D

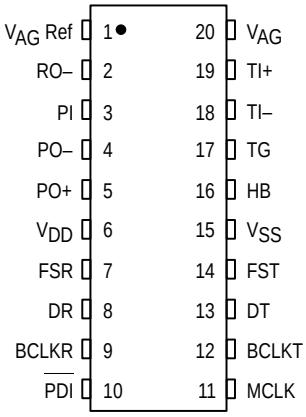


SD SUFFIX
SSOP
CASE 940C

ORDERING INFORMATION

MC145482DW	SOG Package
MC145482SD	SSOP

PIN ASSIGNMENT



The MC145482 is a 13–bit linear PCM Codec–Filter with 2s complement data format, and is offered in 20–pin SOG and SSOP packages. This device performs the voice digitization and reconstruction as well as the band limiting and smoothing required for the voice coding in digital communication systems. This device is designed to operate in both synchronous and asynchronous applications and contains an on–chip precision reference voltage.

This device has an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low–pass filters the analog signal with an active R–C filter to eliminate very high frequency noise from being modulated down to the passband by the switched capacitor filter. From the active R–C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single–ended design, which reduces the significance of noise to both the inverted and non–inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common–mode signal that is cancelled when the inverted and non–inverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter band–passes the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential 13–bit linear A/D converter. The digital output is 2s complement format.

The decoder digital input accepts 2s complement data and reconstructs it using a differential 13–bit linear D/A converter. The output of the D/A is low–pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R–C filter to eliminate the out–of–band energy of the switched capacitor filter.

The MC145482 PCM Codec–Filter has a high impedance V_{AG} reference pin which allows for decoupling of the internal circuitry that generates the mid–supply V_{AG} reference voltage to the V_{SS} power supply ground. This reduces clock noise on the analog circuitry when external analog signals are referenced to the power supply ground.

The MC145482 13–bit linear PCM Codec–Filter accepts both Short Frame Sync and Long Frame Sync clock formats, and utilizes CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.

- Single 5 V Power Supply
- 13–Bit Linear ADC/DAC Conversions with 2s Complement Data Format
- Typical Power Dissipation of 25 mW, Power–Down of 0.01 mW
- Fully–Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Transmit High–Pass Filter May be Bypassed by Pin Selection
- Active R–C Pre–Filtering and Post–Filtering
- On–Chip Precision Reference Voltage of 1.575 V for a 0 dBm TLP @ 600 Ω
- Full–Duplex Sample Rates from 7 k to 16 k Samples/s
- 3–Terminal Input Op Amp Can be Used, or a 2–Channel Input Multiplexer
- Receive Gain Control from 0 dB to – 21 dB in 3 dB Steps in Synchronous Operation
- Push–Pull 300 Ω Power Drivers with External Gain Adjust

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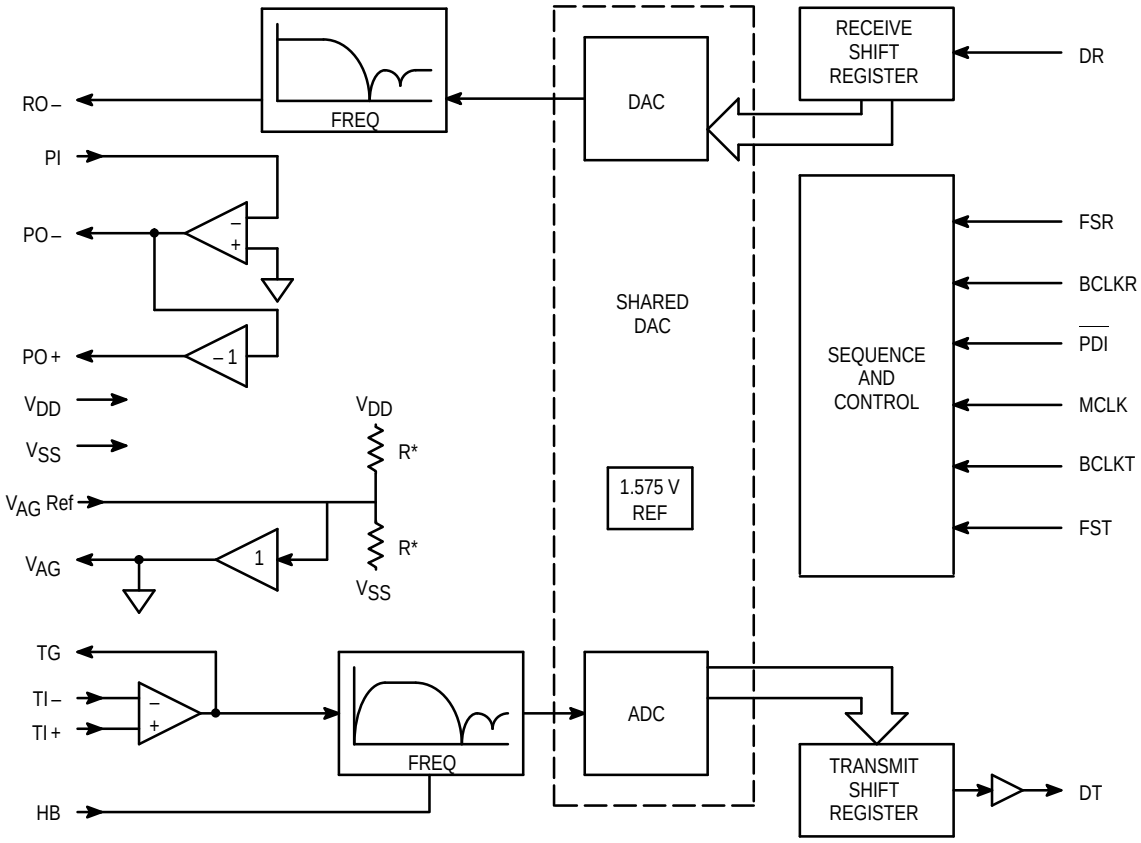


Figure 1. MC145482 13–Bit Linear PCM Codec–Filter Block Diagram

DEVICE DESCRIPTION

A PCM Codec–Filter is used for digitizing and reconstructing the human voice. These devices are used primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from ‘‘COder’’ for the analog–to–digital converter (ADC) used to digitize voice, and ‘‘DECoder’’ for the digital–to–analog converter (DAC) used for reconstructing voice. A codec is a single device that does both the ADC and DAC conversions.

To digitize intelligible voice requires a signal–to–distortion ratio of about 30 dB over a dynamic range of about 40 dB. This may be accomplished with a linear 13–bit ADC and DAC. The MC145482 satisfies these requirements and may be used as the analog front–end for voice coders using DSP technology to further compress the digital data stream.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal’s highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low–pass filter to limit the high frequency energy above 3 kHz from distorting the in–band signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high–pass filter before the analog–to–digital converter. The MC145482 includes a high–pass filter for compatibility with existing telephone applications, but it may be removed from the analog input signal path by the high–pass bypass pin.

The digital–to–analog conversion process reconstructs a staircase version of the desired in–band signal, which has spectral images of the in–band signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components, which need to be attenuated to obtain the desired signal. The low–pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145482 PCM Codec–Filter has the codec, both presampling and reconstruction filters, and a precision voltage reference on–chip.

PIN DESCRIPTIONS

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 6)

This is the most positive power supply and is typically connected to + 5 V. This pin should be decoupled to V_{SS} with a 0.1 μF ceramic capacitor.

V_{SS}
Negative Power Supply (Pin 15)

This is the most negative power supply and is typically connected to 0 V.

V_{AG}
Analog Ground Output (Pin 20)

This output pin provides a mid–supply analog ground. This pin should be decoupled to V_{SS} with a 0.01 μF ceramic capacitor. All analog signal processing within this device is referenced to this pin. If the audio signals to be processed are referenced to V_{SS}, then special precautions must be utilized to avoid noise between V_{SS} and the V_{AG} pin. Refer to the applications information in this document for more information. The V_{AG} pin becomes high impedance when this device is in the powered–down mode.

V_{AG} Ref
Analog Ground Reference Bypass (Pin 1)

This pin is used to capacitively bypass the on–chip circuitry that generates the mid–supply voltage for the V_{AG} output pin. This pin should be bypassed to V_{SS} with a 0.1 μF ceramic capacitor using short, low inductance traces. The V_{AG} Ref pin is only used for generating the reference voltage for the V_{AG} pin. Nothing is to be connected to this pin in addition to the bypass capacitor. All analog signal processing within this device is referenced to the V_{AG} pin. If the audio signals to be processed are referenced to V_{SS}, then special precautions must be utilized to avoid noise between V_{SS} and the V_{AG} pin. Refer to the applications information in this document for more information. When this device is in the powered–down mode, the V_{AG} Ref pin is pulled to the V_{DD} power supply with a non–linear, high–impedance circuit.

CONTROL

HB
Transmit High–Pass Filter Bypass (Pin 16)

This pin selects whether the transmit high–pass filter will be used or bypassed, which allows frequencies below 200 Hz to appear at the input of the ADC to be digitized. This high–pass filter is a third order filter for attenuating power line frequencies, typically 50/60 Hz. A logic low selects this filter. A logic high deselects or bypasses this filter. When the filter is bypassed, the transmit frequency response extends down to dc.

$\overline{PDI}$
Power–Down Input (Pin 10)

This pin puts the device into a low power dissipation mode when a logic 0 is applied. When this device is powered down, all of the clocks are gated off and all bias currents are turned off, which causes RO–, PO–, PO+, TG, V_{AG}, and DT to become high impedance. The device will operate normally when a logic 1 is applied to this pin. The device goes through a power–up sequence when this pin is taken to a logic 1 state, which prevents the DT PCM output from going low impedance for at least two FST cycles. The V_{AG} and V_{AG} Ref circuits and the signal processing filters must settle out before the DT PCM output or the RO– receive analog output will represent a valid analog signal.

ANALOG INTERFACE

TI+
Transmit Analog Input (Non–Inverting) (Pin 19)

This is the non–inverting input of the transmit input gain setting operational amplifier. This pin accommodates a differential to single–ended circuit for the input gain setting op amp. This allows input signals that are referenced to the V_{SS} pin to be level shifted to the V_{AG} pin with minimum noise. This pin may be connected to the V_{AG} pin for an inverting amplifier configuration if the input signal is already referenced to the V_{AG} pin. The common mode range of the TI+ and TI– pins is from 1.2 V, to V_{DD} minus 1.2 V. This is an FET gate input.

The TI+ pin also serves as a digital input control for the transmit input multiplexer. Connecting the TI+ pin to V_{DD} will place this amplifier's output (TG) into a high–impedance state, and selects the TG pin to serve as a high–impedance input to the transmit filter. Connecting the TI+ pin to V_{SS} will also place this amplifier's output (TG) into a high–impedance state, and selects the TI– pin to serve as a high–impedance input to the transmit filter.

TI–
Transmit Analog Input (Inverting) (Pin 18)

This is the inverting input of the transmit gain setting operational amplifier. Gain setting resistors are usually connected from this pin to TG and from this pin to the analog signal source. The common mode range of the TI+ and TI– pins is from 1.2 V to V_{DD} – 1.2 V. This is an FET gate input.

The TI– pin also serves as one of the transmit input mulitplexer pins when the TI+ pin is connected to V_{SS}. When TI+ is connected to V_{DD}, this pin is ignored. See the pin descriptions for the TI+ and the TG pins for more information.

TG
Transmit Gain (Pin 17)

This is the output of the transmit gain setting operational amplifier and the input to the transmit band–pass filter. This op amp is capable of driving a 2 kΩ load. Connecting the TI+ pin to V_{DD} will place the TG pin into a high–impedance state, and selects the TG pin to serve as a high–impedance input to the transmit filter. All signals at this pin are referenced to the V_{AG} pin. When TI+ is connected to V_{SS}, this pin is ignored. See the pin descriptions for TI+ and TI– pins for more information. This pin is high impedance when the device is in the powered–down mode.

RO–
Receive Analog Output (Inverting) (Pin 2)

This is the inverting output of the receive smoothing filter from the digital–to–analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. If the device is operated half–channel with the FST pin clocking and FSR pin held low, the receive filter input will be

connected to the V_{AG} voltage. This minimizes transients at the RO– pin when full–channel operation is resumed by clocking the FSR pin. This pin is high impedance when the device is in the powered–down mode.

PI
Power Amplifier Input (Pin 3)

This is the inverting input to the PO– amplifier. The non–inverting input to the PO– amplifier is internally tied to the V_{AG} pin. The PI and PO– pins are used with external resistors in an inverting op amp gain circuit to set the gain of the PO+ and PO– push–pull power amplifier outputs. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance.

PO–
Power Amplifier Output (Inverting) (Pin 4)

This is the inverting power amplifier output, which is used to provide a feedback signal to the PI pin to set the gain of the push–pull power amplifier outputs. This pin is capable of driving a 300 Ω load to PO+. The PO+ and PO– outputs are differential (push–pull) and capable of driving a 300 Ω load to 3.15 V peak, which is 6.3 V peak–to–peak. The bias voltage and signal reference of this output is the V_{AG} pin. The V_{AG} pin cannot source or sink as much current as this pin, and therefore low impedance loads must be between PO+ and PO–. The PO+ and PO– differential drivers are also capable of driving a 100 Ω resistive load or a 100 nF Piezoelectric transducer in series with a 20 Ω resister with a smalll increase in distortion. These drivers may be used to drive resistive loads of ≥ 32 Ω when the gain of PO– is set to 1/4 or less. Connecting PI to V_{DD} will power down the power driver amplifiers, and the PO+ and PO– outputs will be high impedance. This pin is also high impedance when the device is powered down by the PDI pin.

PO+
Power Amplifier Output (Non–Inverting) (Pin 5)

This is the non–inverting power amplifier output, which is an inverted version of the signal at PO–. This pin is capable of driving a 300 Ω load to PO–. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance. This pin is also high impedance when the device is powered down by the PDI pin. See PI and PO– for more information.

DIGITAL INTERFACE

MCLK
Master Clock (Pin 11)

This is the master clock input pin. The clock signal applied to this pin is used to generate the internal 256 kHz clock and sequencing signals for the switched–capacitor filters, ADC, and DAC. The internal prescaler logic compares the clock on this pin to the clock at FST (8 kHz) and will automatically accept 256, 512, 1536, 1544, 2048, 2560, or 4096 kHz. For MCLK frequencies of 256 and 512 kHz, MCLK must be synchronous and approximately rising edge aligned to FST. For optimum performance at frequencies of 1.536 MHz and higher, MCLK should be synchronous and approximately rising edge aligned to the rising edge of FST. In many applications, MCLK may be tied to the BCLKT pin.

FST
Frame Sync, Transmit (Pin 14)

This pin accepts an 8 kHz clock that synchronizes the output of the serial PCM data at the DT pin. This input is compatible with both Long Frame Sync and Short Frame Sync. If both FST and FSR are held low for several 8 kHz frames, the device will power down. FST must be clocking for the device to power up affter being powered down by the frame syncs.

BCLKT
Bit Clock, Transmit (Pin 12)

This pin controls the transfer rate of transmit PCM data. In the synchronous modes of sign–bit extended and receive gain adjust, the BCLKT also controls the transfer rate of the receive PCM data. This pin can accept any bit clock frequency from 256 to 4096 kHz for Long Frame Sync and Short Frame Sync timing.

DT
Data, Transmit (Pin 13)

This pin is controlled by FST and BCLKT and is high impedance except when outputting PCM data. This pin is high impedance when the device is in the powered–down mode.

FSR
Frame Sync, Receive (Pin 7)

This pin accepts an 8 kHz clock, which synchronizes the input of the serial PCM data at the DR pin. FSR can be asynchronous to FST in the Long Frame Sync or Short Frame Sync modes.

BCLKR
Bit Clock, Receive (Pin 9)

This pin accepts any bit clock frequency from 256 to 4096 kHz. The BCLKR pin is also used as a mode select pin when not being clocked for several 8 kHz frames. The BCKLT pin is used to clock the receive PCM data transfers when the BCLKR pin is not being clocked. When the BCLKR pinis a logic 0, the sign–bit extended synchronous mode is selected, which uses 16–bit transfers with the first four bits being the sign bit. When the BCLKR pin is a logic 1, the receive gain adjust synchronous mode is selected, which uses a 13–bit transfer for the transmit PCM data, but uses a 16–bit transfer for the receive side, with the 13–bit voice data being first, followed by three bits which control the attenuation of the receive analog output.

DR
Data, Receive (Pin 8)

This pin is the PCM data input. See the pin descriptions for FSR, BCLKR, and BCKLT for more information.

FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of this device includes a low–noise, three–terminal op amp capable of driving a 2 kΩ load. This op amp has inputs of TI+ (Pin 19) and TI– (Pin 18) and its output is TG (Pin 17). This op amp is intended to be configured in an inverting gain circuit. The analog signal may be applied directly to the TG pin if this transmit op amp is independently powered down by connecting the TI+ input to the V_{DD} power supply. The TG pin becomes high impedance when the transmit op amp is powered down. The TG pin is internally connected to a 3–pole anti–aliasing pre–filter. This pre–filter incorporates a 2–pole Butterworth active low–pass filter, followed by a single passive pole. This pre–filter is followed by a single–ended to differential converter that is clocked at 512 kHz. All subsequent analog processing utilizes fully–differential circuitry. The next section is a fully–differential, 5–pole switched–capacitor low–pass filter with a 3.4 kHz frequency cutoff. After this filter is a 3–pole switched–capacitor high–pass filter having a cutoff frequency of about 200 Hz. This high–pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated op amp offsets in the preceding filter stages. The high–pass filter may be bypassed or removed from the signal path by the HB pin. When the high–pass filter is bypassed, the frequency response extends down to include dc. The last stage of the high–pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital–to–analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched–capacitor bandgap reference generates precise positive and negative reference voltages that are virtually independent of temperature and power supply voltage. A capacitor array (CDAC) is combined with a resistor string (RDAC) to implement the 13–bit linear DAC structure. The encode process uses the DAC, the voltage reference, and a frame–by–frame autozeroed comparator to implement a successive approximation conversion algorithm. All of the analog circuitry involved in the data conversion (the voltage reference, RDAC, CDAC, and comparator) are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a 5–pole, 3400 Hz switched capacitor low–pass filter with sinX/X correction, and a 2–pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is buffered by an amplifier, which is output at the RO– pin. This output is capable of driving a 2 kΩ load to the V_{AG} pin. The MC145482 also has a pair of power amplifiers that are connected in a push–pull configuration. The PI pin is the inverting input to the PO– power amplifier. The non–inverting input is internally tied to the V_{AG} pin. This allows this amplifier to be used in an inverting gain circuit with two external resistors. The PO+ amplifier has a gain of minus one, and is internally connected to the PO– output. This complete power amplifier circuit is a differential (push–pull) amplifier with adjustable gain. The power amplifier may be powered down independently of the rest of the chip by connecting the PI pin to V_{DD}.

The calibration level for both ADC and DAC of this 13–bit linear PCM Codec–Filter is referenced to Mu–Law with the same bit voltage weighting about the zero crossing. This results in the 0 dBm0 calibration level being 3.20 dB below the peak sinusoidal level before clipping. Based on the reference voltage of 1.575 V, the calibration level is 0.775 Vrms or 0 dBm at 600 Ω.

The MC145482 has the ability to attenuate the receive analog output when used in the receive gain adjust mode. This mode is accessed by applying a logic high to the BCLKR pin while the rest of the clock pins are clocked normally. This allows three additional bits that will be used to control the gain of the analog output to be clocked into the DR pin following the 13 bits of voice data. Table 1 shows the attenuation values and the corresponding digital codes.

Table 1. Receive Gain Adjust Mode Coefficients and Attenuation Weightings

Coefficient	Attenuation in dB
000	0
001	– 3
010	– 6
011	– 9
100	– 12
101	– 15
110	– 18
111	– 21

POWER–DOWN

There are two methods of putting this device into a low power consumption mode, which makes the device nonfunctional and consumes virtually no power. PDI is the power–down input pin which, when taken low, powers down the device. Another way to power the device down is to hold both the FST and FSR pins low while the BCLKT and MCLK pins are clocked. When the chip is powered down, the V_{AG}, TG, RO–, PO+, PO–, and DT outputs are high impedance and the V_{AG} Ref pin is pulled to the V_{DD} power supply with a non–linear, high–impedance circuit. To return the chip to the power–up state, PDI must be high and the FST frame sync pulse must be present while the BCLKT and MCLK pins are clocked. The DT output will remain in a high–impedance state for at least two 8 kHz FST pulses after power–up.

MASTER CLOCK

Since this codec–filter design has a single DAC architecture, the MCLK pin is used as the master clock for all analog signal processing including analog–to–digital conversion, digital–to–analog conversion, and for transmit and receive filtering functions of this device. The clock frequency applied to the MCLK pin may be 256 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, 2.56 MHz, or 4.096 MHz. This device has a prescaler that automatically determines the proper divide ratio to use for the MCLK input, which achieves the required 256 kHz internal sequencing clock. The clocking requirements of the MCLK input are independent of the PCM data transfer mode (i.e., Long Frame Sync, Short Frame Sync, whether the device is used in the synchronous modes or not).

DIGITAL I/O

The MC145482 is a 13–bit linear device using 2s complement data format. Table 2 shows the 13–bit data word format for the maximum positive code and negative zero and full–scale.

Table 3 shows the series of eight 13–bit PCM words that correspond to a digital milliwatt. The digital milliwatt is the 1 kHz calibration signal reconstructed by the DAC that defines the absolute gain or 0 dBm0 transmission level point (TLP) of the DAC. The calibration level for this 13–bit linear ADC and DAC is referenced to Mu–Law with the same bit voltage weighting about the zero crossing. This results in the 0 dBm0 calibration level being 3.20 dB below the peak sinusoidal level before clipping. Refer to Figures 2a–2d for a summary and comparison of the four PCM data interface modes of this device.

Table 2. PCM Codes for Zero and Full–Scale

Level	Sign Bit	Magnitude Bits
+ Full Scale	0	1111 1111 1111
+ One Step	0	0000 0000 0001
Zero	0	0000 0000 0000
– One Step	1	1111 1111 1111
– Full Scale	1	0000 0000 0000

Table 3. PCM Codes for 1 kHz Digital Milliwatt

Level	Sign Bit	Magnitude Bits
$\pi/8$		
$3\pi/8$		
$5\pi/8$		
$7\pi/8$		
$9\pi/8$		
$11\pi/8$		
$13\pi/8$		
$15\pi/8$		

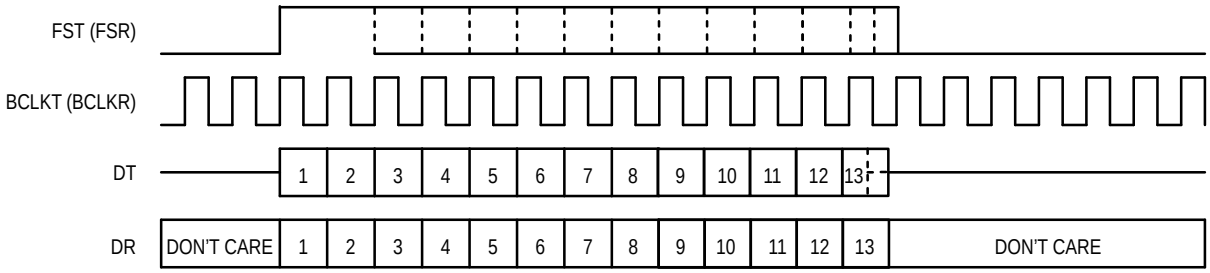


Figure 2a. Long Frame Sync (Transmit and Receive Have Individual Clocking)

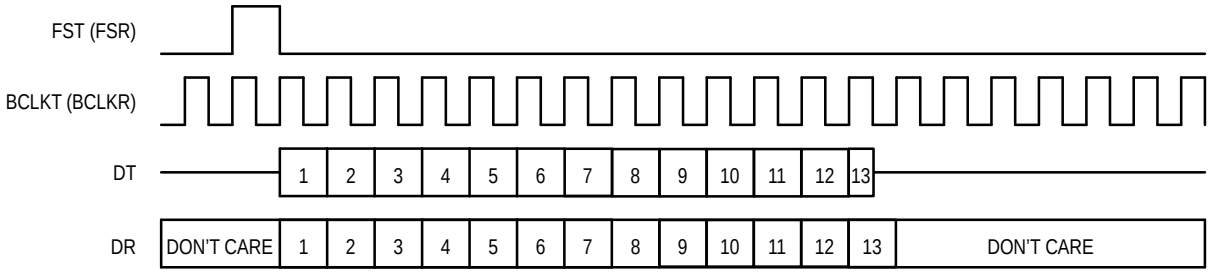


Figure 2b. Short Frame Sync (Transmit and Receive Have Individual Clocking)

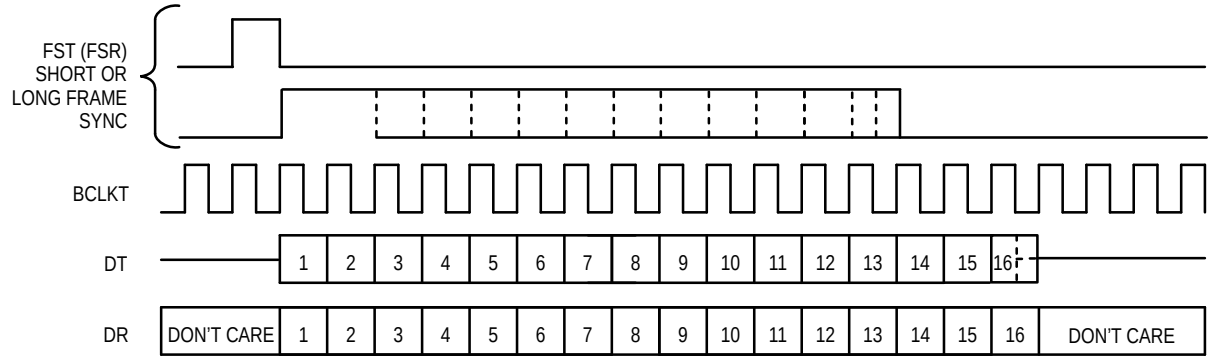


Figure 2c. Sign–Extended (BCLKR = 0)
Transmit and receive both use BCLKT, and the first four data bits are the sign bit.
FST may occur at a different time than FSR.

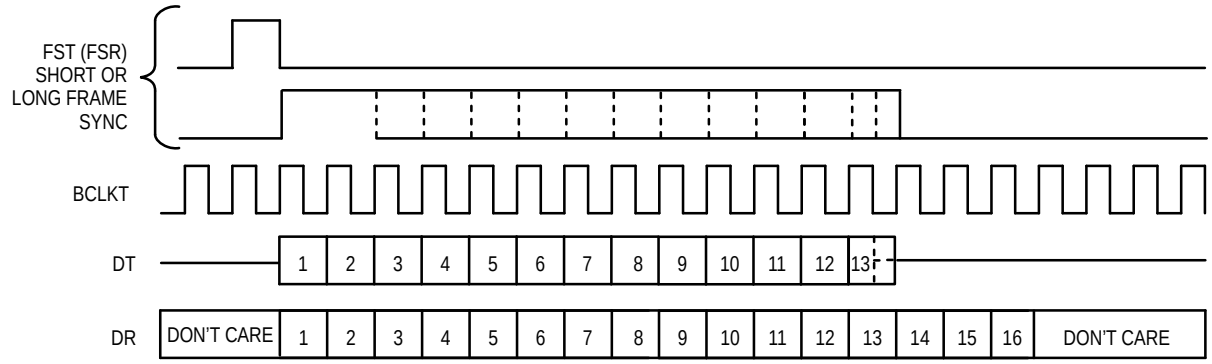


Figure 2d. Receive Gain Adjust (BCLKR = 1)
Transmit and receive both use BCLKT. FST may occur at a different time than FSR.
Bits 14, 15, and 16, clocked into DR, are used for attenuation control for the receive analog output.

Figure 2. Digital Timing Modes for the PCM Data Interface

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The MC145482 is manufactured using high–speed CMOS VLSI technology to implement the complex analog signal processing functions of a PCM Codec–Filter. The fully–differential analog circuit design techniques used for this device result in superior performance for the switched capacitor filters, the analog–to–digital converter (ADC) and the digital–to–analog converter (DAC). Special attention was given to the design of this device to reduce the sensitivities of noise, including power supply rejection and susceptibility to radio frequency noise. This special attention to design includes a fifth order low–pass filter, followed by a third order high–pass filter whose output is converted to a digital signal with greater than 75 dB of dynamic range, all operating on a single 5 V power supply. This results in an LSB size for small audio signals of about 386 μV. The typical idle channel noise level of this device is less than one LSB. In addition to the dynamic range of the codec–filter function of this device, the input gain–setting op amp has the capability of greater than 35 dB of gain intended for an electret microphone interface.

This device was designed for ease of implementation, but due to the large dynamic range and the noisy nature of the environment for this device (digital switches, radio telephones, DSP front–end, etc.) special care must be taken to assure optimum analog transmission performance.

PC BOARD MOUNTING

It is recommended that the device be soldered to the PC board for optimum noise performance. If the device is to be used in a socket, it should be placed in a low parasitic pin inductance (generally, low–profile) socket.

POWER SUPPLY, GROUND, AND NOISE CONSIDERATIONS

This device is intended to be used in switching applications which often require plugging the PC board into a rack with power applied. This is known as ''hot–rack insertion.'' In these applications care should be taken to limit the voltage on any pin from going positive of the V_{DD} pins, or negative of the V_{SS} pins. One method is to extend the ground and power contacts of the PCB connector. The device has input protection on all pins and may source or sink a limited amount of current without damage. Current limiting may be accomplished by series resistors between the signal pins and the connector contacts.

The most important considerations for PCB layout deal with noise. This includes noise on the power supply, noise generated by the digital circuitry on the device, and cross coupling digital or radio frequency signals into the audio signals of this device. The best way to prevent noise is to:

1. Keep digital signals as far away from audio signals as possible.
2. Keep radio frequency signals as far away from the audio signals as possible.
3. Use short, low inductance traces for the audio circuitry to reduce inductive, capacitive, and radio frequency noise sensitivities.
4. Use short, low inductance traces for digital and RF circuitry to reduce inductive, capacitive, and radio frequency radiated noise.
5. Bypass capacitors should be connected from the V_{DD}, V_{AG} Ref, and V_{AG} pins to V_{SS} with minimal trace length. Ceramic monolithic capacitors of about 0.1 μF are acceptable for the V_{DD} and V_{AG} Ref pins to decouple the device from its own noise. The V_{DD} capacitor helps supply the instantaneous currents of the digital circuitry in addition to decoupling the noise which may be generated by other sections of the device or other circuitry on the power supply. The V_{AG} Ref decoupling capacitor is effecting a low–pass filter to isolate the mid–supply voltage from the power supply noise generated on–chip, as well as external to the device. The V_{AG} decoupling capacitor should be about 0.01 μF. This helps to reduce the impedance of the V_{AG} pin to V_{SS} at frequencies above the bandwidth of the V_{AG} generator, which reduces the susceptiblility to RF noise.
6. Use a short, wide, low inductance trace to connect the V_{SS} ground pin to the power supply ground. The V_{SS} pin is the digital ground and the most negative power supply pin for the analog circuitry. All analog signal processing is referenced to the V_{AG} pin, but because digital and RF circuitry will probably be powered by this same ground, care must be taken to minimize high frequency noise in the V_{SS} trace. Depending on the application, a double–sided PCB with a V_{SS} ground plane connecting all of the digital and analog V_{SS} pins together would be a good grounding method. A multilayer PC board with a ground plane connecting all of the digital and analog V_{SS} pins together would be the optimal ground configuration. These methods will result in the lowest resistance and the lowest inductance in the ground circuit. This is important to reduce voltage spikes in the ground circuit resulting from the high speed digital current spikes. The magnitude of digitally induced voltage spikes may be hundreds of times larger than the analog signal the device is required to digitize.
7. Use a short, wide, low inductance trace to connect the V_{DD} power supply pin to the 5 V power supply. Depending on the application, a double–sided PCB with V_{DD} bypass capacitors to the V_{SS} ground plane, as described above, may complete the low impedance coupling for the power supply. For a multilayer PC board with a power plane, connecting all of the V_{DD} pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 5 V V_{DD} power circuit are essentially the same as for the V_{SS} ground circuit.
8. The V_{AG} pin is the reference for all analog signal processing. In some applications the audio signal to be digitized may be referenced to the V_{SS} ground. To reduce the susceptibility to noise at the input of the ADC section, the three–terminal op amp may be used in a differential to single–ended circuit to provide level conversion from the V_{SS} ground to the V_{AG} ground with noise cancellation. The op amp may be used for more than 35 dB of gain in microphone interface circuits, which will require a compact layout with minimum trace lengths as well as isolation from noise sources. It is recommended that the layout be as symmetrical as possible to avoid any imbalances which would reduce the noise cancelling benefits of this differential op amp circuit. Refer to the application schematics for examples of this circuitry.

If possible, reference audio signals to the V_{AG} pin instead of to the V_{SS} pin. Handset receivers and telephone line interface circuits using transformers may be audio signal referenced completely to the V_{AG} pin. Refer to the application schematics for examples of this circuitry. The V_{AG} pin cannot be used for ESD or line protection.

MAXIMUM RATINGS (Voltages Referenced to V_{SS} Pin)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to 6	V
Voltage on Any Analog Input or Output Pin		V_{SS} – 0.3 to V_{DD} + 0.3	V
Voltage on Any Digital Input or Output Pin		V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to +150	°C

POWER SUPPLY (T_A = – 40 to + 85°C)

Characteristics		Min	Typ	Max	Unit
DC Supply Voltage		4.75	5.0	5.25	V
Active Current Dissipation (V_{DD} = 5 V)	(No Load, PI ≥ V_{DD} – 0.5 V) (No Load, PI ≤ V_{DD} – 1.5 V)	— —	5.0 5.2	— —	mA
Power–Down Current (V_{IH} for Logic Levels Must be ≥ V_{DD} – 0.5 V)	$\overline{PDI}$ = V_{SS} FST and FSR = V_{SS}, PDI = V_{DD}	— —	0.001 0.01	— —	mA

DIGITAL LEVELS (V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_A = – 40 to + 85°C)

Characteristics	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	—	0.6	V
Input High Voltage	V_{IH}	2.4	—	V
Output Low Voltage (DT Pin, I_{OL}= 2.5 mA)	V_{OL}	—	0.4	V
Output High Voltage (DT Pin, I_{OH} = – 2.5 mA)	V_{OH}	V_{DD} – 0.5	—	V
Input Low Current ($V_{SS} \le V_{in} \le V_{DD}$)	I_{IL}	– 10	+ 10	µA
Input High Current ($V_{SS} \le V_{in} \le V_{DD}$)	I_{IH}	– 10	+ 10	µA
Output Current in High Impedance State ($V_{SS} \le DT \le V_{DD}$)	I_{OZ}	– 10	+ 10	µA
Input Capacitance of Digital Pins (Except DT)	C_{in}	—	10	pF
Input Capacitance of DT Pin when High–Z	C_{out}	—	15	pF

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_A = – 40 to + 85°C)

Characteristics		Min	Typ	Max	Unit
Input Current	TI+, TI–	—	± 0.1	± 1.0	μA
Input Resistance to V_{AG} (V_{AG} – 0.5 V ≤ V_{in} ≤ V_{AG} + 0.5 V)	TI+, TI–	10	—	—	MΩ
Input Capacitance	TI+, TI–	—	—	10	pF
Input Offset Voltage of TG Op Amp	TI+, TI–	—	—	± 5	mV
Input Common Mode Voltage Range	TI+, TI–	1.2		V_{DD} – 1.2	V
Input Common Mode Rejection Ratio	TI+, TI–	—	TBD	—	dB
Gain Bandwidth Product (10 kHz) of TG Op Amp (R_L ≥ 10 kΩ)		—	3000	—	kHz
DC Open Loop Gain of TG Op Amp (R_L ≥ 10 kΩ)		—	95	—	dB
Equivalent Input Noise (C–Message) Between TI+ and TI– at TG		—	– 30	—	dBrnC
Output Load Capacitance for TG Op Amp		0	—	100	pF
Output Voltage Range for TG	(R_L = 2 kΩ to V_{AG})	0.5	—	V_{DD} – 0.5	V
Output Current (0.5 V ≤ V_{out} ≤ V_{DD} – 0.5 V)	TG, RO–	± 1.0	—	—	mA
Output Load Resistance to V_{AG}	TG, RO–	2	—	—	kΩ
Output Impedance	RO–	—	1	—	Ω
Output Load Capacitance	RO–	0	—	500	pF
DC Output Offset Voltage of RO– Referenced to V_{AG}		—	—	± 25	mV
V_{AG} Output Voltage Referenced to V_{SS} (No Load)		V_{DD}/2 – 0.1	V_{DD}/2	V_{DD}/2 + 0.1	V
V_{AG} Output Current with ± 25 mV Change in Output Voltage		± 2.0	± 10	—	mA
Power Supply Rejection Ratio (0 to 100 kHz @100 mVrms Applied to V_{DD}, C–Message Weighting, All Analog Signals Referenced to V_{AG} Pin)	Transmit Receive	TBD TBD	TBD TBD	— —	dBC
Power Drivers PI, PO+, PO–					
Input Current (V_{AG} – 0.5 V ≤ PI ≤ V_{AG} + 0.5 V)	PI	—	± 0.05	± 1.0	μA
Input Resistance (V_{AG} – 0.5 V ≤ PI ≤ V_{AG} + 0.5 V)	PI	10	—	—	MΩ
Input Offset Voltage	PI	—	—	± 20	mV
Output Offset Voltage of PO+ Relative to PO– (Inverted Unity Gain for PO–)		—	—	± 50	mV
Output Current (V_{SS} + 0.7 V ≤ PO+ or PO– ≤ V_{DD} – 0.7 V)		± 10	—	—	mA
PO+ or PO– Output Resistance (Inverted Unity Gain for PO–)		—	1	—	Ω
Gain Bandwidth Product (10 kHz, Open Loop for PO–)		—	1000	—	kHz
Load Capacitance (PO+ or PO– to V_{AG}, or PO+ to PO–)		0	—	1000	pF
Gain of PO+ Relative to PO– (R_L = 300 Ω, + 3 dBm0, 1 kHz)		– 0.2	0	+ 0.2	dB
Total Signal to Distortion at PO+ and PO– with a Differential Load of: 100 nF in series with ≥ 20 Ω ≥ 100 Ω	300 Ω	45 — —	60 40 40	— — —	dBC
Power Supply Rejection Ratio (0 to 25 kHz @ 100 mVrms Applied to V_{DD}. PO– Connected to PI. Differential or Measured Referenced to V_{AG} Pin.)	0 to 4 kHz 4 to 25 kHz	TBD —	TBD TBD	— —	dB

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, All Analog Signals Referenced to V_{AG}, 0 dBm0 = 0.775 Vrms = 0 dBm @ 600 Ω, FST = FSR = 8 kHz, BCLKT = MCLK = 2.048 MHz Synchronous Operation, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Characteristics		A/D			D/A			Units
		Min	Typ	Max	Min	Typ	Max	
Peak Single Frequency Tone Amplitude without Clipping	T_{max}	—	1.575	—	—	1.575	—	Vpk
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{DD} = 5.0 V)		– 0.25	—	+ 0.25	– 0.25	—	+ 0.25	dB
Absolute Gain Variation with Temperature	0 to + 70°C	—	TBD	—	—	TBD	—	dB
	– 40 to + 85°C	—	TBD	—	—	TBD	—	
Absolute Gain Variation with Power Supply (T_A = 25°C)		—	TBD	—	—	TBD	—	dB
Total Distortion, 1.02 kHz Tone (C–Message Weighting)								
	+ 3 dBm0	—	55	—	—	60	—	dBC
	0 dBm0	—	58	—	—	60	—	
	– 10 dBm0	—	58	—	—	60	—	
	– 20 dBm0	—	53	—	—	55	—	
	– 30 dBm0	—	44	—	—	46	—	
	–40 dBm0	—	34	—	—	36	—	
	–50 dBm0	—	24	—	—	26	—	
	–60 dBm0	—	14	—	—	16	—	
Idle Channel Noise (For End–to–End and A/D, See Note 1)								
	(C–Message Weighted)	—	—	17	—	—	11	dBrnc0
	(Psophometric Weighted)	—	—	– 69	—	—	– 79	dBm0p
Frequency Response	15 Hz	—	—	– 40	– 0.5	—	0	dB
(Relative to 1.02 kHz @ 0 dBm0) (HB = 0)	50 Hz	—	—	– 30	– 0.5	—	0	
	60 Hz	—	—	– 26	– 0.5	—	0	
	165 Hz	—	– 3	—	– 0.5	—	0	
	200 Hz	– 1.0	—	– 0.4	– 0.5	—	0	
	300 to 3000 Hz	– 0.20	—	+ 0.20	– 0.20	—	+ 0.20	
	3300 Hz	– 0.35	—	+ 0.20	– 0.35	—	+ 0.20	
	3400 Hz	– 0.9	—	0	– 0.9	—	0	
	3600 Hz	—	– 3	—	—	– 3	—	
	4000 Hz	—	—	– 14	—	—	– 14	
	4600 Hz to 100 kHz	—	—	– 32	—	—	– 30	
Out–of–Band Spurious at V_{AG} Ref (300 to 3400 Hz @ 0 dBm0 in)								
	4600 to 7600 Hz	—	—	—	—	—	– 30	dB
	7600 to 8400 Hz	—	—	—	—	—	– 40	
	8400 to 100,000 Hz	—	—	—	—	—	– 30	
Idle Channel Noise Selective (8 kHz, Input = V_{AG}, 30 Hz Bandwidth)		—	—	—	—	—	– 70	dBm0
Absolute Delay (1600 Hz) (HB = 0)		—	—	315	—	—	205	µs
Group Delay Referenced to 1600 Hz (HB = 0)	500 to 600 Hz	—	—	210	– 40	—	—	µs
	600 to 800 Hz	—	—	130	– 40	—	—	
	800 to 1000 Hz	—	—	70	– 40	—	—	
	1000 to 1600 Hz	—	—	35	– 30	—	—	
	1600 to 2600 Hz	—	—	70	—	—	85	
	2600 to 2800 Hz	—	—	95	—	—	110	
	2800 to 3000 Hz	—	—	145	—	—	175	
Crosstalk of 1020 Hz @ 0 dBm0 from A/D or D/A (Note 2)		—	—	– 75	—	—	– 75	dB

NOTES:

1. Extrapolated from a 1020 Hz @ – 50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while stimulated with 2667 Hz @ – 50 dBm0.

DIGITAL SWITCHING CHARACTERISTICS, LONG FRAME SYNC AND SHORT FRAME SYNC

(V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, All Digital Signals Referenced to V_{SS}, T_A = – 40 to + 85°C, C_L = 150 pF, FST = FSR = 8 kHz, Unless Otherwise Noted)

Ref. No.	Characteristics	Min	Typ	Max	Unit
1	Master Clock Frequency for MCLK	— — — — — — —	256 512 1536 1544 2048 2560 4096	— — — — — — —	kHz
1	MCLK Duty Cycle for 256 kHz Operation	45	—	55	%
2	Minimum Pulse Width High for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
3	Minimum Pulse Width Low for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
4	Rise Time for All Digital Signals	—	—	50	ns
5	Fall Time for All Digital Signals	—	—	50	ns
6	Setup Time from MCLK Low to FST High	50	—	—	ns
7	Setup Time from FST High to MCLK Low	50	—	—	ns
8	Bit Clock Data Rate for BCLKT or BCLKR	256	—	4096	kHz
9	Minimum Pulse Width High for BCLKT or BCLKR	50	—	—	ns
10	Minimum Pulse Width Low for BCLKT or BCLKR	50	—	—	ns
11	Hold Time from BCLKT (BCLKR) Low to FST (FSR) High	20	—	—	ns
12	Setup Time for FST (FSR) High to BCLKT (BCLKR) Low	80	—	—	ns
13	Setup Time from DR Valid to BCLKR Low	0	—	—	ns
14	Hold Time from BCLKR Low to DR Invalid	50	—	—	ns
	LONG FRAME SPECIFIC TIMING				
15	Hold Time from 2nd Period of BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
16	Delay Time from FST or BCLKT, Whichever is Later, to DT for Valid MSB Data	—	—	60	ns
17	Delay Time from BCLKT High to DT for Valid Data	—	—	60	ns
18	Delay Time from the Later of the 13th (16th for Sign–Extended Mode) BCLKT Falling Edge, or the Falling Edge of FST to DT Output High Impedance	10	—	60	ns
19	Minimum Pulse Width Low for FST or FSR	50	—	—	ns
	SHORT FRAME SPECIFIC TIMING				
20	Hold Time from BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
21	Setup Time from FST (FSR) Low to MSB Period of BCLKT (BCLKR) Low	50	—	—	ns
22	Delay Time from BCLKT High to DT Data Valid	10	—	60	ns
23	Delay Time from the 13th (16th for Sign–Extended Mode) BCLKT Low to DT Output High Impedance	10	—	60	ns

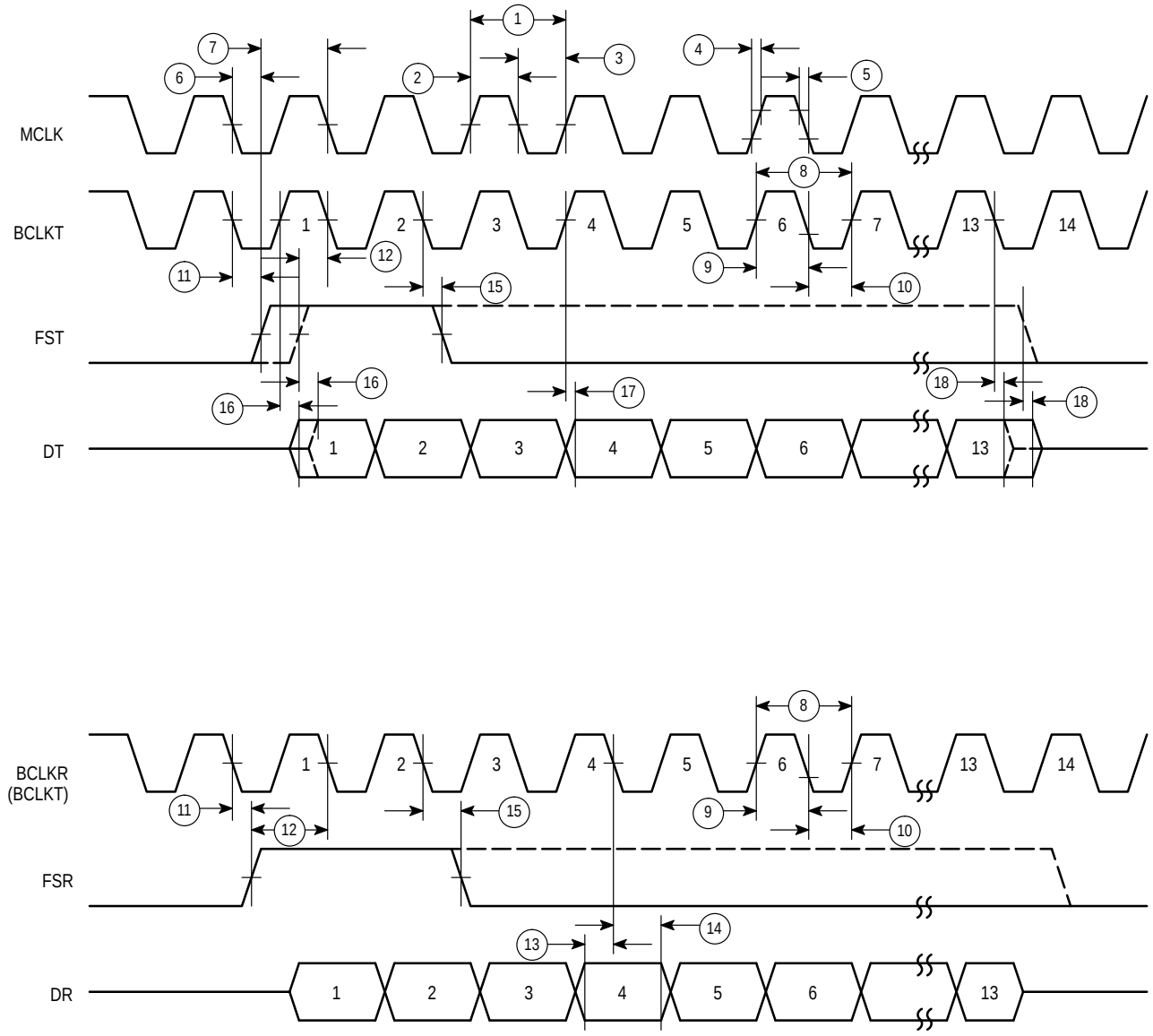


Figure 3. Long Frame Sync Timing

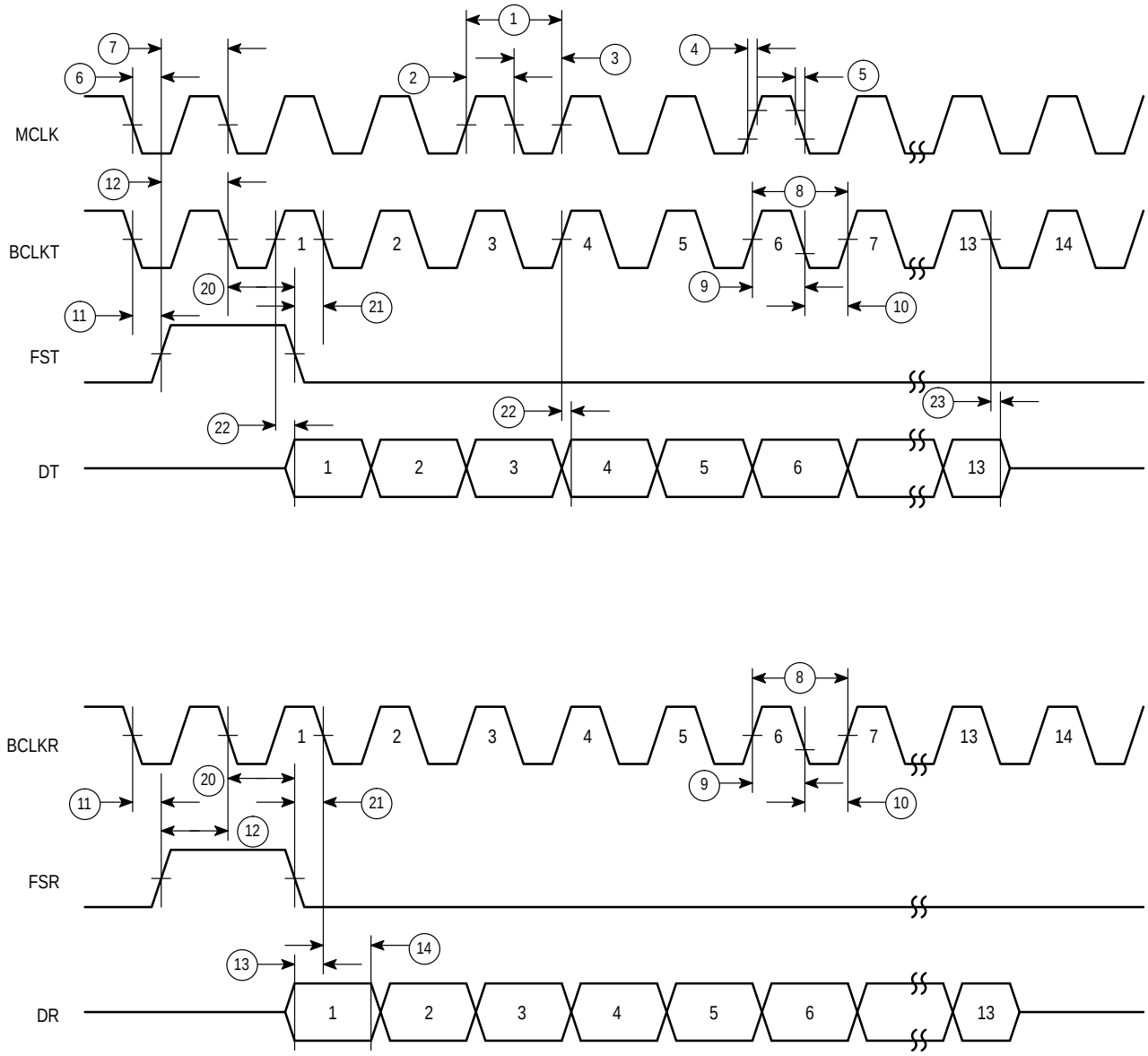


Figure 4. Short Frame Sync Timing

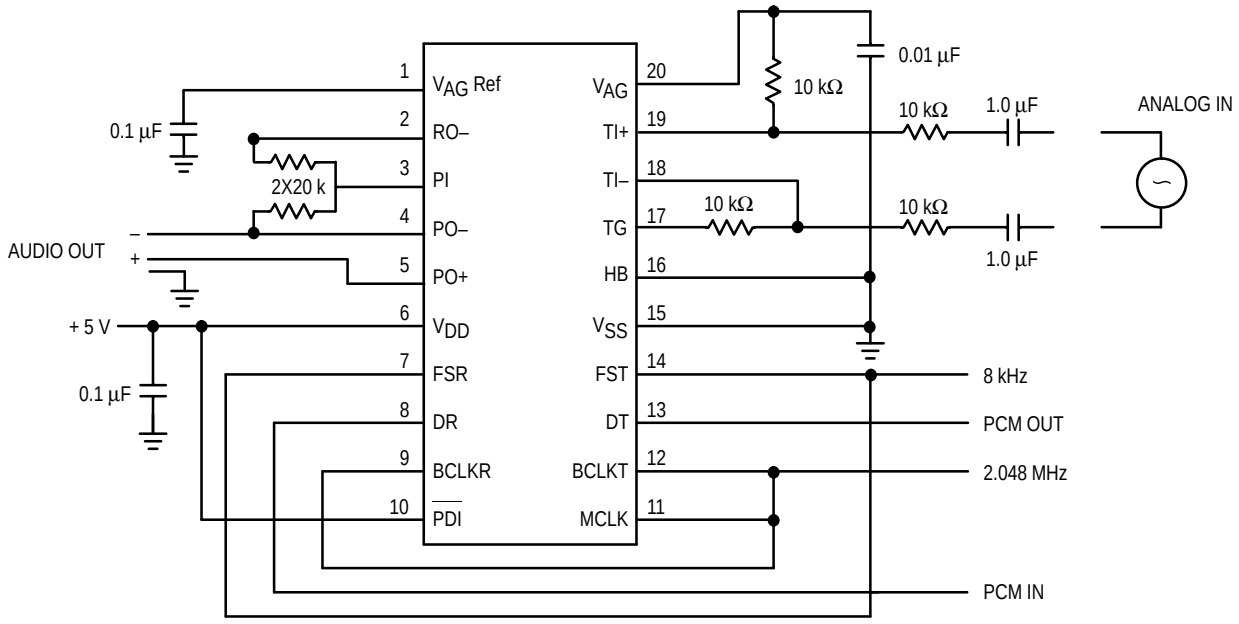


Figure 5. MC145482 Test Circuit — Signals Referenced to V_{AG} Pin

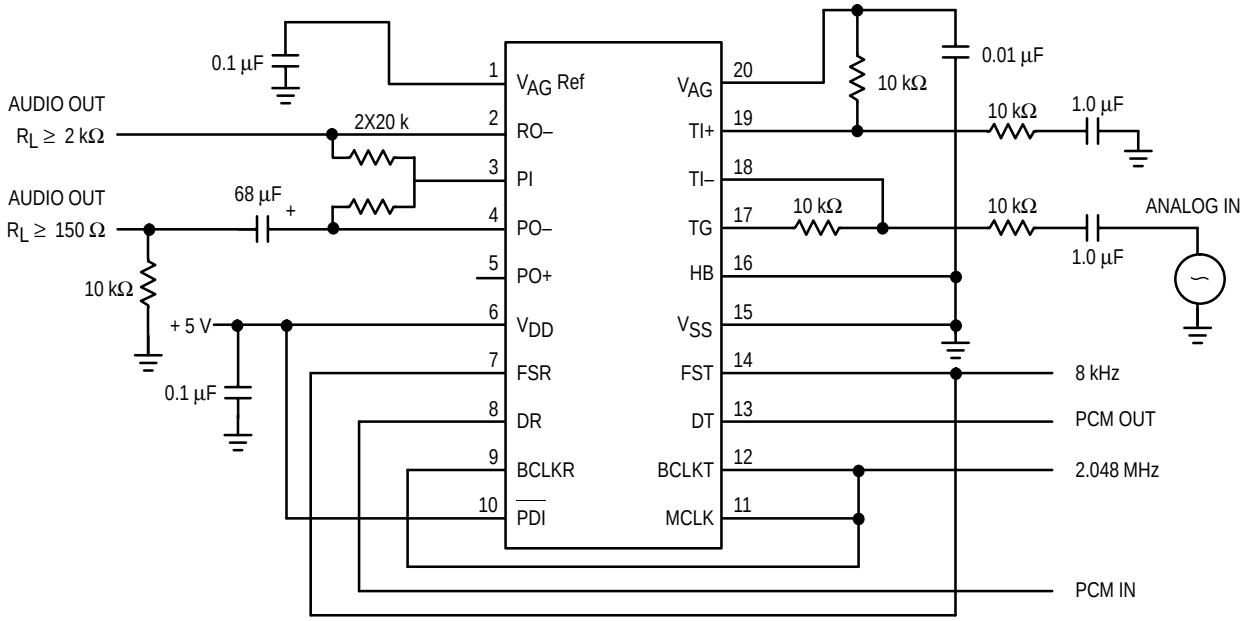


Figure 6. MC145482 Test Circuit — Signals Referenced to V_{SS}

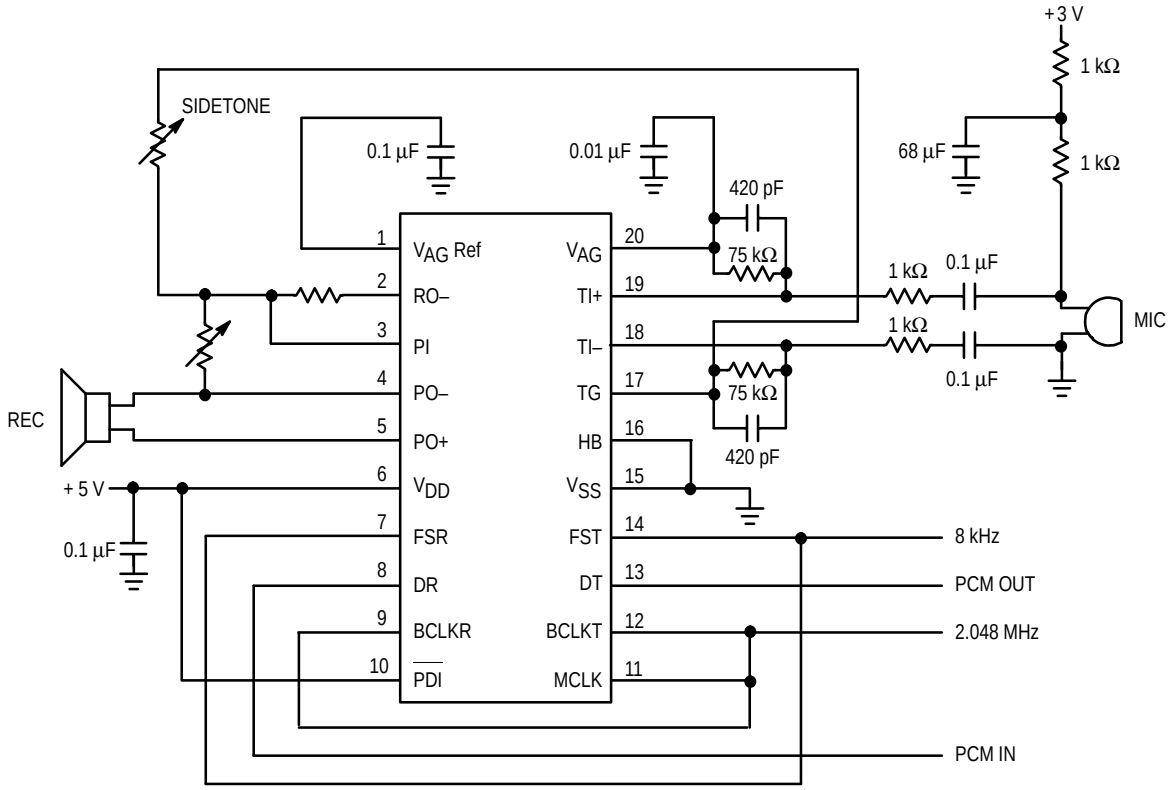


Figure 7. MC145482 Handset Interface

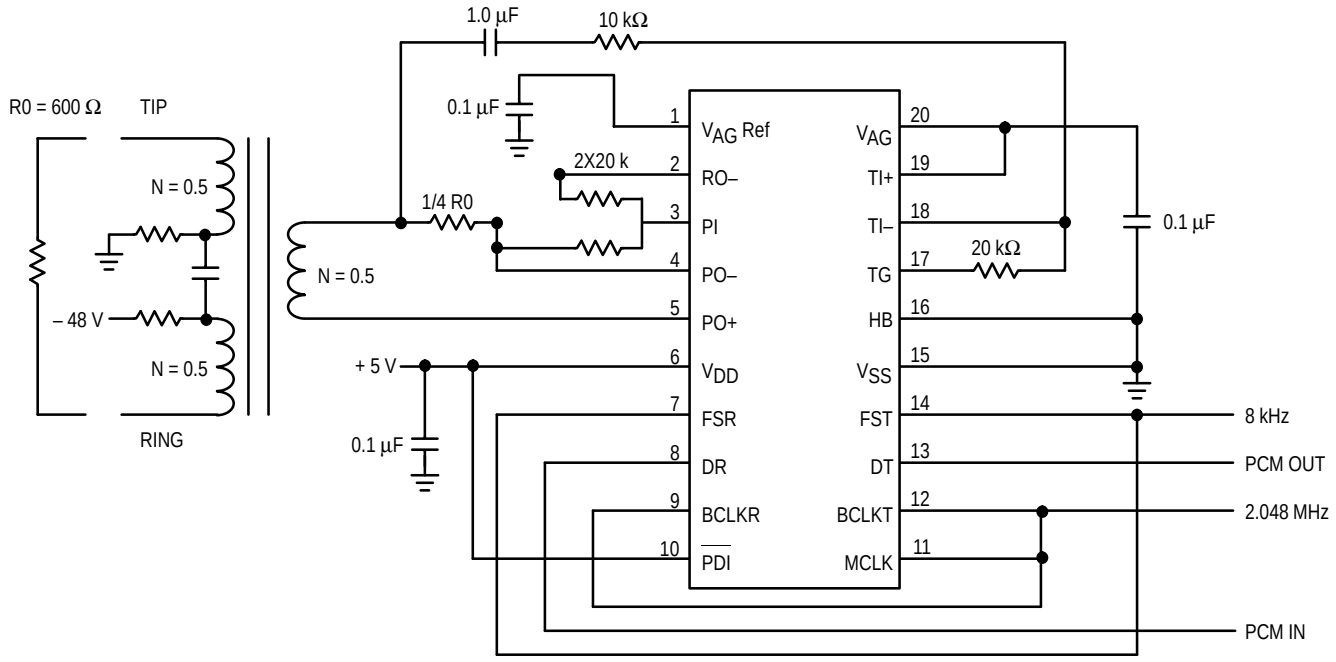
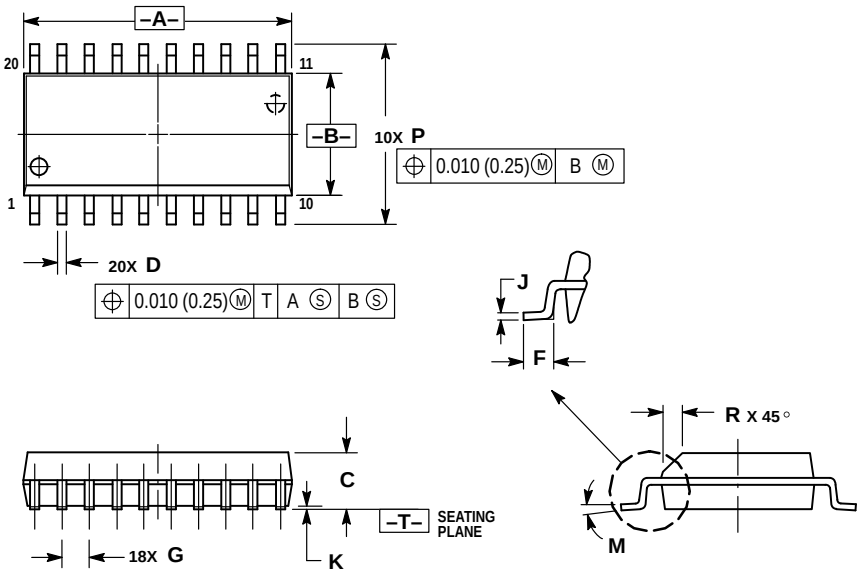


Figure 8. MC145482 Step–Up Transformer Line Interface

PACKAGE DIMENSIONS

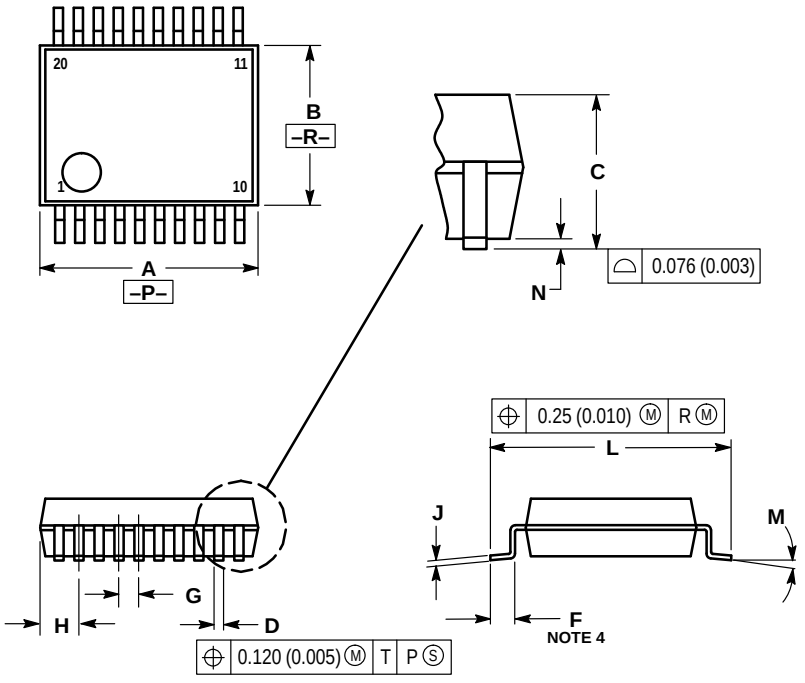
DW SUFFIX
SOG PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX
SSOP
CASE 940C–02



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15MM PER SIDE.
4. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
6. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.10	7.30	0.280	0.287
B	5.20	5.38	0.205	0.212
C	1.75	1.99	0.069	0.078
D	0.25	0.38	0.010	0.015
F	0.65	1.00	0.026	0.039
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.10	0.20	0.004	0.008
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°
N	0.05	0.21	0.002	0.008

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3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298