

New product

MITSUBISHI MICROCOMPUTERS M37733S4BFP

16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37733S4BFP is a microcomputer using the 7700 Family core. This microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the RAM, multiple-function timers, serial I/O, A-D converter, and so on.

FEATURES

- Number of basic instructions 103
- Memory size RAM 2048 bytes
- Instruction execution time
The fastest instruction at 25 MHz frequency 160 ns
- Single power supply 5 V ± 10 %
- Low power dissipation (At 25 MHz frequency)..... 47.5 mW (Typ.)
- Interrupts 19 types, 7 levels
- Multiple-function 16-bit timer 5 + 3
- Serial I/O (UART or clock synchronous)..... 3
- 10-bit A-D converter 8-channel inputs
- 12-bit watchdog timer

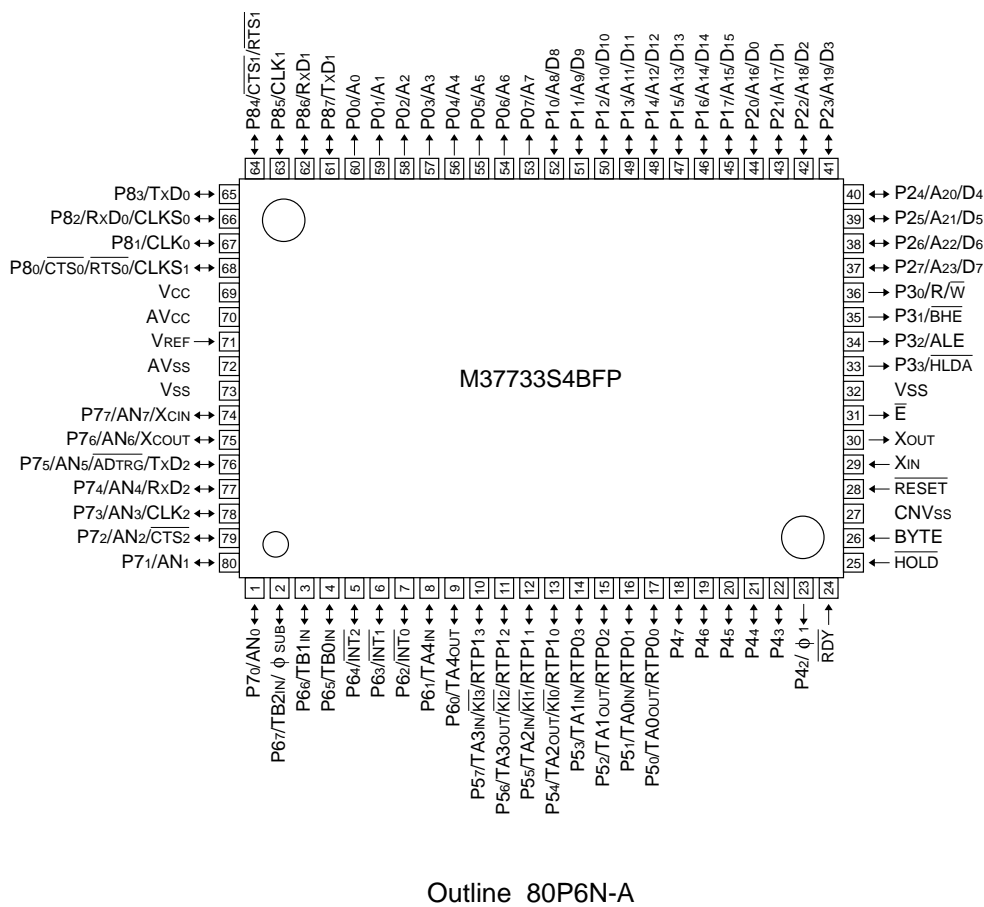
- Programmable input/output
(ports P4, P5, P6, P7, P8) 37
- Clock generating circuit 2 circuits built-in

APPLICATION

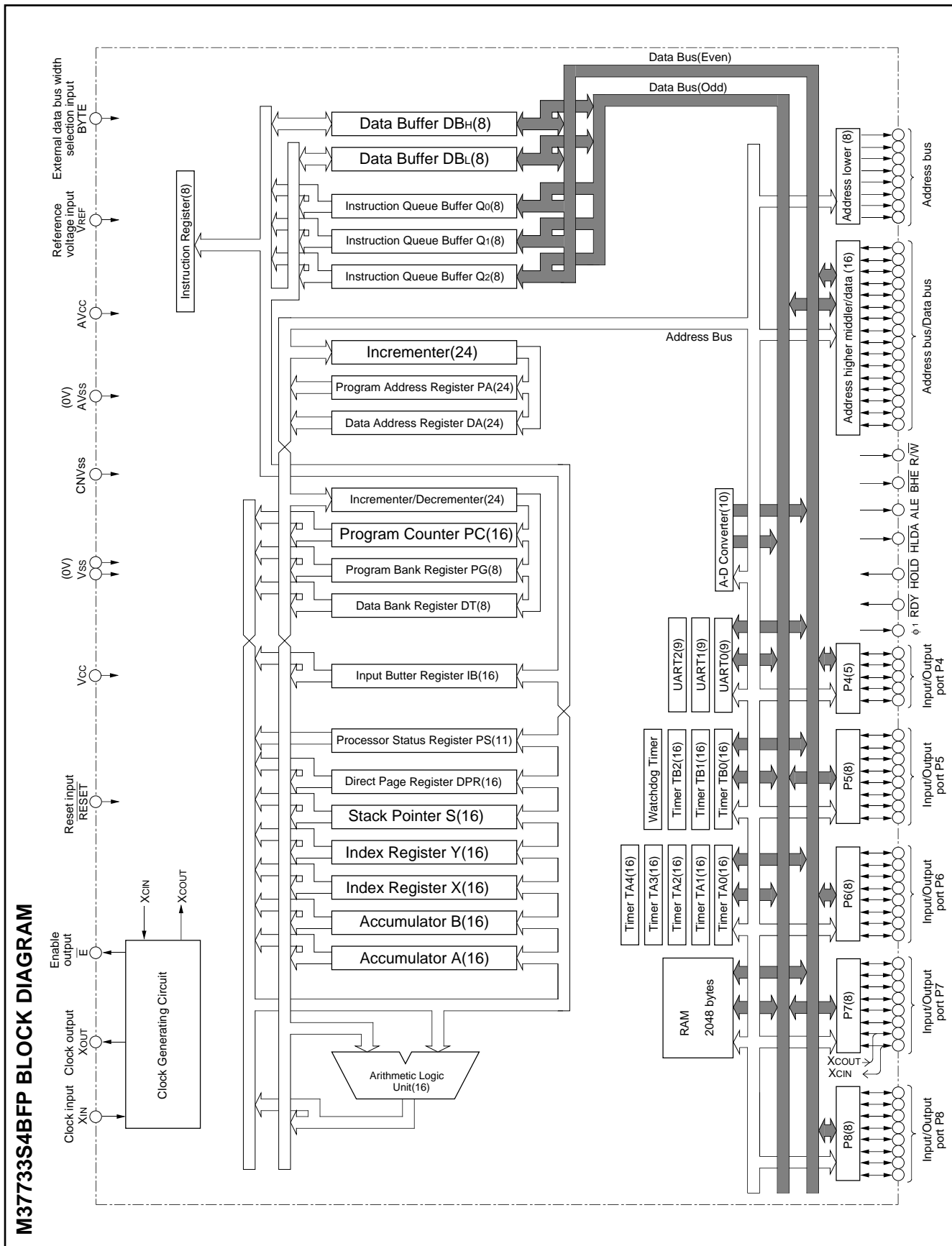
Control devices for general commercial equipment such as office automation, office equipment, personal information equipment, and so on.

Control devices for general industrial equipment such as communication equipment, and so on.

PIN CONFIGURATION (TOP VIEW)



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FUNCTIONS OF M37733S4BFP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		160 ns (the fastest instruction at external clock 25 MHz frequency)
Memory size	RAM	2048 bytes
Input/Output ports	P5 – P8	8-bit X 4
	P4	5-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		5 V ± 10 %
Power dissipation		47.5 mW (at external clock 25 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16 Mbytes
Operating temperature range		-20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded QFP (80P6N-A)

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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 5 V \pm 10 % to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	Connect to Vcc.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
E	Enable output	Output	When output level of E signal is "L", data/instruction read or data write is performed.
BYTE	Bus width selection input	Input	This pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P0/A0 – P07/A7	Address (low-order) output	Output	Address (A0 – A7) is output.
P10/A8/D8 – P17/A15/D15	Address (middle-order) output/data (high-order) I/O	I/O	When the BYTE pin is set to "L" and external data bus has a 16-bit width, high-order data (D8 – D15) is input/output or an address (A8 – A15) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A8 – A15) is output.
P20/A16/D0 – P27/A23/D7	Address (high-order) output/data (low-order) I/O	I/O	Low-order data (D0 – D7) is input/output or an address (A16 – A23) is output.
P30/R/W	Read/Write output	Output	"H" indicates the read status and "L" indicates the write status.
P31/BHE	Byte high enable output	Output	"L" is output when an odd-numbered address is accessed.
P32/ALE	Address latch enable output	Output	This is used to retrieve only the address from address and data multiplex signal.
P33/HLDA	Hold acknowledge output	Output	This outputs "L" level when the microcomputer enters hold state after a hold request is accepted.
HOLD	Hold request input	Input	This is an input pin for HOLD request signal. The microcomputer enters into hold state while this signal is "L".
RDY	Ready input	Input	This is an input pin for RDY signal. The microcomputer enters into ready state while this signal is "L".
P42/ ϕ 1	Clock output	Output	This pin outputs the clock ϕ 1.
P43 – P47	I/O port P4	I/O	These pins become a 5-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset.
P50 – P57	I/O port P5	I/O	In addition to having the same functions as port P4, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input (KI0 – KI3).
P60 – P67	I/O port P6	I/O	In addition to having the same functions as port P4, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{\text{INT}}_0$ – $\overline{\text{INT}}_2$) and input pins for timers B0 to B2. P67 also functions as sub-clock ϕ SUB output pin.
P70 – P77	I/O port P7	I/O	In addition to having the same functions as port P4, these pins function as input pins for A-D converter. P72 to P75 also function as I/O pins for UART2. Additionally, P76 and P77 have the function as the output pin (XCOUT) and the input pin (XCIN) of the sub-clock (32 kHz) oscillation circuit, respectively. When P76 and P77 are used as the XCOUT and XCIN pins, connect a resonator or an oscillator between the both.
P80 – P87	I/O port P8	I/O	In addition to having the same functions as port P4, these pins also function as I/O pins for UART 0 and UART 1.

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BASIC FUNCTION BLOCKS

The M37733S4BFP has the same functions as the M37733MHBXXXFP except for the following :

- (1) The memory map is different.
- (2) The processor mode is different.
- (3) The reset circuit is different.
- (4) Pulse output port mode of timer A is available.
- (5) The function of ROM area modification is not available.

MEMORY

The memory map is shown in Figure 1. The address space has a capacity of 16 Mbytes and is allocated to addresses from 0₁₆ to FFFFFFF₁₆. The address space is divided by 64-Kbyte unit called bank. The banks are numbered from 0₁₆ to FF₁₆.

Built-in RAM and control registers for internal peripheral devices are assigned to bank 0₁₆.

Addresses FFD6₁₆ to FFFF₁₆ are the RESET and interrupt vector addresses and contain the interrupt vectors. Use ROM for memory of this address.

The 2048-byte area allocated to addresses from 80₁₆ to 87F₁₆ is the built-in RAM. In addition to storing data, the RAM is used as stack during a subroutine call or interrupts.

Peripheral devices such as I/O ports, A-D converter, serial I/O, timer, and interrupt control registers are allocated to addresses from 0₁₆ to 7F₁₆.

A 256-byte direct page area can be allocated anywhere in bank 0₁₆ by using the direct page register (DPR). In the direct page addressing mode, the memory in the direct page area can be accessed with two words. Hence program steps can be reduced.

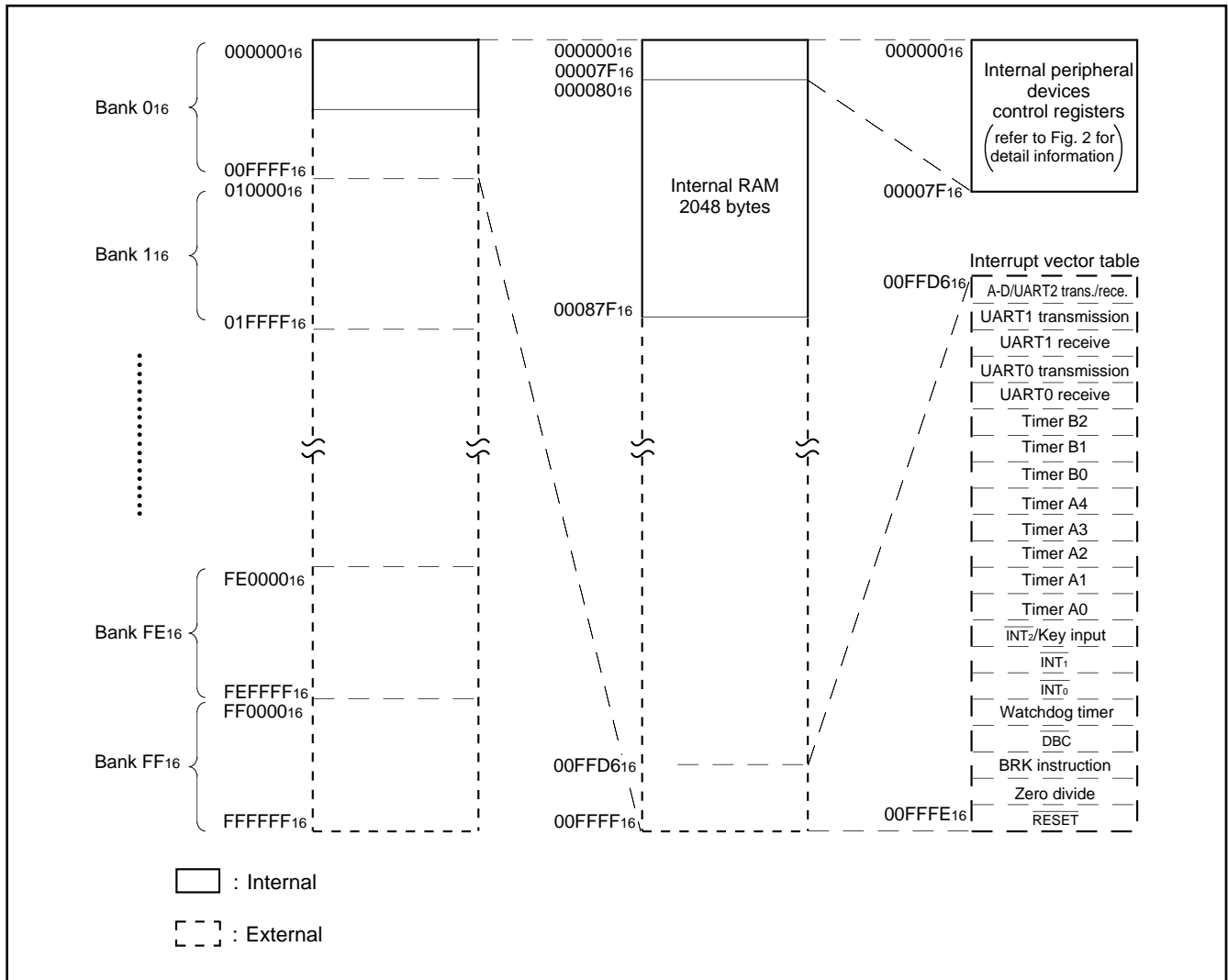


Fig. 1 Memory map

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Address (Hexadecimal notation)		Address (Hexadecimal notation)	
000000		000040	Count start flag
000001		000041	
000002	Port P0 register	000042	One-shot start flag
000003	Port P1 register	000043	
000004	Port P0 direction register	000044	Up-down flag
000005	Port P1 direction register	000045	
000006	Port P2 register	000046	Timer A0 register
000007	Port P3 register	000047	
000008	Port P2 direction register	000048	Timer A1 register
000009	Port P3 direction register	000049	
00000A	Port P4 register	00004A	Timer A2 register
00000B	Port P5 register	00004B	
00000C	Port P4 direction register	00004C	Timer A3 register
00000D	Port P5 direction register	00004D	
00000E	Port P6 register	00004E	Timer A4 register
00000F	Port P7 register	00004F	
000010	Port P6 direction register	000050	Timer B0 register
000011	Port P7 direction register	000051	
000012	Port P8 register	000052	Timer B1 register
000013		000053	
000014	Port P8 direction register	000054	Timer B2 register
000015		000055	
000016		000056	Timer A0 mode register
000017		000057	Timer A1 mode register
000018		000058	Timer A2 mode register
000019		000059	Timer A3 mode register
00001A		00005A	Timer A4 mode register
00001B		00005B	Timer B0 mode register
00001C	Pulse output data register 1	00005C	Timer B1 mode register
00001D	Pulse output data register 0	00005D	Timer B2 mode register
00001E	A-D control register 0	00005E	Processor mode register 0
00001F	A-D control register 1	00005F	Processor mode register 1
000020	A-D register 0	000060	Watchdog timer register
000021		000061	Watchdog timer frequency selection flag
000022	A-D register 1	000062	Waveform output mode register
000023		000063	Reserved area (Note)
000024	A-D register 2	000064	UART2 transmit/receive mode register
000025		000065	UART2 baud rate register (BRG2)
000026	A-D register 3	000066	UART2 transmission buffer register
000027		000067	UART2 transmit/receive control register 0
000028	A-D register 4	000068	UART2 transmit/receive control register 1
000029		000069	UART2 receive buffer register
00002A	A-D register 5	00006A	
00002B		00006B	Oscillation circuit control register 0
00002C	A-D register 6	00006C	Port function control register
00002D		00006D	Serial transmit control register
00002E	A-D register 7	00006E	Oscillation circuit control register 1
00002F		00006F	A-D/UART2 trans./rece. interrupt control register
000030	UART 0 transmit/receive mode register	000070	UART 0 transmission interrupt control register
000031	UART 0 baud rate register (BRG0)	000071	UART 0 receive interrupt control register
000032	UART 0 transmission buffer register	000072	UART 1 transmission interrupt control register
000033		000073	UART 1 receive interrupt control register
000034	UART 0 transmit/receive control register 0	000074	Timer A0 interrupt control register
000035	UART 0 transmit/receive control register 1	000075	Timer A1 interrupt control register
000036	UART 0 receive buffer register	000076	Timer A2 interrupt control register
000037		000077	Timer A3 interrupt control register
000038	UART 1 transmit/receive mode register	000078	Timer A4 interrupt control register
000039	UART 1 baud rate register (BRG1)	000079	Timer B0 interrupt control register
00003A	UART 1 transmission buffer register	00007A	Timer B1 interrupt control register
00003B		00007B	Timer B2 interrupt control register
00003C	UART 1 transmit/receive control register 0	00007C	INT ₀ interrupt control register
00003D	UART 1 transmit/receive control register 1	00007D	INT ₁ interrupt control register
00003E	UART 1 receive buffer register	00007E	
00003F		00007F	INT ₂ /Key input interrupt control register

Note . Do not write to this address.

Fig. 2 Location of internal peripheral devices and interrupt control registers

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Pulse output port mode

The pulse motor drive waveform can be output by using plural internal timer A.

Figure 3 shows a block diagram for pulse output port mode. In the pulse output port mode, two pairs of four-bit pulse output ports are used. Whether using pulse output port or not can be selected by waveform output selection bit (bit 0, bit 1) of waveform output mode register (62₁₆ address) shown in Figure 4. When bit 0 of waveform output selection bit is set to "1", RTP10, RTP11, RTP12, and RTP13 are used as pulse output ports, and when bit 1 of waveform output selection bit is set to "1", RTP00, RTP01, RTP02, and RTP03 are used as pulse output ports. When bits 1 and 0 of waveform output selection bit are set to "1", RTP10, RTP11, RTP12, and RTP13, and RTP00, RTP01, RTP02, and RTP03 are used as pulse output ports. The ports not used as pulse output ports can be used as normal parallel ports, timer input/output or key input interrupt input.

In the pulse output port mode, set timers A0 and A2 to timer mode as timers A0 and A2 are used. Figure 5 shows the bit configuration of timer A0, A2 mode registers in pulse output port mode.

Data can be set in each bit of the pulse output data register corresponding to four ports selected as pulse output ports. Figure 6

shows the bit configuration of the pulse output data register. The contents of the pulse output data register 1 (low-order four bits of 1C₁₆ address) corresponding to RTP10, RTP11, RTP12, and RTP13 is output to the ports each time the counter of timer A2 becomes 0000₁₆. The contents of the pulse output data register 0 (low-order four bits of 1D₁₆ address) corresponding to RTP00, RTP01, RTP02, and RTP03 is output to the ports each time the counter of timer A0 becomes 0000₁₆.

Figure 7 shows example of waveforms in pulse output port mode. When "0" is written to a specified bit of the pulse output data register, "L" level is output to the corresponding pulse output port when the counter of corresponding timer becomes 0000₁₆, and when "1" is written, "H" level is output to the pulse output port.

Pulse width modulation can be applied to each pulse output port. Since pulse width modulation involves the use of timers A1 and A3, activate these timers in pulse width modulation mode.

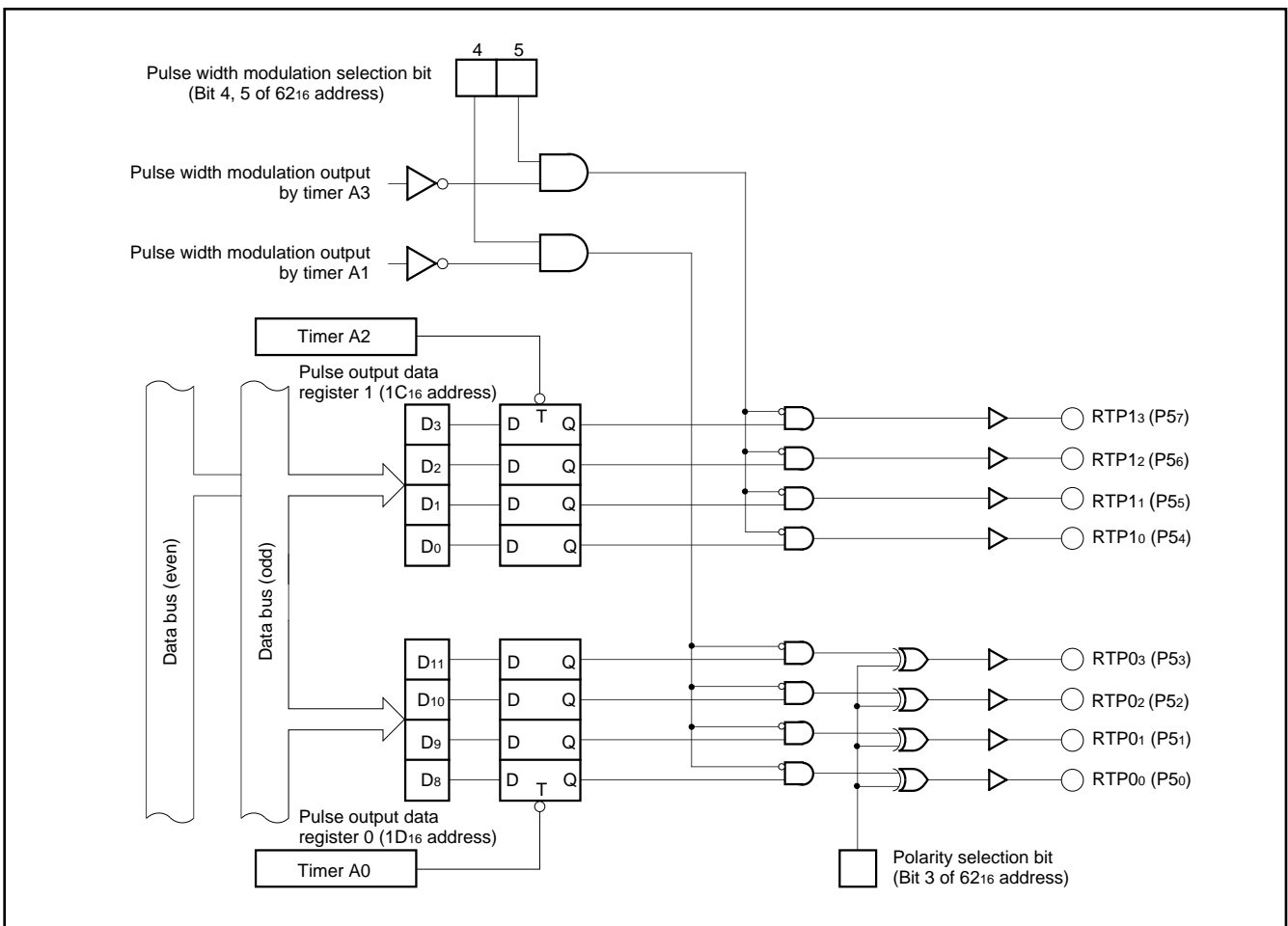


Fig. 3 Block diagram for pulse output port mode

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RTP10, RTP11, RTP12, and RTP13 are applied pulse width modulation by timer A3 by setting the pulse width modulation selection bit by timer A3 (bit 5) of the waveform output mode register to "1".

RTP00, RTP01, RTP02, and RTP03 are applied pulse width modulation by timer A1 by setting the pulse width modulation selection bit by timer A1 (bit 4) of the waveform output mode register to "1".

The contents of the pulse output data register 0 can be reversed and output to pulse output ports RTP00, RTP01, RTP02, and RTP03 by the polarity selection bit (bit 3) of the waveform output mode register. When the polarity selection bit is "0", the contents of the pulse output data register 0 is output unchangeably, and when "1", the contents of the pulse output data register 0 is reversed and output. When pulse width modulation is applied, likewise the polarity reverse to pulse width modulation can be selected by the polarity selection bit.

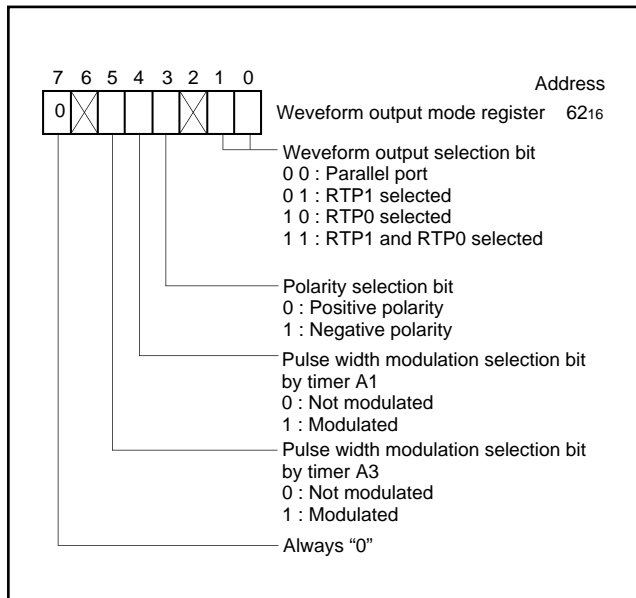


Fig. 4 Waveform output mode register bit configuration

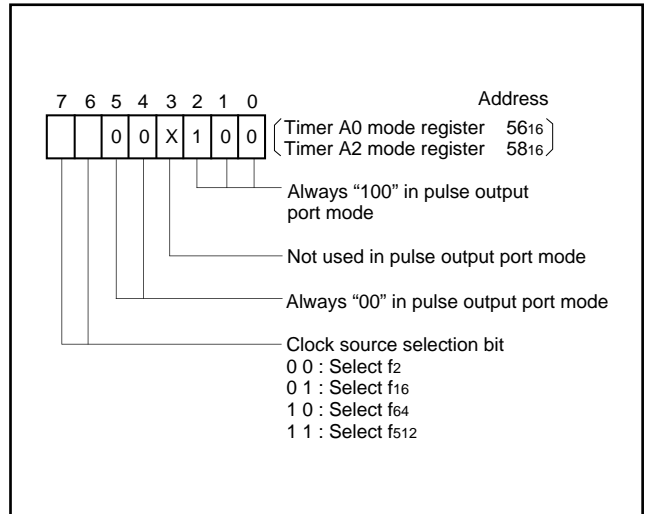


Fig. 5 Timer A0, A2 mode register bit configuration in pulse output port mode

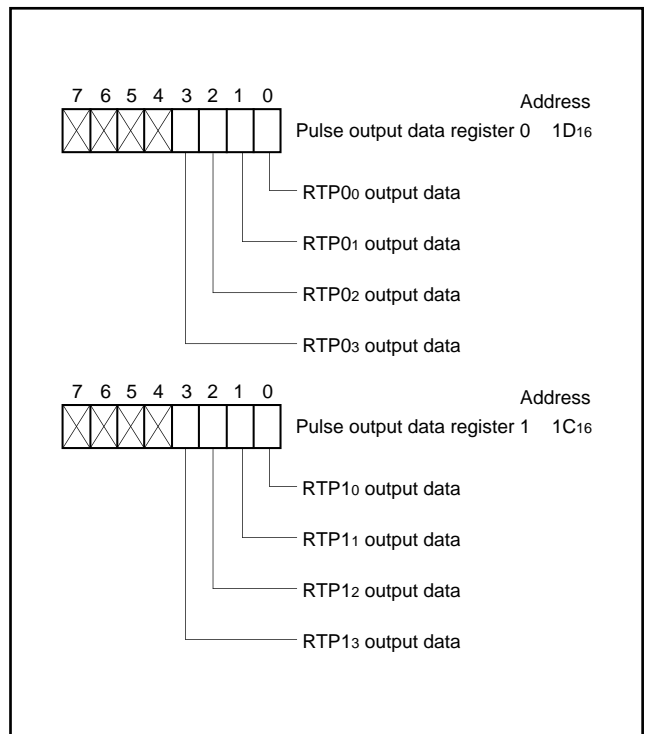


Fig. 6 Pulse output data register bit configuration

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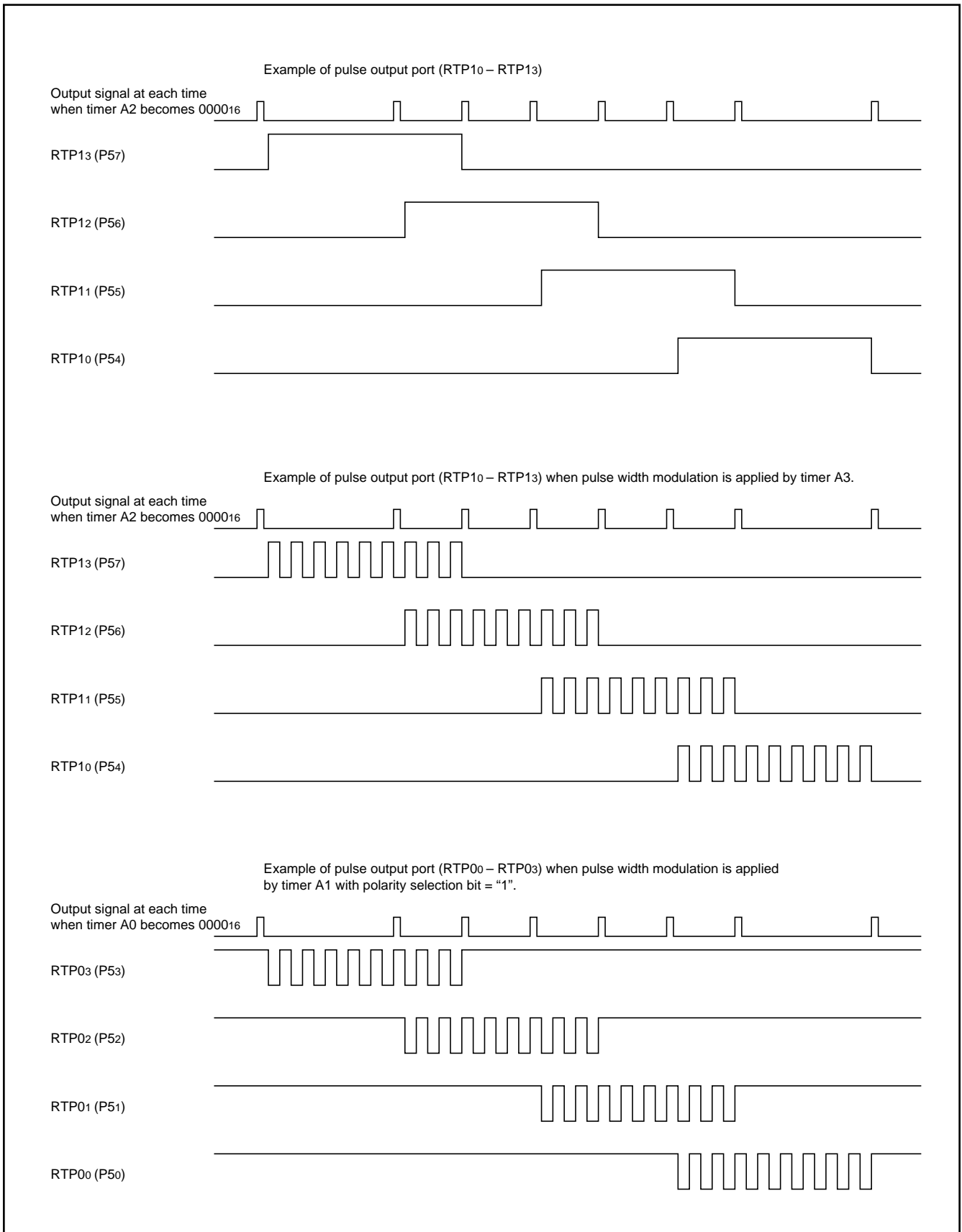


Fig. 7 Example of waveforms in pulse output port mode

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PROCESSOR MODE

The bits 0 of processor mode register 0 as shown in Figure 8 is used to select which mode of microprocessor mode, and evaluation chip mode.

Figure 9 shows functions of P0₀/A₀ to P4₇ pins in each mode.

The external memory area also changes when the mode changes.

Figure 10 shows the memory map for each mode.

The accessing of the external memory is affected by the BYTE pin, the bit 2 (wait bit) of processor mode register 0, and bit 0 (wait selection bit) of processor mode register 1.

• BYTE pin

When accessing the external memory, the level of the BYTE pin is used to determine whether to use the data bus as 8-bit width or 16-bit width.

The data bus width is 8 bits when the level of the BYTE pin is "H", and P2₀/A₁₆/D₀ to P2₇/A₂₃/D₇ pins become the data I/O pins.

The data bus width is 16 bits when the level of the BYTE pin is "L", and both P2₀/A₁₆/D₀ to P2₇/A₂₃/D₇ pins and P1₀/A₈/D₈ to P1₇/A₁₅/D₁₅ pins become the data I/O pins.

When accessing the internal memory, the data bus width is always 16 bits regardless of the BYTE pin level.

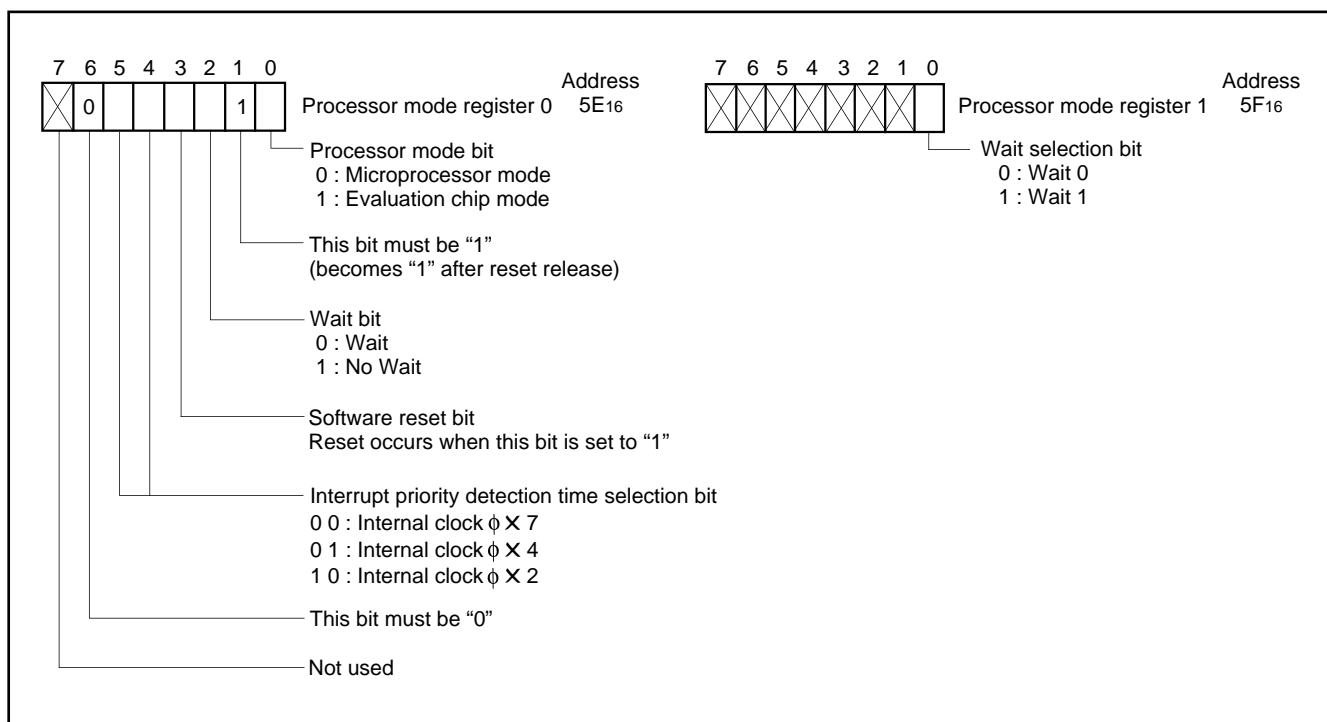


Fig. 8 Processor mode register bit configuration

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Pin	PM ₁	1	1
	PM ₀	0	1
Mode	Microprocessor mode		Evaluation Chip mode
P00/A0 - P07/A7	\bar{E}		Same as left
P10/A8/D8 P17/A15/D15	BYTE = "L"		Same as left
	BYTE = "H"		 Ports P4, P5 and their direction registers are treated as 16-bit wide bus.
P20/A16/D0 P27/A23/D7	BYTE = "L"		Same as left
	BYTE = "H"		 Ports P4, P5 and their direction registers are treated as 16-bit wide bus.
P30/R/W, P31/BHE, P32/ALE, P33/HLDA	\bar{E}		Same as left
HOLD, RDY, P42/phi 1, P43 to P47	\bar{E}		

Fig. 9 Relationship between pins P00/A0 to P47 and processor modes

Note. The signal output disable selection bit (bit 6 of the oscillation circuit control register 0) can stop the $\phi 1$ output in the microprocessor mode. In the microprocessor mode, signal \bar{E} can also be fixed to "H" when the internal memory area is accessed.

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• Wait bit

As shown in Figure 11, when the external memory area is accessed with the processor mode register 0 (address 5E16) bit 2 (wait bit) cleared to "0", the access time can be extended compared with no wait (the wait bit is "1").

The access time is extended in two ways and this is selected with bit 0 (wait selection bit) of processor mode register 1 (address 5F16). When this bit is "1", the access time is 1.5 times compared to that for no wait. When this bit is "0", the access time is twice compared to that for no wait.

At reset, the wait bit and the wait selection bit are "0".

The accessing of internal memory area is performed in no wait mode regardless of the wait bit.

The processor modes are described below.

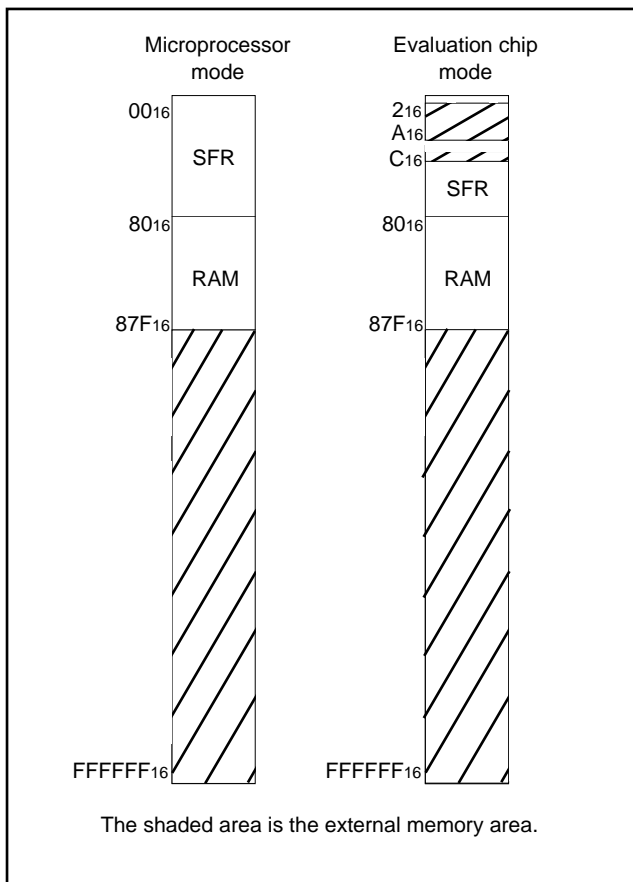


Fig. 10 External memory area for each processor mode

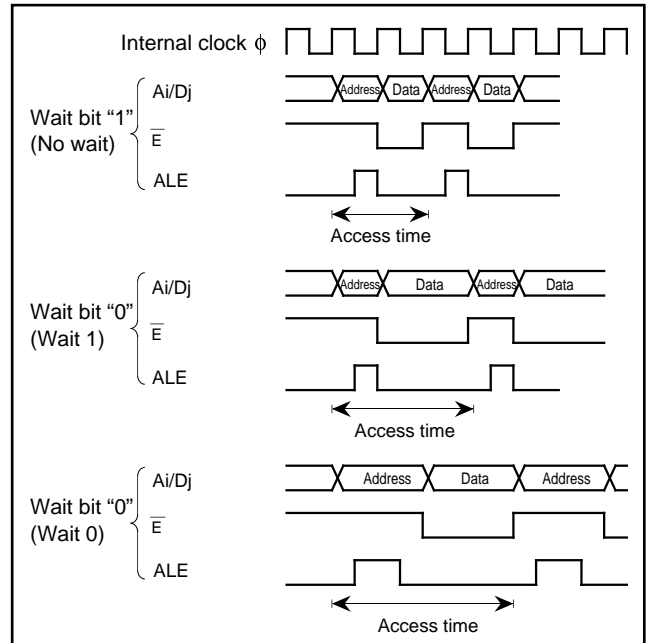


Fig. 11 Relationship between wait bit, wait selection bit, and access time

(1) Microprocessor mode [10]

Microprocessor mode is entered by connecting the CNVss pin to Vcc and starting from reset.

Signal E-bar is output from pin E-bar and is "L" during the data/instruction code read or data write term. When the internal memory area is read or written, E-bar can be fixed to "H" by setting the signal output disable selection bit (bit 6 of oscillation circuit control register 0) to "1".

P00/A0 to P07/A7 pins become address output pins.

P10/A8/D8 to P17/A15/D15 pins have two functions depending on the level of the BYTE pin.

When the BYTE pin level is "L", P10/A8/D8 to P17/A15/D15 pins function as an address output pin while E-bar is "H" and as an odd address data I/O pin while E-bar is "L". However, if an internal memory is read, external data is ignored while E-bar is "L".

When the BYTE pin level is "H", P10/A8/D8 to P17/A15/D15 pins function as an address output pin.

When the BYTE pin level is "L", P20/A16/D0 to P27/A23/D7 pins function as an address output pin while E-bar is "H" and as an even address data I/O pin while E-bar is "L". However, if an internal memory is read, external data is ignored while E-bar is "L".

R-bar/W is a read/write signal which indicates a read when it is "H" and a write when it is "L".

BHE is a byte high enable signal which indicates that an odd address is accessed when it is "L".

Therefore, two bytes at even and odd addresses are accessed simultaneously if address A0 is "L" and BHE is "L".

ALE is an address latch enable signal used to latch the address signal from a multiplexed signal of address and data. The latch is transparent while ALE is "H" to let the address signal pass through and held while ALE is "L".

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HLDA is a hold acknowledge signal and is used to notify externally when the microcomputer receives HOLD input and enters hold state. HOLD is a hold request signal. It is an input signal used to put the microcomputer in hold state. HOLD input is accepted when the internal clock ϕ falls from "H" level to "L" level while the bus is not used. P00/A0 to P07/A7 pins, P10/A8/D8 to P17/A15/D15 pins, P20/A16/D0 to P27/A23/D7 pins, P30/R/W pin, and P31/BHE pin are floating while the microcomputer stays in hold state. These pins are floating after one cycle of the internal clock ϕ later than HLD A signal changes to "L" level. At the removing of hold state, these ports are removed from floating state after one cycle of internal clock ϕ later than HLD A signal changes to "H" level.

RDY is a ready signal. If this signal goes "L", the internal clock ϕ stops at "L". RDY is used when slow external memory is attached. P42/ ϕ 1 pin is an output pin for clock ϕ 1. The ϕ 1 output is independent of RDY and does not stop even when internal clock ϕ stops because of "L" input to the RDY pin. As shown in Table 2, ϕ 1 output can also be stopped with the signal output disable selection bit "1". In this case, write "1" to the port P42 direction register.

(2) Evaluation chip mode [11]

Evaluation chip mode is entered by applying voltage twice the Vcc voltage to the CNVss pin. This mode is normally used for evaluation tools.

The functions of E, P00/A0 to P07/A7 pins, R/W, BHE, ALE, and HLD A are the same as those in microprocessor mode.

P10/A8/D8 to P17/A15/D15 pins function as address output pins while E is "H" and as data I/O pin of odd addresses while E is "L" regardless of the BYTE pin level. However, if an internal memory is read, external data is ignored while E is "L". P20/A16/D0 to P27/A23/D7 pins function as address output pins while E is "H" and as data I/O pin of even addresses while E is "L" when the BYTE pin level is "L". However, if an internal memory is read, external data is ignored while E is "L". When the BYTE pin level is "H" or 2•Vcc, port P2 functions as an address output pin while E is "H" and as data I/O pin of even and odd addresses while E is "L". However, if an internal memory is read, external data is ignored while E is "L".

Port P4 and its data direction which are located at address 0A16 and 0C16 are treated differently in evaluation chip mode. When these

addresses are accessed, the data bus width is treated as 16 bits regardless of the BYTE pin level, and the access cycle is treated as internal memory regardless of the wait bit.

The functions of HOLD and RDY are the same as those in microprocessor mode. Clock ϕ 1 from P42/ ϕ 1 pin is always output regardless of signal output disable selection bit.

Ports P43 to P46 become MX, QCL, VDA, and VPA output pins respectively. Port P47 becomes the DBC input pin.

The MX signal normally contents of flag m, but the contents of flag x is output if the CPU is using flag x.

QCL is the queue buffer clear signal. It becomes "H" when the instruction queue buffer is cleared, for example, when a jump instruction is executed.

VDA is the valid data address signal. It becomes "H" while the CPU is reading data from data buffer or writing data to data buffer. It also becomes "H" when the first byte of the instruction (operation code) is read from the instruction queue buffer.

VPA is the valid program address signal. It becomes "H" while the CPU is reading an instruction code from the instruction queue buffer.

DBC is the debug control signal and is used for debugging. Table 1 shows the relationship between the CNVss pin input levels and processor modes.

Table 1. Relationship between CNVss pin input levels and processor modes

CNVss	Mode	Description
Vss	• Microprocessor (• Evaluation chip)	Microprocessor mode upon starting after reset.
2 • Vcc	• Evaluation chip	Evaluation chip mode only.

Table 2. Function of signal output disable selection bit CM6 (bit 6 of oscillation circuit control register 0)

Processor mode	Pin	Function	
		CM6 = "0"	CM6 = "1"
Microprocessor mode	E	E is output when the internal/external memory area is accessed. After WIT/STP instruction is executed, "H" is output.	E is output only when the external memory area is accessed. "L" is output after WIT/STP instruction is executed. * Standby state selection bit (bit 0 of port function control register) must be set to "1".
	ϕ 1	Clock ϕ 1 is output.	"H" or "L" is output. (Output the content of P42 latch.) * Port P42 direction register must be set to "1".

Note. Functions shown in Table 2 cannot be emulated in a debugger.

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RESET CIRCUIT

The microcomputer is released from the reset state when the RESET pin is returned to "H" level after holding it at "L" level with the power source voltage at 5 V ± 10 %. Program execution starts at the address formed by setting address A23 – A16 to 0016, A15 – A8 to the contents of address FFFF16, and A7 – A0 to the contents of address FFFE16. Figure 12 shows the status of the internal registers during reset. Figure 13 shows an example of a reset circuit. If the stabilized clock

is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.9 V or less when the power source voltage reaches 4.5 V. If a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.

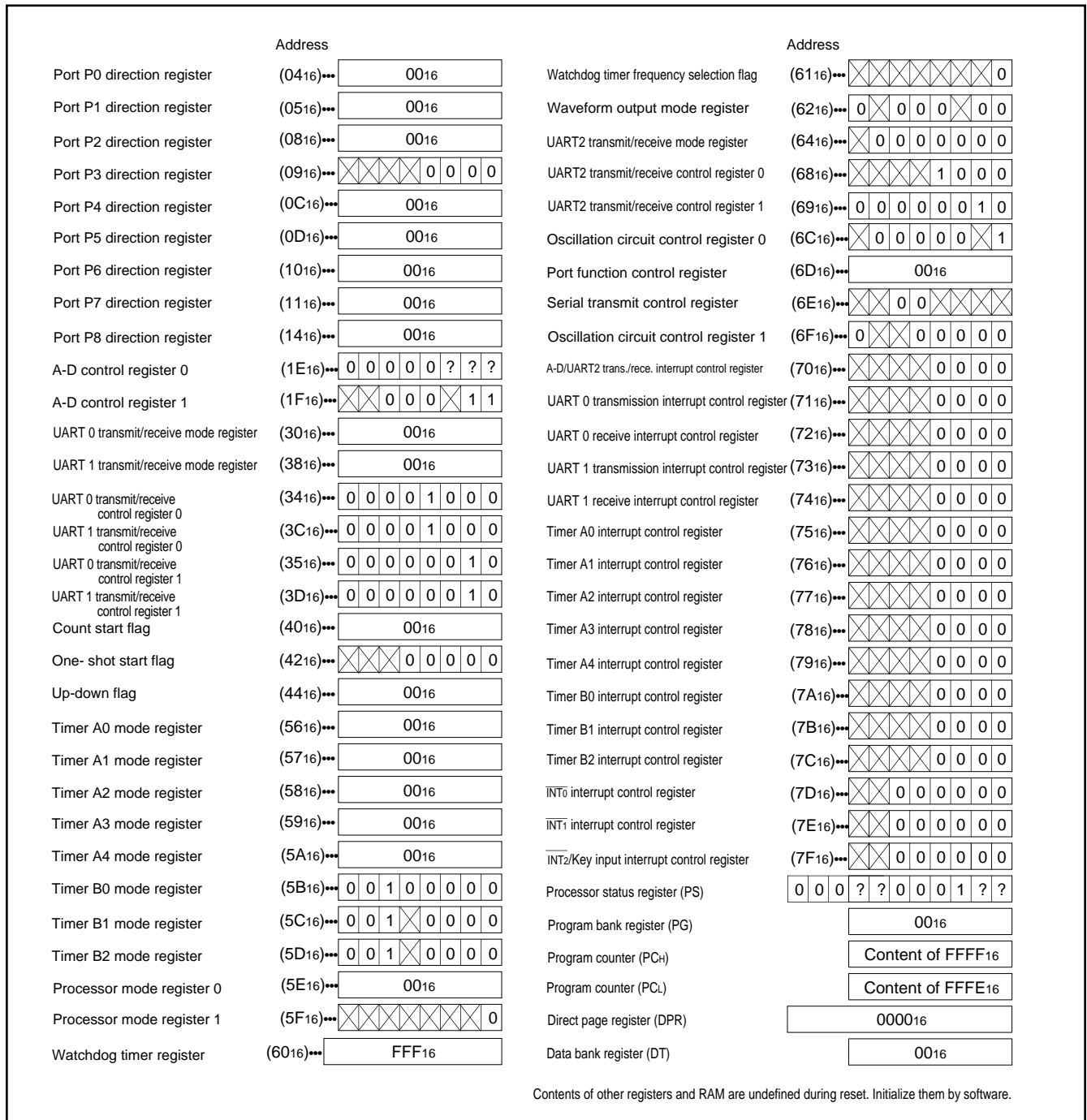


Fig. 12 Microcomputer internal status during reset

New product

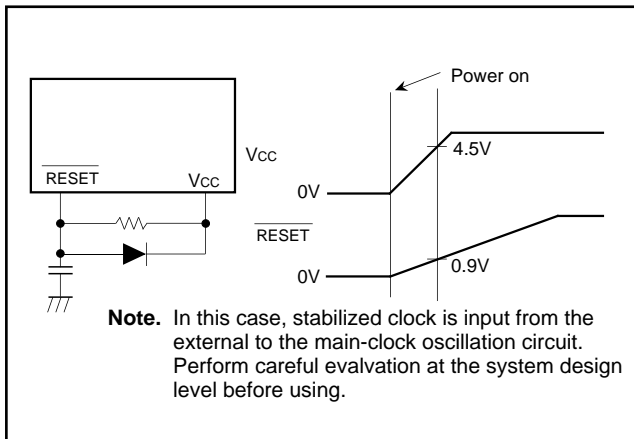


Fig. 13 Example of a reset circuit

ADDRESSING MODES

The M37733S4BFP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE - CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37733S4BFP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE - CHIP 16-BIT MICROCOMPUTERS for details.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Power source voltage		-0.3 to +7	V
AV _{cc}	Analog power source voltage		-0.3 to +7	V
V _i	Input voltage RESET, CNV _{ss} , BYTE		-0.3 to +12	V
V _i	Input voltage P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7, P43 - P47, P50 - P57, P60 - P67, P70 - P77, P80 - P87, V _{REF} , X _{IN} , HOLD, RDY		-0.3 to V _{cc} + 0.3	V
V _o	Output voltage P00/A0 - P07/A7, P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7, P30/R/W, P31/BHE, P32/ALE, P33/HLDA, P42/ φ 1, P43 - P47, P50 - P57, P60 - P67, P70 - P77, P80 - P87, X _{OUT} , E		-0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	300	mW
T _{opr}	Operating temperature		-20 to +85	°C
T _{stg}	Storage temperature		-40 to +150	°C

RECOMMENDED OPERATING CONDITIONS (V_{cc} = 5 V ± 10 %, T_a = -20 to +85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{cc}	Power source voltage	f(X _{IN}) : Operating 4.5	5.0	5.5	V
		f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz 2.7		5.5	
AV _{cc}	Analog power source voltage		V _{cc}		V
V _{ss}	Power source voltage		0		V
AV _{ss}	Analog power source voltage		0		V
V _{IH}	High-level input voltage HOLD, RDY, P43 - P47, P50 - P57, P60 - P67, P70 - P77, P80 - P87, X _{IN} , RESET, CNV _{ss} , BYTE, X _{CIN} (Note 3)	0.8 V _{cc}		V _{cc}	V
V _{IH}	High-level input voltage P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7	0.5 V _{cc}		V _{cc}	V
V _{IL}	Low-level input voltage HOLD, RDY, P43 - P47, P50 - P57, P60 - P67, P70 - P77, P80 - P87, X _{IN} , RESET, CNV _{ss} , BYTE, X _{CIN} (Note 3)	0		0.2V _{cc}	V
V _{IL}	Low-level input voltage P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7	0		0.16V _{cc}	V
I _{OH(peak)}	High-level peak output current P00/A0 - P07/A7, P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7, P30/R/W, P31/BHE, P32/ALE, P33/HLDA, P42/ φ 1, P43 - P47, P50 - P57, P60 - P67, P70 - P77, P80 - P87			-10	mA
I _{OH(avg)}	High-level average output current P00/A0 - P07/A7, P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7, P30/R/W, P31/BHE, P32/ALE, P33/HLDA, P42/ φ 1, P43 - P47, P50 - P57, P60 - P67, P70 - P77, P80 - P87			-5	mA
I _{OL(peak)}	Low-level peak output current P00/A0 - P07/A7, P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7, P30/R/W, P31/BHE, P32/ALE, P33/HLDA, P42/ φ 1, P43, P54 - P57, P60 - P67, P70 - P77, P80 - P87			10	mA
I _{OL(peak)}	Low-level peak output current P44 - P47, P50 - P53			20	mA
I _{OL(avg)}	Low-level average output current P00/A0 - P07/A7, P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7, P30/R/W, P31/BHE, P32/ALE, P33/HLDA, P42/ φ 1, P43, P54 - P57, P60 - P67, P70 - P77, P80 - P87			5	mA
I _{OL(avg)}	Low-level average output current P44 - P47, P50 - P53			15	mA
f(X _{IN})	Main-clock oscillation frequency (Note 4)			25	MHz
f(X _{CIN})	Sub-clock oscillation frequency		32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

2. The sum of I_{OL(peak)} for ports P00/A0 - P07/A7, P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7, P30/R/W, P31/BHE, P32/ALE, P33/HLDA and P8 must be 80 mA or less, the sum of I_{OH(peak)} for ports P00/A0 - P07/A7, P10/A8/D8 - P17/A15/D15, P20/A16/D0 - P27/A23/D7, P30/R/W, P31/BHE, P32/ALE, P33/HLDA and P8 must be 80 mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, and P7 must be 80 mA or less.

3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".

4. The maximum value of f(X_{IN}) = 12.5 MHz when the main clock division selection bit = "1".

New product

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage P00/A0 – P07/A7, P10/A8/D8 – P17/A15/D15, P20/A16/D0 – P27/A23/D7, P33/HLD \bar{A} , P42/ ϕ 1, P43 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87	$I_{OH} = -10\text{ mA}$	3			V
V_{OH}	High-level output voltage P00/A0 – P07/A7, P10/A8/D8 – P17/A15/D15, P20/A16/D0 – P27/A23/D7, P33/HLD \bar{A} , P42/ ϕ 1	$I_{OH} = -400\text{ }\mu\text{ A}$	4.7			V
V_{OH}	High-level output voltage P30/R/ \bar{W} , P31/ \bar{BHE} , P32/ALE	$I_{OH} = -10\text{ mA}$ $I_{OH} = -400\text{ }\mu\text{ A}$	3.1 4.8			V
V_{OH}	High-level output voltage \bar{E}	$I_{OH} = -10\text{ mA}$ $I_{OH} = -400\text{ }\mu\text{ A}$	3.4 4.8			V
V_{OL}	Low-level output voltage P00/A0 – P07/A7, P10/A8/D8 – P17/A15/D15, P20/A16/D0 – P27/A23/D7, P33/HLD \bar{A} , P42/ ϕ 1, P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87	$I_{OL} = 10\text{ mA}$			2	V
V_{OL}	Low-level output voltage P44 – P47, P50 – P53	$I_{OL} = 20\text{ mA}$			2	V
V_{OL}	Low-level output voltage P00/A0 – P07/A7, P10/A8/D8 – P17/A15/D15, P20/A16/D0 – P27/A23/D7, P33/HLD \bar{A} , P42/ ϕ 1	$I_{OL} = 2\text{ mA}$			0.45	V
V_{OL}	Low-level output voltage P30/R/ \bar{W} , P31/ \bar{BHE} , P32/ALE	$I_{OL} = 10\text{ mA}$ $I_{OL} = 2\text{ mA}$			1.9 0.43	V V
V_{OL}	Low-level output voltage \bar{E}	$I_{OL} = 10\text{ mA}$ $I_{OL} = 2\text{ mA}$			1.6 0.4	V V
$V_{T+} - V_{T-}$	Hysteresis \bar{HOLD} , \bar{RDY} , $TA0_{IN} - TA4_{IN}$, $TB0_{IN} - TB2_{IN}$, $INT_0 - INT_2$, AD_{TRG} , CTS_0 , CTS_1 , CTS_2 , CLK_0 , CLK_1 , CLK_2 , $KI_0 - KI_3$		0.4		1	V
$V_{T+} - V_{T-}$	Hysteresis \bar{RESET}		0.2		0.5	V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}	$V_{CC} = 5\text{ V}$	0.1		0.4	V
$V_{T+} - V_{T-}$	Hysteresis X_{CIN} (When external clock is input)		0.1		0.4	V
I_{IH}	High-level input current P10/A8/D8 – P17/A15/D15, P20/A16/D0 – P27/A23/D7, P43 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X_{IN} , \bar{RESET} , CNV_{SS} , $BYTE$	$V_I = 5\text{ V}$			5	$\mu\text{ A}$
I_{IL}	Low-level input current P10/A8/D8 – P17/A15/D15, P20/A16/D0 – P27/A23/D7, P43 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, X_{IN} , \bar{RESET} , CNV_{SS} , $BYTE$	$V_I = 0\text{ V}$			-5	$\mu\text{ A}$
I_{IL}	Low-level input current P54 – P57, P62 – P64	$V_I = 0\text{ V}$, without a pull-up transistor			-5	$\mu\text{ A}$
		$V_I = 0\text{ V}$, with a pull-up transistor	-0.25	-0.5	-1.0	mA
V_{RAM}	RAM hold voltage	When clock is stopped	2			V

New product

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+85\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
I _{CC}	Power source current	When external bus is in use, output pins are open, and other pins are V _{SS} .	V _{CC} = 5 V, f(X _{IN}) = 25 MHz (square waveform), (f _{f2}) = 12.5 MHz, f(X _{CIN}) = 32.768 kHz, in operating (Note 1)		11.4	22.8	mA
			V _{CC} = 5 V, f(X _{IN}) = 25 MHz (square waveform), (f _{f2}) = 1.5625 MHz, f(X _{CIN}) = Stopped, in operating (Note 1)		1.6	3.2	mA
			V _{CC} = 5 V, f(X _{IN}) = 25 MHz (square waveform), f(X _{CIN}) = 32.768 kHz, when a WIT instruction is executed (Note 2)		10	20	μA
			V _{CC} = 5 V, f(X _{IN}) = Stopped, f(X _{CIN}) = 32.768 kHz, in operating (Note 3)		60	120	μA
			V _{CC} = 5 V, f(X _{IN}) = Stopped, f(X _{CIN}) = 32.768 kHz, when a WIT instruction is executed (Note 4)		5	10	μA
			T _a = 25 °C, when clock is stopped			1	μA
			T _a = 85 °C, when clock is stopped				20

- Notes**
1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
 2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
 3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
 4. This applies when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+85\text{ }^\circ\text{C}$, f(X_{IN}) = 25 MHz, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V _{REF} = V _{CC}			10	Bits
—	Absolute accuracy	V _{REF} = V _{CC}			± 3	LSB
RLADDER	Ladder resistance	V _{REF} = V _{CC}	10		25	kΩ
t _{CONV}	Conversion time		9.44			μs
V _{REF}	Reference voltage		2		V _{CC}	V
V _{IA}	Analog input voltage		0		V _{REF}	V

Note. This applies when the main clock division selection bit = "0" and f_{f2} = 12.5 MHz.

New product

TIMING REQUIREMENTS ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted (Note 1))

Notes 1. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 1)	40		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 2)	15		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 2)	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns

Notes 1. When the main clock division selection bit = "1", the minimum value of $t_c = 80\text{ ns}$.

2. When the main clock division selection bit = "1", values of $t_{w(H)} / t_c$ and $t_{w(L)} / t_c$ must be set to values from 0.45 through 0.55.

Microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P4D-E)}$	Port P4 input setup time	60		ns
$t_{su(P5D-E)}$	Port P5 input setup time	60		ns
$t_{su(P6D-E)}$	Port P6 input setup time	60		ns
$t_{su(P7D-E)}$	Port P7 input setup time	60		ns
$t_{su(P8D-E)}$	Port P8 input setup time	60		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		ns
$t_{su(D-E)}$	Data input setup time	32		ns
$t_{su(RDY-\phi 1)}$	RDY input setup time	55		ns
$t_{su(HOLD-\phi 1)}$	HOLD input setup time	55		ns
$t_{h(E-D)}$	Data input hold time	0		ns
$t_{h(\phi 1-RDY)}$	RDY input hold time	0		ns
$t_{h(\phi 1-HOLD)}$	HOLD input hold time	0		ns

New product

Timer A input (Count input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time	80		ns
t _w (TAH)	TAiIN input high-level pulse width	40		ns
t _w (TAL)	TAiIN input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time (Note)	320		ns
t _w (TAH)	TAiIN input high-level pulse width (Note)	160		ns
t _w (TAL)	TAiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS."

Timer A input (External trigger input in one-shot pulse mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time (Note)	320		ns
t _w (TAH)	TAiIN input high-level pulse width	80		ns
t _w (TAL)	TAiIN input low-level pulse width	80		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS."

Timer A input (External trigger input in pulse width modulation mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _w (TAH)	TAiIN input high-level pulse width	80		ns
t _w (TAL)	TAiIN input low-level pulse width	80		ns

Timer A input (Up-down input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (UP)	TAiOUT input cycle time	2000		ns
t _w (UPH)	TAiOUT input high-level pulse width	1000		ns
t _w (UPL)	TAiOUT input low-level pulse width	1000		ns
t _{su} (UP-T _{IN})	TAiOUT input setup time	400		ns
t _h (T _{IN} -UP)	TAiOUT input hold time	400		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAjIN input cycle time	800		ns
t _{su} (TAjIN-TAjOUT)	TAjIN input setup time	200		ns
t _{su} (TAjOUT-TAjIN)	TAjOUT input setup time	200		ns

New product

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (one edge count)	80		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (one edge count)	40		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (one edge count)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (both edges count)	160		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (both edges count)	80		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (both edges count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (Note)	320		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (Note)	160		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS."

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (Note)	320		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (Note)	160		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS."

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	ADTRG input cycle time (minimum allowable trigger)	1000		ns
$t_{w(ADL)}$	ADTRG input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high-level pulse width	100		ns
$t_{w(CKL)}$	CLKi input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	30		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

External interrupt \overline{INT}_i input, key input interrupt \overline{KI}_i input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INT}_i input high-level pulse width	250		ns
$t_{w(INL)}$	\overline{INT}_i input low-level pulse width	250		ns
$t_{w(KIL)}$	\overline{KI}_i input low-level pulse width	250		ns

New product

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ expresses the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".

New product

SWITCHING CHARACTERISTICS

(VCC = 5 V ± 10 %, VSS = 0 V, Ta = -20 to +85°C, f(XIN) = 25 MHz, unless otherwise noted (Note))

Microprocessor mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
td(E-P4Q)	Port P4 data output delay time	Fig. 14		80	ns
td(E-P5Q)	Port P5 data output delay time			80	ns
td(E-P6Q)	Port P6 data output delay time			80	ns
td(E-P7Q)	Port P7 data output delay time			80	ns
td(E-P8Q)	Port P8 data output delay time			80	ns

Note. This applies when the main clock division selection bit = "0" and f(f2) = 12.5 MHz.

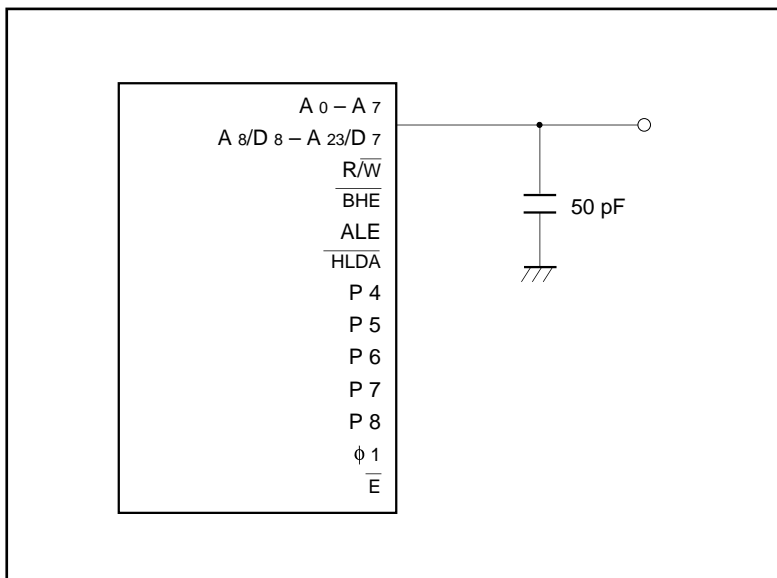


Fig. 14 Measuring circuit for each pin

New product

Microprocessor mode

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = 25 °C, f(X_{IN}) = 25 MHz, unless otherwise noted (Note 1))

Symbol	Parameter	(Note2) Wait mode	Test conditions	Limits		Unit	
				Min.	Max.		
t _d (A _n -E)	Address output delay time	No wait	Fig. 14	12		ns	
		Wait 1					
		Wait 0		87		ns	
t _d (A-E)	Address output delay time	No wait		12		ns	
		Wait 1					
		Wait 0		75		ns	
t _h (E-An)	Address hold time				18		ns
t _w (ALE)	ALE pulse width	No wait		22		ns	
		Wait 1					
		Wait 0		57		ns	
t _{su} (A-ALE)	Address output setup time	No wait		5		ns	
		Wait 1					
		Wait 0		45		ns	
t _h (ALE-A)	Address hold time	No wait		9		ns	
		Wait 1					
		Wait 0		15		ns	
t _d (ALE-E)	ALE output delay time	No wait		4		ns	
		Wait 1					
		Wait 0	10		ns		
t _d (E-DQ)	Data output delay time				45	ns	
t _h (E-DQ)	Data hold time			18		ns	
t _w (EL)	E pulse width	No wait	50		ns		
		Wait 1					
		Wait 0	130		ns		
t _{pxz} (E-DZ)	Floating start delay time				5	ns	
t _{pzx} (E-DZ)	Floating release delay time			20		ns	
t _d (BHE-E)	BHE output delay time	No wait	12		ns		
		Wait 1					
		Wait 0	87		ns		
t _d (R/W-E)	R/W output delay time	No wait	12		ns		
		Wait 1					
		Wait 0	87		ns		
t _h (E-BHE)	BHE hold time			18		ns	
t _h (E-R/W)	R/W hold time			18		ns	
t _d (E- φ ₁)	φ ₁ output delay time			0	18	ns	
t _d (φ ₁ -HLDA)	HLDA output delay time				50	ns	

Notes 1. This applies when the main clock division selection bit = "0" and f(f₂) = 12.5 MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

New product

Bus timing data formulas

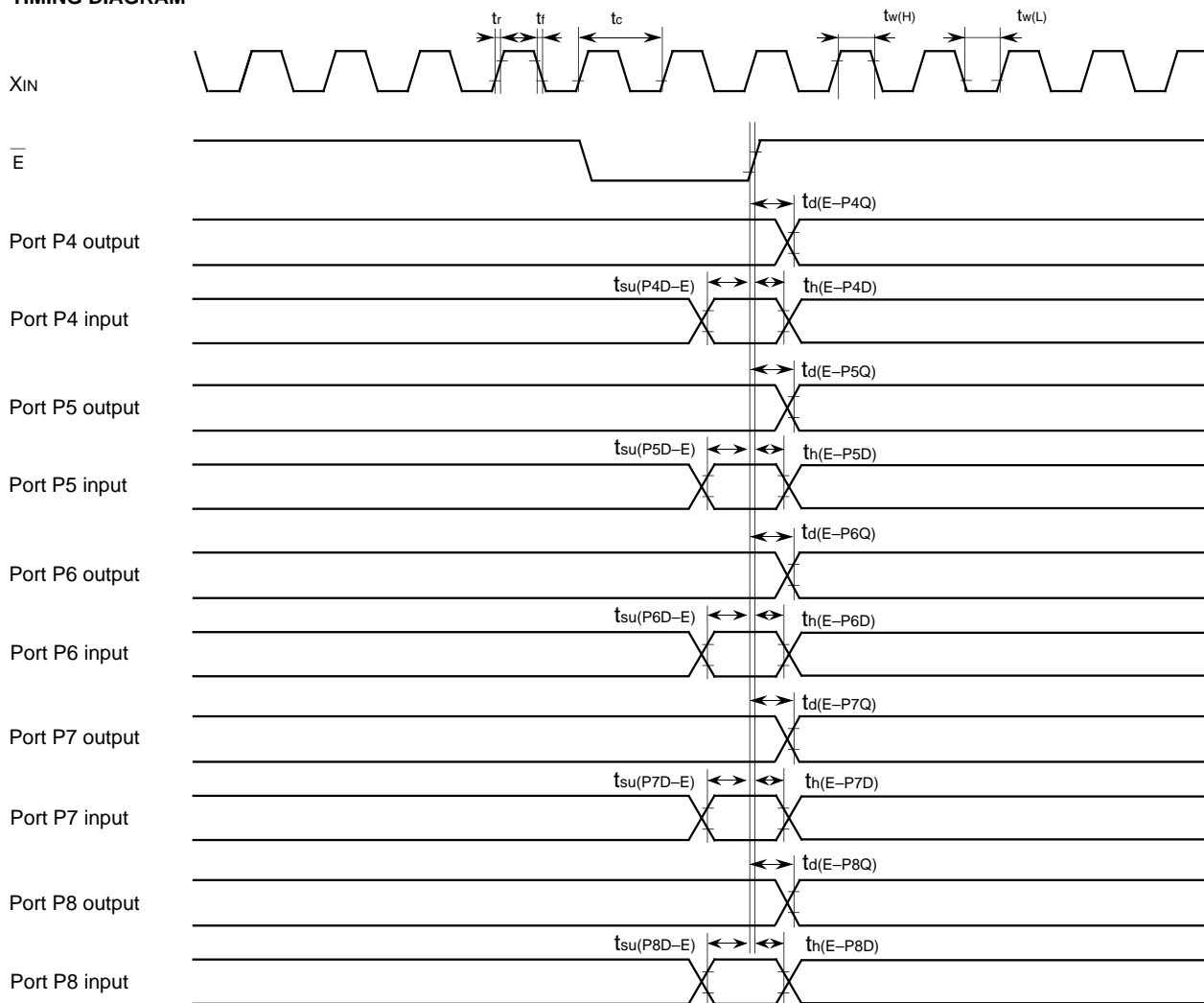
(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, T_a = -20 to +85 °C, f(X_{IN}) = 25 MHz (Max.), unless otherwise noted (Note 1))

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
t _d (A _n -E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 28	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 33	
t _d (A-E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 28	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 45	
t _h (E-A _n)	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 22	ns
t _w (ALE)	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 18	ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 23	
t _{su} (A-ALE)	Address output setup time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 35	ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 35	
t _h (ALE-A)	Address hold time	No wait	9		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 25	
t _d (ALE-E)	ALE output delay time	No wait	4		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 30	
t _d (E-DQ)	Data output delay time			45	ns
t _h (E-DQ)	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 22	ns
t _w (EL)	\overline{E} pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)}$	- 30	ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$	- 30	
t _{pxz} (E-DZ)	Floating start delay time			5	ns
t _{pxz} (E-DZ)	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 22	ns
t _d (BHE-E)	BHE output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 28	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 33	
t _d (R/W-E)	R/ \overline{W} output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 28	ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)}$	- 33	
t _h (E-BHE)	\overline{BHE} hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 22	ns
t _h (E-R/W)	R/ \overline{W} hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)}$	- 22	ns
t _d (E- φ ₁)	φ ₁ output delay time		0	18	ns

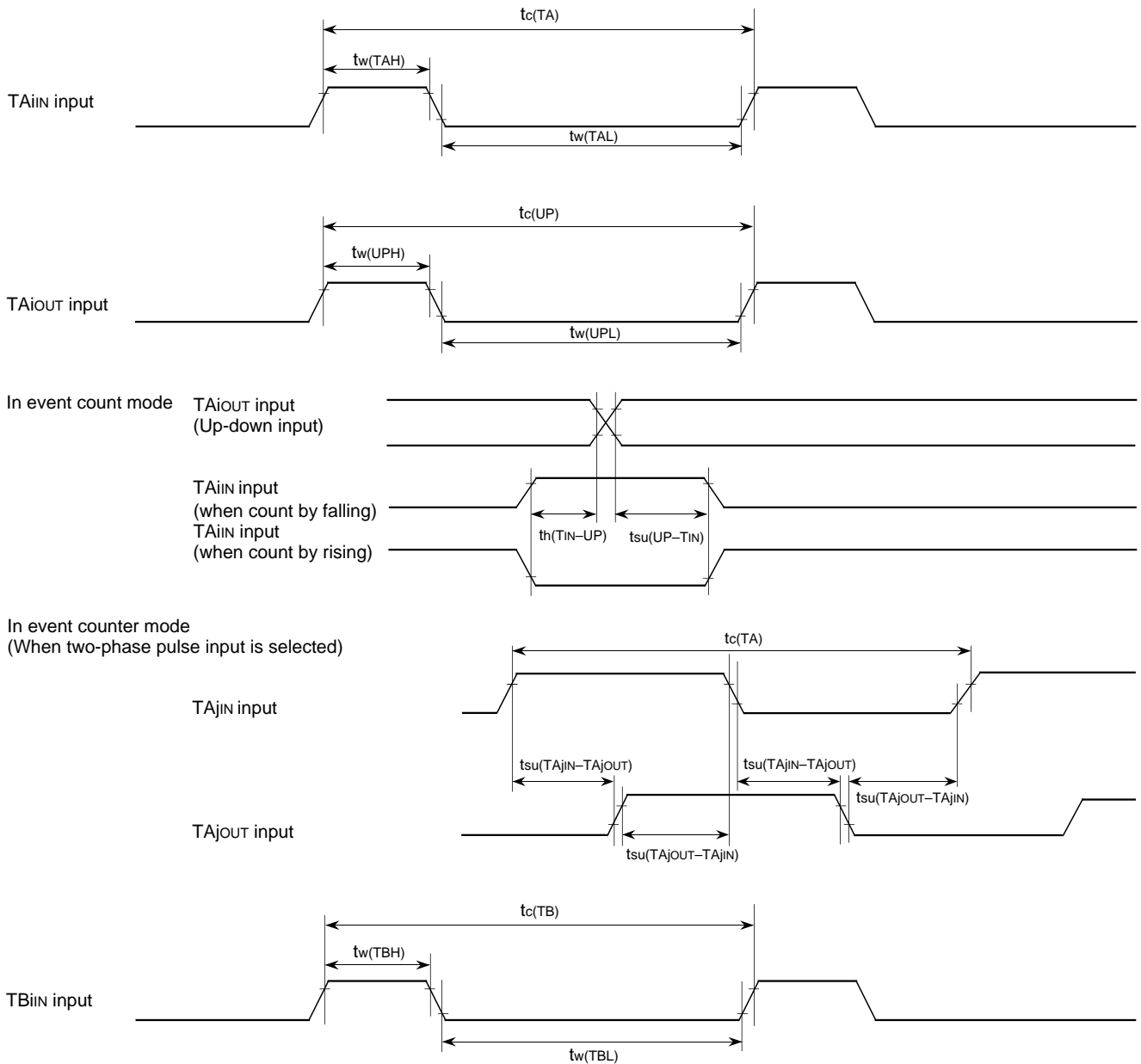
- Notes**
1. This applies when the main-clock division selection bit = "0".
 2. f(f₂) expresses the clock f₂ frequency.
For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXXFP".

New product

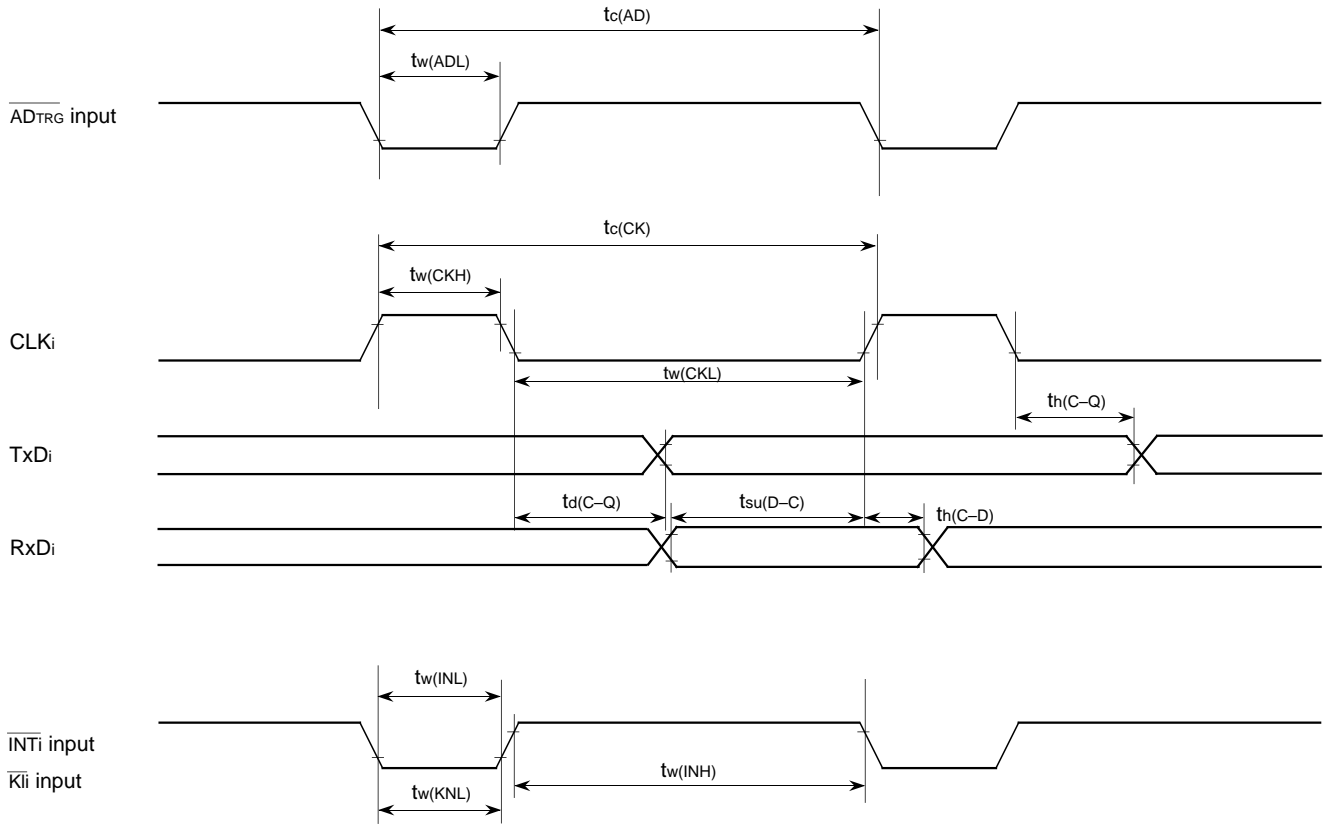
TIMING DIAGRAM



New product

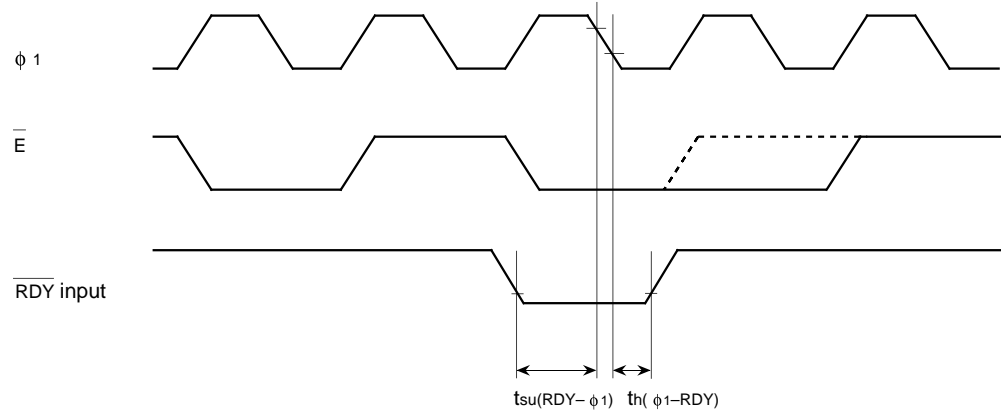


New product

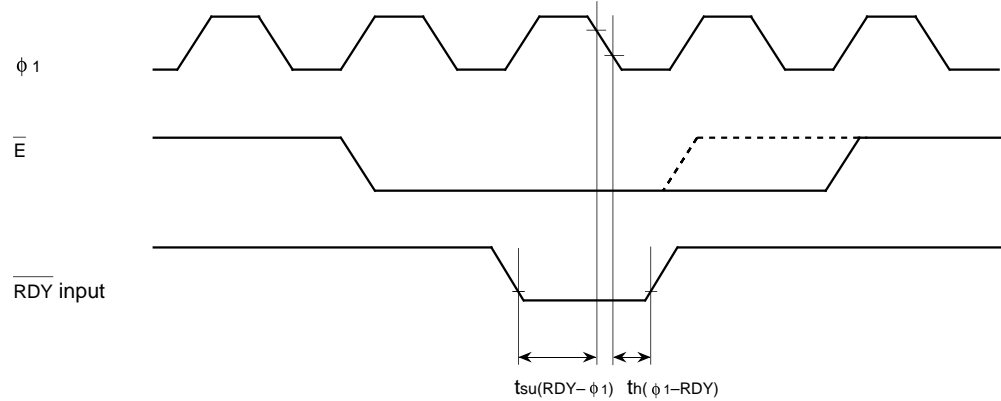


New product

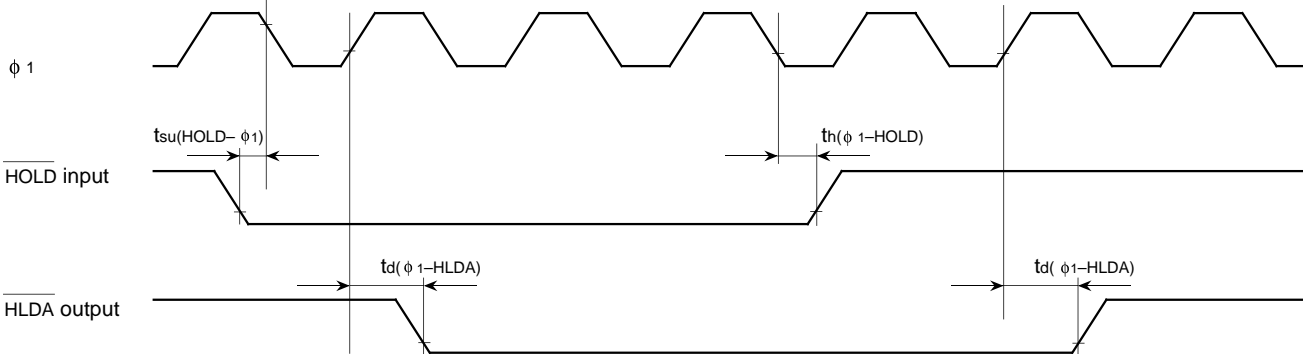
Microprocessor mode
(When wait bit = "1")



(When wait bit = "0")



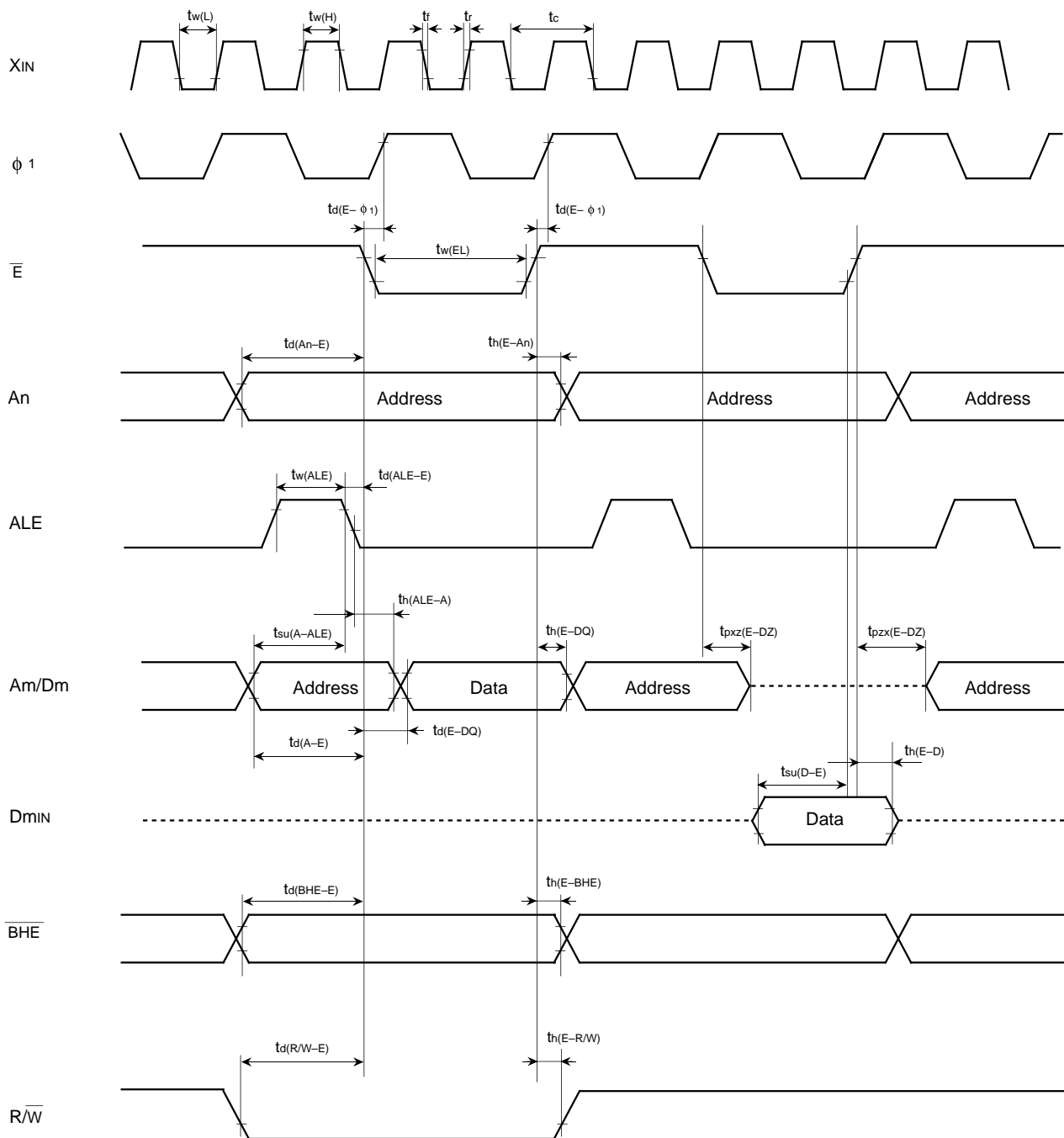
(When wait bit = "1" or "0" in common)



- Test conditions
- $V_{CC} = 5\text{ V} \pm 10\%$
 - Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$
 - Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$

New product

Microprocessor mode
(No wait : When wait bit = "1")



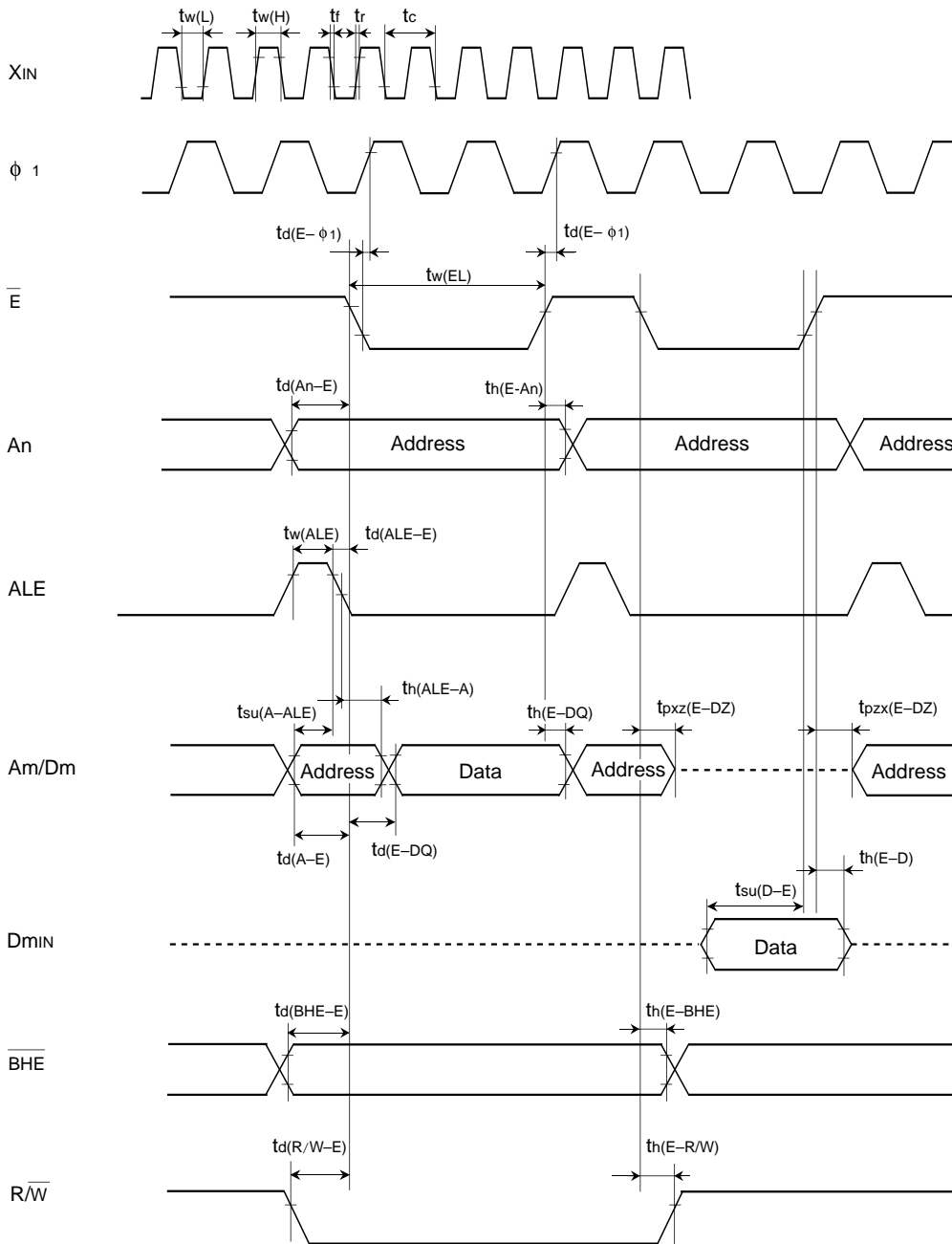
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{MIN} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

New product

Microprocessor mode

(Wait 1 : The external memory area is accessed when wait bit = "0" and wait selection bit = "1".)



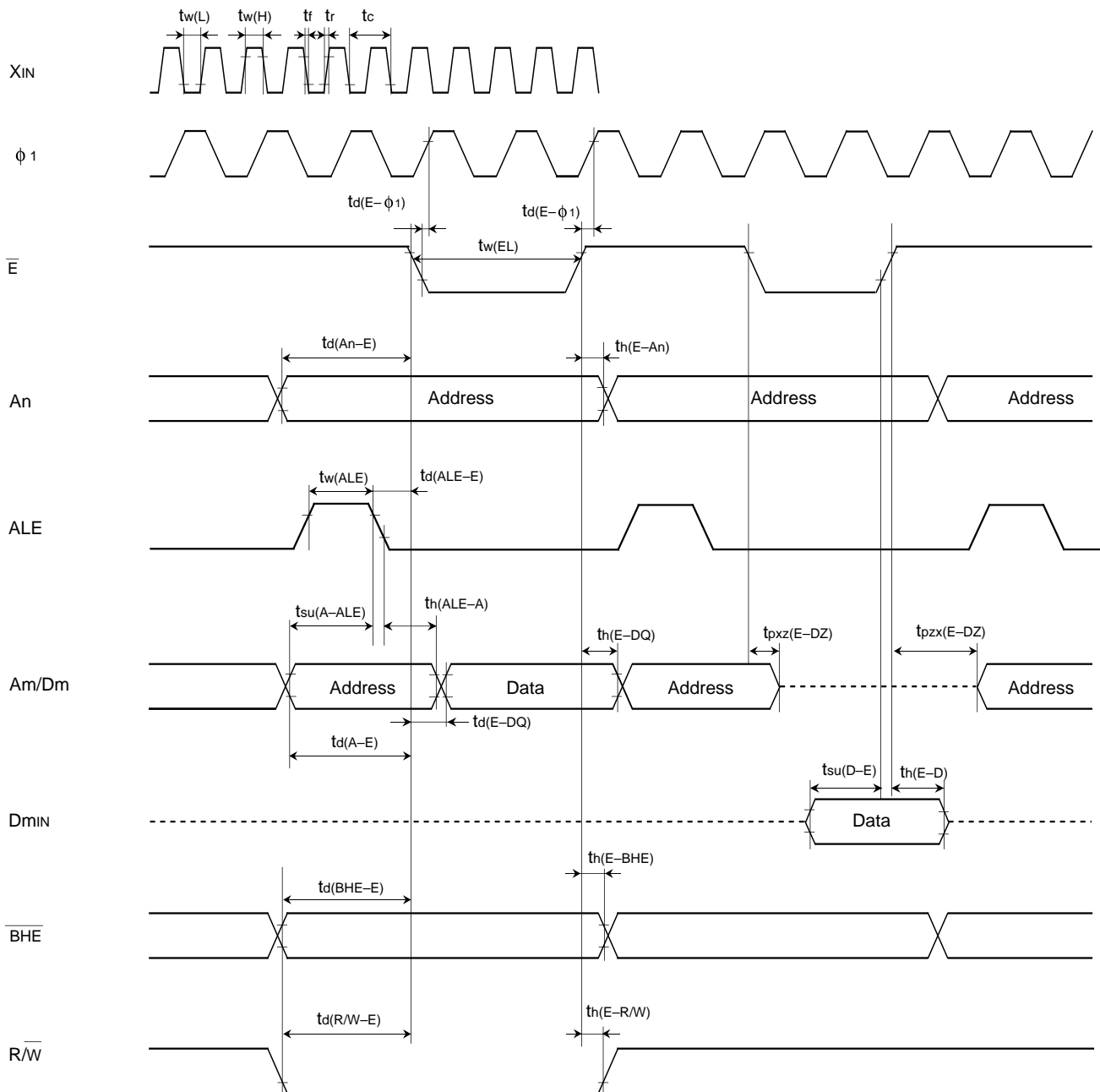
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

New product

Microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

New product

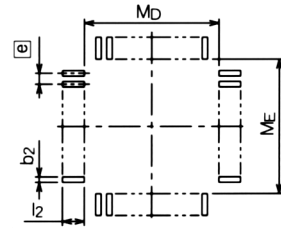
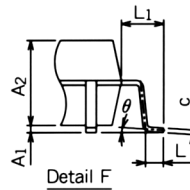
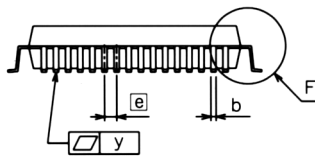
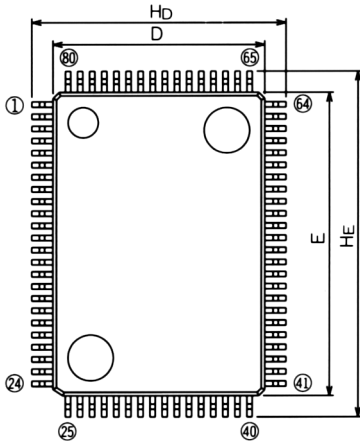
PACKAGE OUTLINE

80P6N-A

Plastic 80pin 14x20mm body QFP

EIAJ Package Code	JEDEC Code	Weight (g)	Lead Material
QFP80-P-1420-0.80	-	1.58	Alloy 42

Scale : 2/1



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	-	0.8	-
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	-	1.4	-
y	-	-	0.1
theta	0°	-	10°
b2	-	0.5	-
l2	1.3	-	-
MD	-	14.6	-
ME	-	20.6	-

New product

MEMO

New product

MEMO

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