Ordering number : EN5814

CMOS IC

LC72134M

Dual PLL Frequency Synthesizer for FM Tuner Systems

Overview

The LC72134M is a dual PLL frequency synthesizer product that integrates on a single chip both an AM/FM audio broadcast reception PLL circuit (main PLL) and a dedicated FM multiplex reception PLL circuit (sub PLL). Since the main PLL circuit is equivalent to the LC72135M, software developed for that product can be used with this chip. The sub-PLL circuit can be controlled independently.

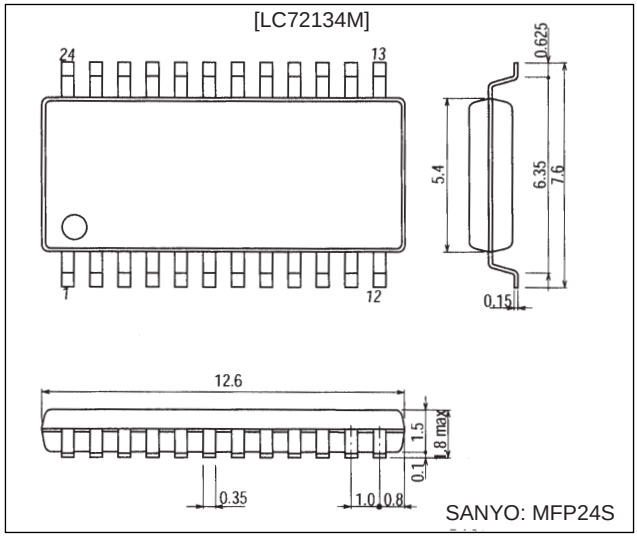
Functions

- High-speed programmable divider
  - FMINa (main): 10 to 160 MHz ... Pulse swallower technique (With built-in divide-by-2 prescaler)
  - FMINb (sub): 10 to 160 MHz ... Pulse swallower technique (With built-in divide-by-2 prescaler)
  - AMIN (main): 0.5 to 40 MHz ... Pulse swallower and direct division techniques
- IF counter
  - Two input pins provided: IFIN1 and IFIN2
  - IFIN1: 0.4 to 25 MHz ... For AM and FM IF counting
  - IFIN2: 0.4 to 25 MHz ... For AM and FM IF counting
- Reference frequency
  - One of 12 reference frequencies can be selected (using a 4.5 or 7.2 MHz crystal element)
    1, 3, 5, 9, 10, 3.125, 6.25, 12.5*, 15*, 25*, 50*, or 100 kHz
    *: Sub PLL reference frequencies
- Phase comparator
  - Supports dead zone control.
  - Built-in unlocked state detection circuit
  - Built-in deadlock clear circuit
- An MOS transistor for an active low-pass filter is built in.
- I/O ports
  - Output-only ports: 4 pins
  - I/O ports: 1 pin
  - Input-only ports: 1 pin (function shared with the IFIN2 pin)
  - Supports the output of an 8-Hz clock time base signal.
- CCB interface used for data I/O.
  - The main PLL is compatible with the LC72135M.
  - The sub PLL can be controlled at an independent address.
- Operating ranges
  - Supply voltage: 4.5 to 5.5 V
  - Operating temperature: –40 to 85°C
- Package: MFP24S

Package Dimensions

unit: mm

3112-MFP24S



This product supports the Sanyo-original CCB bus format.

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

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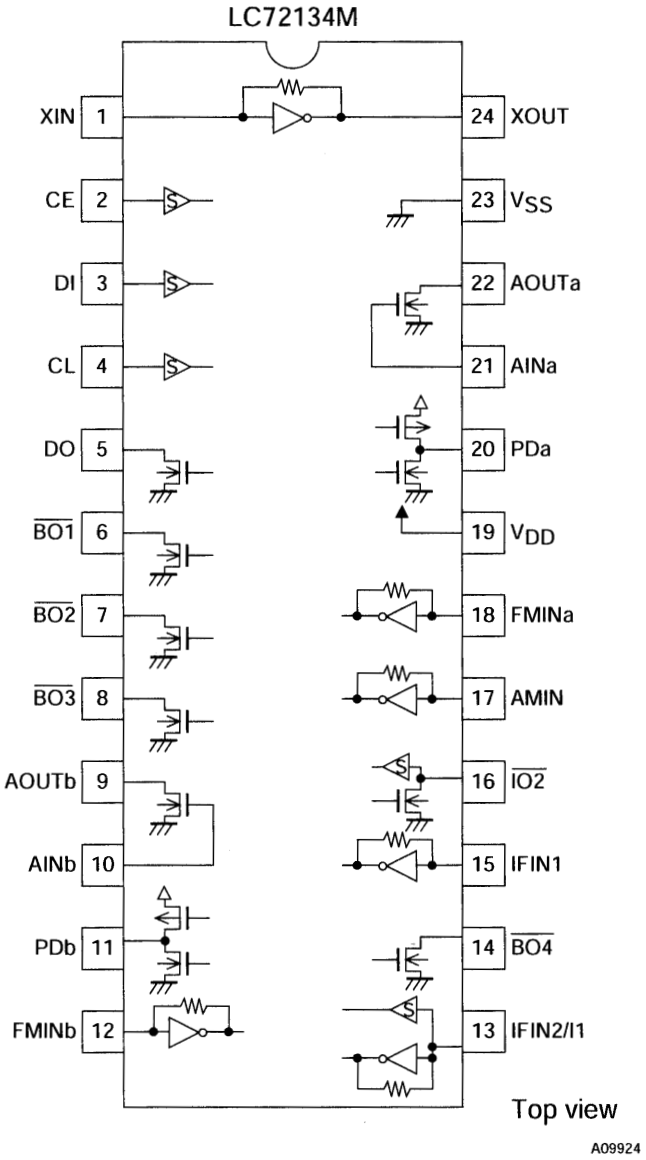
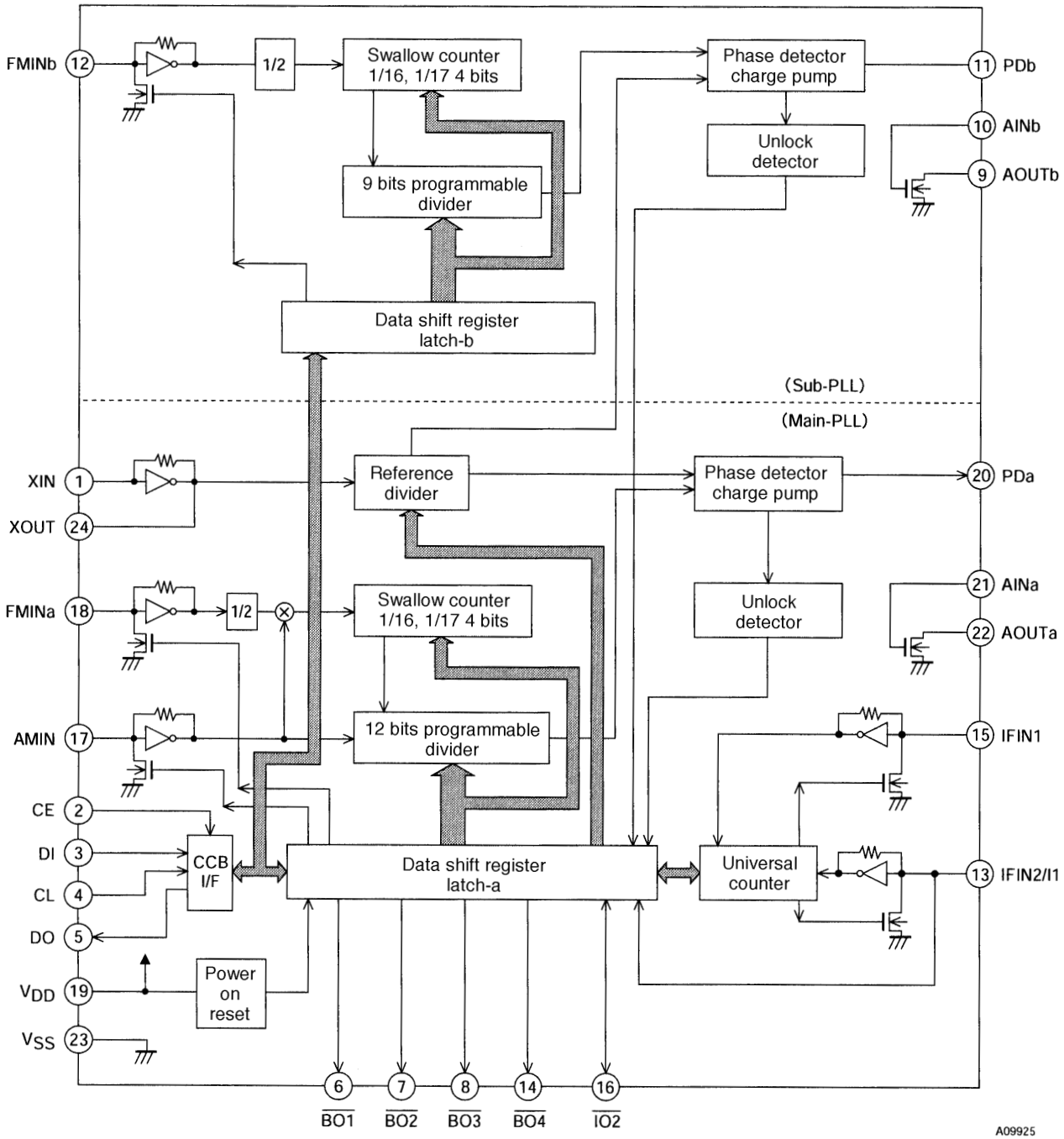
Pin Assignments



Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
Maximum input voltage	V_{IN}1 max	CE, DI, CL, AINa, AINb	–0.3 to +7.0	V
	V_{IN}2 max	XIN, FMINa, FMINb, AMIN, IFIN1, IFIN2/I1	–0.3 to V_{DD} +0.3	V
	V_{IN}3 max	$\overline{IO2}$	–0.3 to +15	V
Maximum output voltage	V_O1 max	DO	–0.3 to +7.0	V
	V_O2 max	XOUT, PDa, PDb	–0.3 to V_{DD} +0.3	V
	V_O3 max	$\overline{BO1}$ to $\overline{BO4}$, $\overline{IO2}$, AOUTa, AOUTb	–0.3 to +15	V
Maximum output current	I_O1 max	$\overline{BO1}$	0 to +3.0	mA
	I_O2 max	DO, AOUTa, AOUTb	0 to +6.0	mA
	I_O3 max	$\overline{BO2}$ to $\overline{BO4}$, $\overline{IO2}$	0 to +10.0	mA
Allowable power dissipation	Pd max	Ta ≤ 85°C	200	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to 85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		5.5	V
Input high-level voltage	V_{IH}1	CE, DI, CL	0.7 V_{DD}		6.5	V
	V_{IH}2	IFIN2/I1	0.7 V_{DD}		V_{DD}	V
	V_{IH}3	$\overline{IO2}$	0.7 V_{DD}		13	V
Input low-level voltage	V_{IL}	CE, DI, CL, $\overline{IO2}$, IFIN2/I1	0		0.3 V_{DD}	V
Output voltage	V_O1	DO	0		6.5	V
	V_O2	$\overline{BO1}$ to $\overline{BO4}$, $\overline{IO2}$, AOUTa, AOUTb	0		13	V
Input frequency	f_{IN}1	XIN: V_{IN}1	1		8	MHz
	f_{IN}2	FMINa, FMINb: V_{IN}2	10		160	MHz
	f_{IN}3	AMIN: V_{IN}3, SNS = 1	2		40	MHz
	f_{IN}4	AMIN: V_{IN}4, SNS = 0	0.5		10	MHz
	f_{IN}5	IFIN1, IFIN2/I1: V_{IN}5	0.4		25	MHz
Input amplitude	V_{IN}1	XIN: f_{IN}1	400		1500	mVrms
	V_{IN}2-1	FMINa, FMINb: f = 10 to 130 MHz	40		1500	mVrms
	V_{IN}2-2	FMINa, FMINb: f = 130 to 160 MHz	70		1500	mVrms
	V_{IN}3	AMIN: f_{IN}3, SNS = 1	40		1500	mVrms
	V_{IN}4	AMIN: f_{IN}4, SNS = 0	40		1500	mVrms
	V_{IN}5	IFIN1, IFIN2/I1: f = 0.4 to 25 MHz, IFS = 1	70		1500	mVrms
	V_{IN}6	IFIN1, IFIN2/I1: f = 0.4 to 12 MHz, IFS = 0	100		1500	mVrms
Guaranteed crystal oscillator frequency	Xtal	XIN, XOUT: *1	4.0		8.0	MHz

Note: Recommended value for CI for the crystal oscillator element: CI ≤ 120 Ω (4.5 MHz) or CI ≤ 70 Ω (7.2 MHz)
However, since the oscillator circuit characteristics depend on the printed circuit board, circuit constants, and other factors, consult with the manufacturer of the crystal element.

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Internal feedback resistance	Rf1	XIN		1.0		MΩ
	Rf2	FMINa, FMINb		500		kΩ
	Rf3	AMIN		500		kΩ
	Rf4	IFIN1, IFIN2/I1		250		kΩ
Internal pull-down resistance	Rpd1	FMINa, FMINb		200		kΩ
	Rpd2	AMIN		200		kΩ
Hysteresis	V_{HIS}	CE, DI, CL, $\overline{IO2}$, IFIN2/II		0.1 V_{DD}		V
Output high-level voltage	V_{OH}1	PDa, PDb: I_O = –1 mA	V_{DD} – 1.0			V

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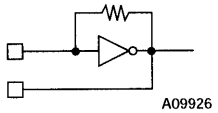
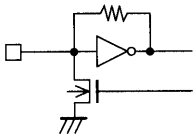
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output low-level voltage	$V_{OL}1$	PDa, PDb: I_O = 1 mA			1.0	V
	$V_{OL}2$	$\overline{BO1}$: I_O = 0.5 mA			0.5	V
		$\overline{BO1}$: I_O = 1 mA			1.0	V
	$V_{OL}3$	DO: I_O = 1 mA			0.2	V
		DO: I_O = 5 mA			1.0	V
	$V_{OL}4$	$\overline{BO2}$ to $\overline{BO4}$, $\overline{IO2}$: I_O = 1 mA			0.2	V
		$\overline{BO2}$ to $\overline{BO4}$, $\overline{IO2}$: I_O = 5 mA			1.0	V
		$\overline{BO2}$ to $\overline{BO4}$, $\overline{IO2}$: I_O = 8 mA			1.6	V
	$V_{OL}5$	AOUTa, AOUTb: I_O = 1 mA, AIN = 1.3 V			0.5	V
Input high-level current	$I_{IH}1$	CE, DI, CL: V_I = 6.5 V			5.0	µA
	$I_{IH}2$	IFIN2/I1: $V_I = V_{DD}$, L/I1 = 0			5.0	µA
	$I_{IH}3$	$\overline{IO2}$: V_I = 13 V			5.0	µA
	$I_{IH}4$	XIN: $V_I = V_{DD}$	2.0		11	µA
	$I_{IH}5$	FMINa, FMINb, AMIN: $V_I = V_{DD}$	4.0		22	µA
	$I_{IH}6$	IFIN1, IFIN2/I1: $V_I = V_{DD}$	8.0		44	µA
	$I_{IH}7$	AINa, AINb: V_I = 6.5 V			200	nA
Input low-level current	$I_{IL}1$	CE, DI, CL: V_I = 0 V			5.0	µA
	$I_{IL}2$	IFIN2/I1: V_I = 0 V, L/I1 = 0			5.0	µA
	$I_{IL}3$	$\overline{IO2}$: V_I = 0 V			5.0	µA
	$I_{IL}4$	XIN: V_I = 0 V	2.0		11	µA
	$I_{IL}5$	FMINa, FMINb, AMIN: V_I = 0 V	4.0		22	µA
	$I_{IL}6$	IFIN1, IFIN2/I1: V_I = 0 V	8.0		44	µA
	$I_{IL}7$	AINa, AINb: V_I = 0 V			200	nA
Output off leakage current	$I_{OFF}1$	$\overline{BO1}$ to $\overline{BO4}$, AOUTa, AOUTb, $\overline{IO2}$: V_O = 13 V			5.0	µA
	$I_{OFF}2$	DO: V_O = 6.5 V			5.0	µA
High-level 3-state off leakage current	I_{OFFH}	PDa, PDb: $V_O = V_{DD}$		0.01	200	nA
Low-level 3-state off leakage current	I_{OFFL}	PDa, PDb: V_O = 0 V		0.01	200	nA
Input capacitance	C_{IN}	FMINa, FMINb		6		pF
Current drain	$I_{DD}1$	V_{DD}: Crystal = 7.2 MHz, $f_{IN}2$ = 130 MHz (FMINa operating), $V_{IN}2$ = 40 mV rms		5	10	mA
	$I_{DD}2$	V_{DD}: Crystal = 7.2 MHz, $f_{IN}2$ = 130 MHz (FMINa and FMINb operating), $V_{IN}2$ = 40 mV rms		8	16	mA
	$I_{DD}3$	V_{DD}: PLL block stopped (PLL INHIBIT mode) Crystal oscillator operating (crystal frequency: 7.2 MHz)		0.5		mA
	$I_{DD}4$	V_{DD}: PLL block stopped, crystal oscillator stopped			10	µA

Pin Descriptions

Pin	Pin No.	Type	Function	Equivalent circuit
XIN XOUT	1 24	Xtal	• Crystal oscillator element connections (4.5 or 7.2 MHz)	 A09926
FMINa	18	Main PLL local oscillator signal input	• FMINa is selected when DVS in the serial data is set to 1. • Input frequency: 10 to 160 MHz • The signal is passed through an internal divide-by-two prescaler and then input to the swallow counter. • The divisor can be set to a value in the range 272 to 65535. Since the internal divide-by-two prescaler is used, the actual divisor will be twice the set value.	 A09927

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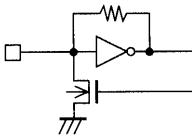
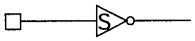
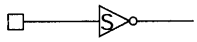
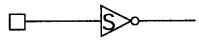
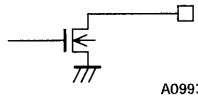
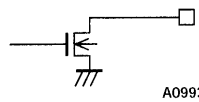
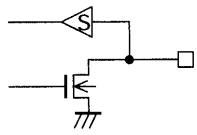
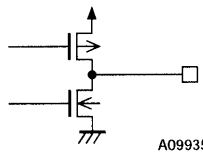
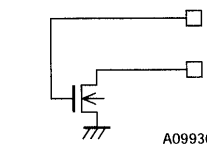
Pin	Pin No.	Type	Function	Equivalent circuit

AMIN	17	Main PLL local oscillator signal input	• AMIN is selected when DVS in the serial data is set to 0.
			• When SNS in the serial data is set to 1:
			  • Input frequency: 2 to 40 MHz
			  • The signal is input to the swallow counter directly.
			  • The divisor can be set to a value in the range 272 to 65535. The set value becomes the actual divisor.
			• When SNS in the serial data is set to 0:
			  • Input frequency: 0.5 to 10 MHz
			  • The signal is input to a 12-bit programmable divider directly.
			  • The divisor can be set to a value in the range 5 to 4095. The set value becomes the actual divisor.
				
				A09928

CE	2	Chip enable	• This pin must be set high to enable serial data input (DI) or serial data output (DO).	 A09929
DI	3	Input data	• Input for serial data transferred from the controller	 A09930
CL	4	Clock	• Clock used for data synchronization for serial data input (DI) and serial data output (DO).	 A09931
DO	5	Output data	• Output for serial data transmitted to the controller. The content of the data transmitted is determined by DOC0 through DOC2.	 A09932
V_{DD}	19	Power supply	• LC72134M power supply (V_{DD} = 4.5 to 5.5 V) • The power on reset circuit operates when power is first applied.	——
V_{SS}	23	Ground	• LC72134M ground	——
$\overline{BO1}$ $\overline{BO2}$ $\overline{BO3}$ $\overline{BO4}$	6 7 8 14	Output ports	• Output-only ports • The output state is determined by BO1 through BO4 in the serial data. When the data value is 0: The output state will be the open circuit state. When the data value is 1: The output state will be a low level. • A time base signal (8 Hz) is output from $\overline{BO1}$ when TBC in the serial data is set to 1.	 A09933
$\overline{IO2}$	16	I/O port	• Shared function I/O port • The pin function is determined by IOC2 in the serial data. When the data value = 0: Input port When the data value = 1: Output port • When specified to function as an input port: The input pin state is reported to the controller through the DO pin. When the input state is low: The data will be 0: When the input state is high: The data will be 1: • When specified to function as an output port: The output state is determined by IO2 in the serial data. When the data value is 0: The output state will be the open circuit state. When the data value is 1: The output state will be a low level. • This pin is set to input mode after a power on reset.	 A09934
PDa	20	Main PLL charge pump output	• PLL charge pump output A high level is output when the frequency of the local oscillator signal divided by N is higher than the reference frequency, and a low level is output when that frequency is lower. This pin goes to the high-impedance state when the frequencies match.	 A09935
AINa AOUTa	21 22	Main PLL low-pass filter amplifier transistor	• Connections for the n-channel MOS transistor to be used for the PLL active low-pass filter.	 A09936

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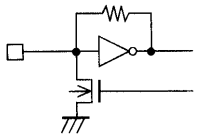
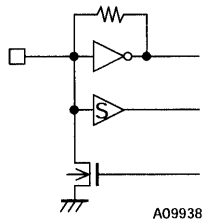
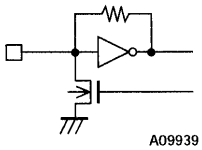
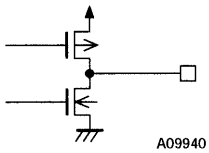
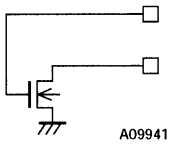
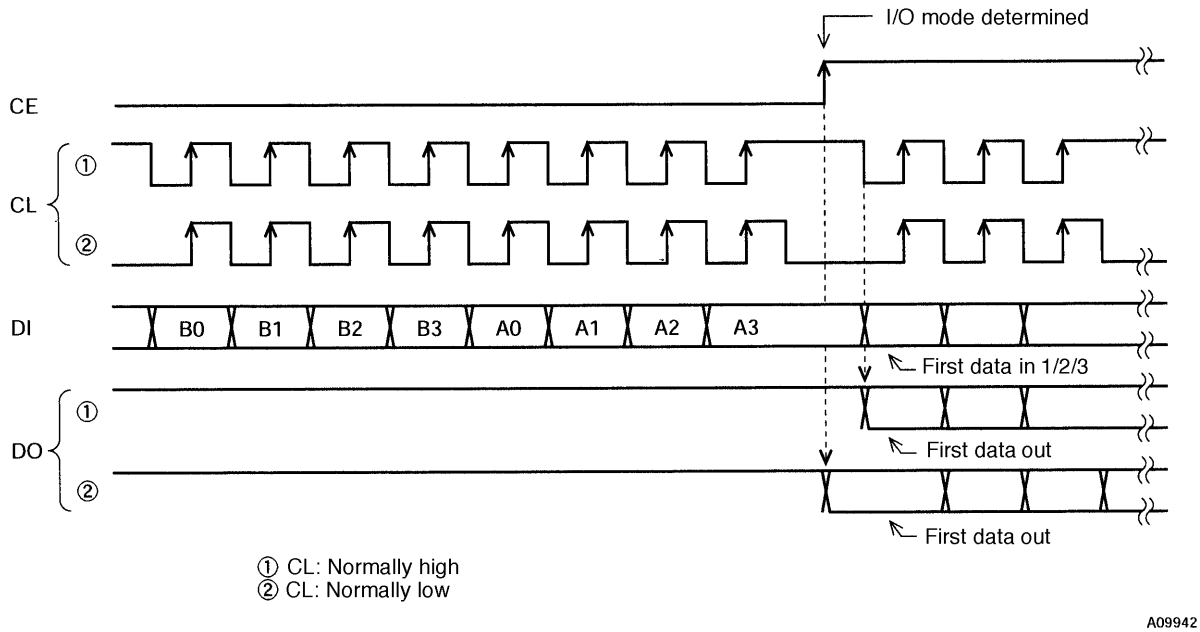
Pin	Pin No.	Type	Function	Equivalent circuit
IFIN1	15	IF counter 1	• IFIN1 is selected when LCTS in the serial data is set to 0. • The input frequency range is 0.4 to 25 MHz when IFS is 1, and 0.4 to 12 MHz when IFS is 0. • The signal is passed directly to the IF counter. • The result is output, MSB first, through the DO pin. • Four measurement periods are supported: 4, 8, 32, and 64 ms.	 A09937
IFIN2/I1	13	IF counter 2 input port	• IFIN2 is selected when both LCTS and L/I1 in the serial data are set to 1. • The input frequency range is 0.4 to 25 MHz when IFS is 1 and 0.4 to 12 MHz when IFS is 0. • The signal is passed directly to the IF counter. • The result (the IF counter value) is output, MSB first, through the DO pin. • Four measurement periods are supported: 4, 8, 32, and 64 ms. • If the L/I1 bit in the serial data is set to 0, the IFIN2/I1 port will function as an input port and the state of the input pin will be reported to the microcontroller from the DO pin. (Note that the LCTS value is ignored in this case.) When the input state is low: the data will be 0: When the input state is high: the data will be 1:	 A09938
FMINb	12	Sub PLL local oscillator signal input	• FMINb is selected when SDVS in the serial data is set to 1. • The input frequency range is 10 to 160 MHz. • The signal is passed through an internal divide-by-two prescaler and then input to the swallow counter. • The divisor can be set to a value in the range 272 to 8191. Since the internal divide-by-two prescaler is used, the actual divisor will be twice the set value. • FMINb goes to the stopped state (pulled down) when SDVS in the serial data is set to 0.	 A09939
PDb	11	Sub PLL charge pump output	• Sub PLL charge pump output A high level is output from the PD pin when the frequency of the local oscillator signal divided by N is higher than the reference frequency, and a low level is output when that frequency is lower. This pin goes to the high-impedance state when the frequencies match.	 A09940
AINb AOUTb	10 9	Sub PLL low-pass filter amplifier transistor	• Connections for the n-channel MOS transistor used for the sub PLL active low-pass filter.	 A09941

Procedures for Input and Output of Serial Data

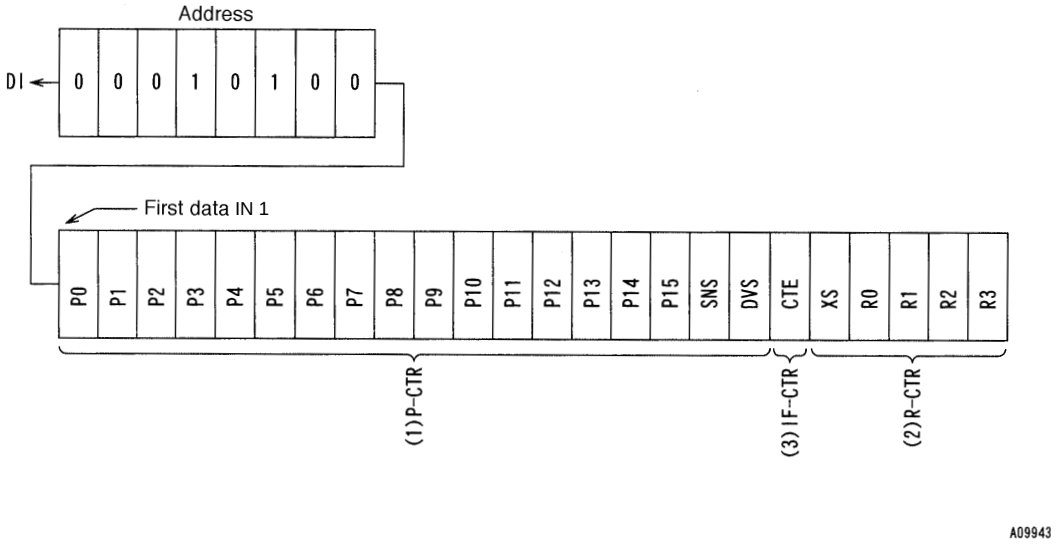
This product uses the CCB (Computer Control Bus), which is Sanyo's audio product serial bus format, for data input and output. This product adopts an 8-bit address CCB format.

	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
1	IN1 (82)	0	0	0	1	0	1	0	0	• Control data input (serial data input) mode • 24 bits of data are input. • See the "DI Control Data (serial data input)" section for details on the content of the input data.
2	IN2 (92)	1	0	0	1	0	1	0	0	• Control data input (serial data input) mode • 24 bits of data are input. • See the "DI Control Data (serial data input)" section for details on the content of the input data.
3	IN3 (B2)	1	1	0	1	0	1	0	0	• Control data input (serial data input) mode • 24 bits of data are input. • See the "DI Control Data (serial data input)" section for details on the content of the input data.
4	OUT (A2)	0	1	0	1	0	1	0	0	• Data output (serial data output) mode • The number of bits output is equal to the number of clock cycles. • See the "DO Control Data (serial data output)" section for details on the content of the output data.

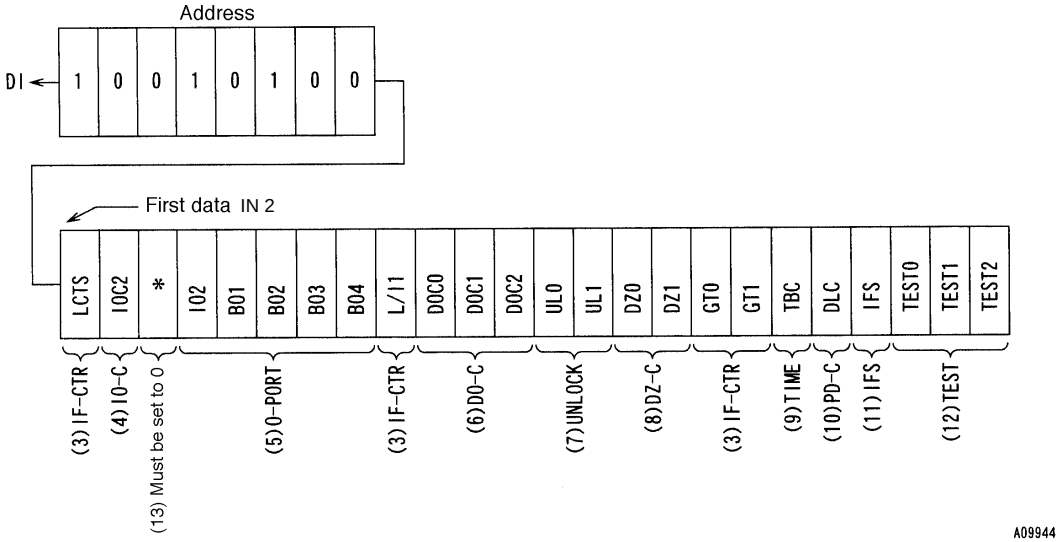


Structure of the DI Control Data (serial data input)

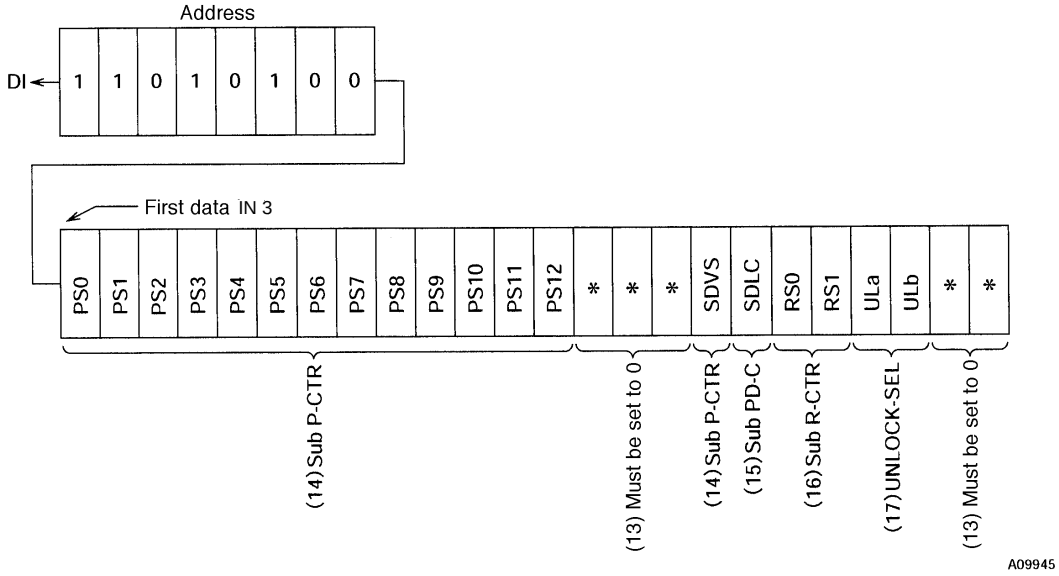
• IN1 (Main PLL/Latch-a)



• IN2 (Main PLL/Latch-a)



• IN3 (Sub PLL/Latch-b)



DI Control Data

<table>
<tr><th>No.</th><th>Control block/data</th><th>Function</th><th>Related data</th></tr>
<tr><td>1</td><td>Main PLL programmable divider data
P0 to P15
DVS, SNS</td><td>
• Specifies the divider for the main PLL programmable divider.
This is a binary value in which P15 is the MSB. The position of the LSB changes depending on DVS and SNS.
(* : don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Set divisor (N)</th><th>Actual divisor</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The set value</td></tr>
</table>
* LSB: When P4 is the LSB, P0 to P3 are ignored.
• These pins select the signal input to the main PLL programmable divider (FMINa or AMIN) and switch the input frequency range.
(* : don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Frequency range accepted by the input pin</th></tr>
<tr><td>1</td><td>*</td><td>FMINa</td><td>10 to 160 MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr>
</table>
* See the "Structure of the Programmable Divider" section for details.
</td><td></td></tr>
<tr><td>2</td><td>Main PLL reference divider data
R0 to R3

XS</td><td>
• Selects the reference frequency for the main PLL
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT mode
In this mode, the main PLL programmable divider is stopped, the FMINa and AMIN pins are pulled down to ground, and the main PLL charge pump output goes to the high-impedance state.
* Crystal oscillator stop mode
The crystal oscillator circuit is stopped.
Therefore applications must not select this mode while the sub PLL is operating.
• Crystal oscillator element selection data
XS = 0: 4.5 MHz
XS = 1: 7.2 MHz
Note that 7.2 MHz is selected after a power on reset.
</td><td></td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Function</th><th>Related data</th></tr>
<tr><td>3</td><td>IF counter control data
CTE
GT0, GT1

IF counter selection data
LCTS
L/I1</td><td>
• IF counter measurement start command data
CTE = 1: Starts the counter
CTE = 0: Resets the counter
• Determines the IF counter measurement time.
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td></tr>
</table>
* See the “Structure of the IF Counter” section for details.
• Specifies the IF counter input pin (IFIN1 or IFIN2/I1).
LCTS = 0: IFIN1
LCTS = 1: IFIN2/I1
L/I1 = 0: I1 (Input port)
L/I1 = 1: IFIN2 (IF counter 2)
<table>
<tr><th>LCTS</th><th>L/I1</th><th>IFIN2/I1 pin</th><th>IFIN1 pin</th></tr>
<tr><td>0</td><td>0</td><td>I1 (Input port)</td><td rowspan="2">IFIN1 (IF counter 1)</td></tr>
<tr><td>0</td><td>1</td><td>OFF (Pulled down)</td></tr>
<tr><td>1</td><td>0</td><td>I1 (Input port)</td><td rowspan="2">OFF (Pulled down)</td></tr>
<tr><td>1</td><td>1</td><td>IFIN2 (IF counter 2)</td></tr>
</table>
</td><td>IFS</td></tr>
<tr><td>4</td><td>I/O port setup data
IOC2</td><td>
• Specifies input or output for the shared function I/O pin ($\overline{IO2}$).
Data = 0: Input port
Data = 1: Output port
</td><td></td></tr>
<tr><td>5</td><td>Output port data
BO1 to BO4
IO2</td><td>
• Determines the output state of the $\overline{BO1}$ through $\overline{BO4}$ and $\overline{IO2}$ output ports.
Data = 0: Open
Data = 1: Low level
• The data is reset to 0, setting the pins to the open state, after a power on reset.
</td><td>IOC2</td></tr>
</table>

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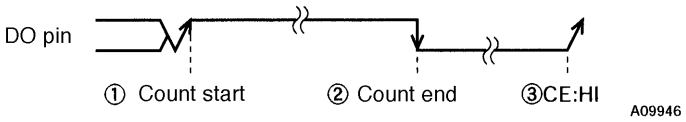
<table>
<tr><th>No.</th><th>Control block/data</th><th>Function</th><th>Related data</th></tr>
<tr><td>6</td><td>DO pin control data
DOC0
DOC1
DOC2</td><td>
• Determines the DO pin output.
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when the PLL is unlocked</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC (See *1 below.)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>IFIN2/I1 pin state (*2)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The $\overline{IO2}$ pin state (*3)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
The open state is selected after a power on reset.
*1. end-UC: IF counter measurement end check


(1) When end-UC is selected and an IF count is started (by switching CTE from 0 to 1), the DO pin automatically goes to the open state.
(2) When the IF counter measurement period completes, the DO pin goes to the low level, allowing applications to test for the completion of the count period.
(3) The DO pin is set to the open state by performing a serial data input or output operation (when the CE pin is set high).
*2. Valid when the IFIN2/I1 pin is set to the input port state (L/I1 = 0).
(The DO pin will go to the open state if L/I1 is set to 1.)
*3. Goes to the open state when the IO pin is set to the output state.
Note: During the data input period (the period that CE is high in IN1, IN2, or IN3 mode), the DO pin goes to the open state regardless of the DO pin control data (DOC0 to DOC2). During the data output period (the period that CE is high in OUT mode) the DO pin state reflects the internal DO serial data in synchronization with the CL clock, regardless of the DO pin control data (DOC0 to DOC2).
</td><td>UL0, UL1
ULa, ULb
CTE

L/I1
IOC2</td></tr>
<tr><td>7</td><td>Unlocked state detection data

UL0, UL1</td><td>
• Selects the width of the phase error (øE) detected for PLL lock state discrimination. A phase error is recognized if a phase error in excess of the detection width occurs.
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detection output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>øE is output directly</td></tr>
<tr><td>1</td><td>0</td><td>±0.55 µs</td><td>øE is extended by 1 to 2 ms</td></tr>
<tr><td>1</td><td>1</td><td>±1.11 µs</td><td>øE is extended by 1 to 2 ms</td></tr>
</table>
* When the PLL is unlocked, the DO pin goes low and UL in the serial data output is set to 0.
When the PLL is locked, the DO pin goes high and UL in the serial data output is set to 1.
</td><td>DOC0
DOC1
DOC2</td></tr>
<tr><td>8</td><td>Phase comparator control data

DZ0, DZ1</td><td>
• Controls the phase comparator dead zone
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead band mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
Dead zone width: DZA < DZB < DZC < DZD
</td><td></td></tr>
<tr><td>9</td><td>Clock time base
TBC</td><td>• Setting the TBC bit to 1 causes an 8-Hz clock time base signal with a 40% duty to be output from the $\overline{BO1}$ pin. (The BO1 data will be ignored.)</td><td>BO1</td></tr>
</table>

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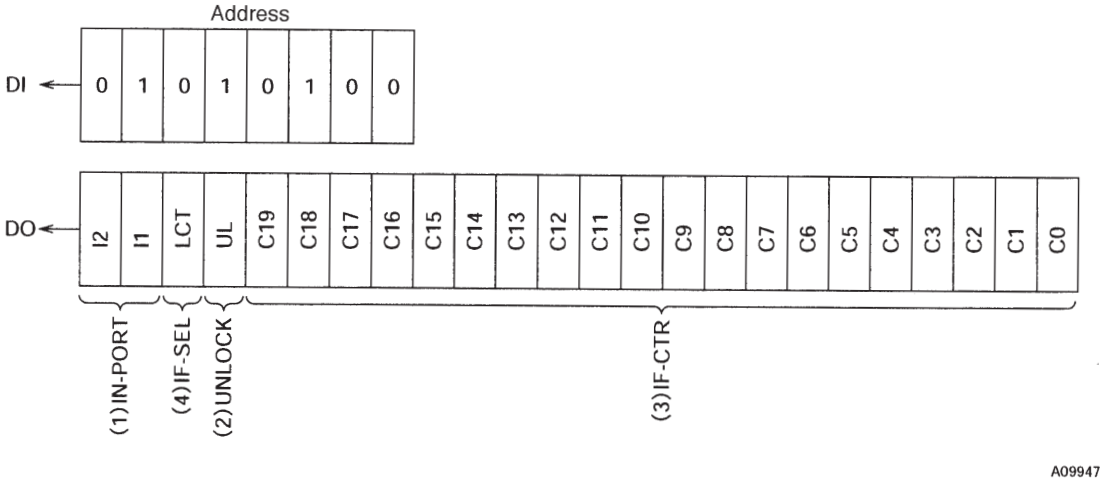
<table>
<tr><th>No.</th><th>Control block/data</th><th>Function</th><th>Related data</th></tr>
<tr><td>10</td><td>Main charge pump control data
DLC</td><td>• Controls the charge pump output (PDa).
<table><tr><th>DLC</th><th>Charge pump output</th></tr><tr><td>0</td><td>Normal operation</td></tr><tr><td>1</td><td>Forced to low</td></tr></table>* If the circuit deadlocks due to the VCO control voltage (Vtune) being 0 and the VCO being stopped, applications can get out of the deadlocked state by setting the charge pump output to low and setting Vtune to V_{CC}. (Deadlock clear circuit)</td><td></td></tr>
<tr><td>11</td><td>IFS</td><td>• This data is normally set to 1. Setting this data to 0 sets the circuit to reduced input sensitivity mode, in which the sensitivity is reduced by about 10 to 30 mV rms.</td><td></td></tr>
<tr><td>12</td><td>Test data
TEST0 to 2</td><td>• Test data
TEST0, TEST1, TEST2 — All these bits must be set to 0.
All these bits are set to 0 after a power on reset.</td><td></td></tr>
<tr><td>13</td><td>*</td><td>• This bit must be set to 0.</td><td></td></tr>
<tr><td>14</td><td>Sub PLL programmable divider data
PS0 to 12
SDVS</td><td>• Specifies the divisor for the sub PLL programmable divider (FMINb).
This is a binary value in which PS0 is the LSB and PS12 the MSB.
• The divisor can be set to a value in the range 272 to 8191. Since the internal divide-by-two prescaler is used, the actual divisor will be twice the set value.
• Sets the sub PLL programmable divider operating state.
<table><tr><th>SDVS</th><th>Operating state</th><th>Input pin frequency range</th></tr><tr><td>1</td><td>The FMINb counter operates</td><td rowspan="2">10 to 160 MHz</td></tr><tr><td>0</td><td>The FMINb counter is stopped
(FMINb is pulled down)</td></tr></table>*: See the “Structure of the Programmable Divider” section for details.</td><td></td></tr>
<tr><td>15</td><td>Sub PLL charge pump control data
SDLC</td><td>• Forcibly controls the charge pump output (PDb).
<table><tr><th>SDLC</th><th>Charge pump output</th></tr><tr><td>0</td><td>Normal operation</td></tr><tr><td>1</td><td>Forced to low</td></tr></table>* If the circuit deadlocks due to the VCO control voltage (Vtune) being 0 and the VCO being stopped, applications can get out of the deadlocked state by setting the charge pump output to low and setting Vtune to V_{CC}. (Deadlock clear circuit)</td><td></td></tr>
<tr><td>16</td><td>Sub PLL reference divider data
RS0, RS1</td><td>• Sub PLL reference frequency (fref) selection data
<table><tr><th>RS1</th><th>RS0</th><th>Reference frequency</th></tr><tr><td>0</td><td>0</td><td>50 kHz</td></tr><tr><td>0</td><td>1</td><td>25</td></tr><tr><td>1</td><td>0</td><td>12.5</td></tr><tr><td>1</td><td>1</td><td>15</td></tr></table></td><td></td></tr>
<tr><td>17</td><td>Unlocked state detection output switching data
ULa, ULb</td><td>• The unlocked state information output from the DO pin can be selected to be that for either the main PLL or the sub PLL.
<table><tr><th>ULb</th><th>ULa</th><th>Unlocked state information</th></tr><tr><td>0</td><td>0</td><td>No unlocked state information is output. The output data, UL is 1.</td></tr><tr><td>0</td><td>1</td><td>Main PLL unlocked state information</td></tr><tr><td>1</td><td>0</td><td>Sub PLL unlocked state information</td></tr><tr><td>1</td><td>1</td><td>Main PLL plus sub PLL unlocked state information.
(Indicates that either the main or the sub PLL is unlocked.)</td></tr></table></td><td></td></tr>
</table>

Structure of the DO Output Data (serial data output)

• OUT mode

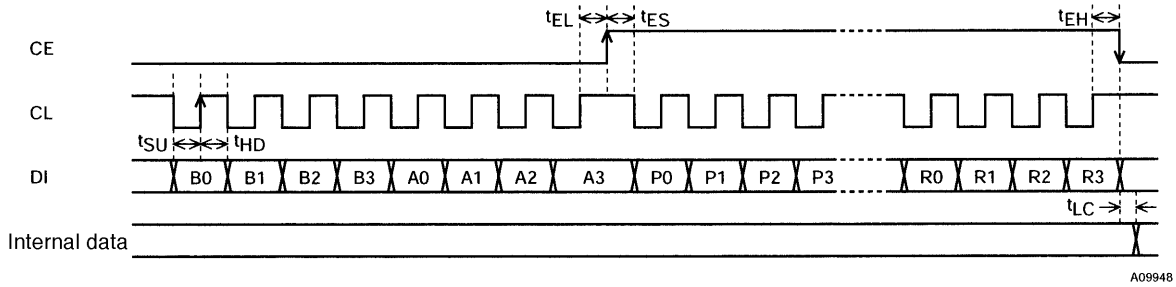


DO Output Data

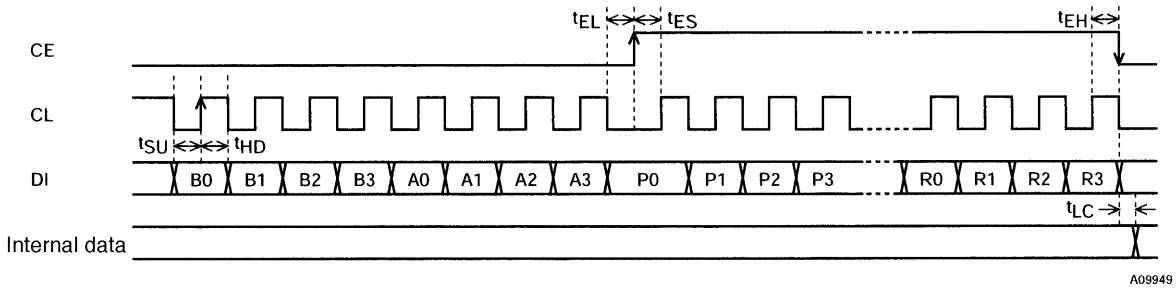
No.	Control block/data	Description	Related data
1	I/O port data 12, I1	• Data latched from the IFIN2/I1 input port (when L/I1 is 0) and the I/O port $\overline{IO2}$ pin. The I2 data reflects the pin state regardless of the I/O port mode (input or output). The data is latched at the point the circuit enters data output mode (OUT mode). The data is latched at the point the circuit enters data output mode (OUT mode). I1 ← IFIN2/I1 pin state ┐ H : 1 I2 ← The $\overline{IO2}$ pin state ┘ L : 0	L/I1 IOC2
2	PLL unlocked state data UL	• Indicates the state of the unlocked state detection circuit. UL ← 0: When the PLL is unlocked. UL ← 1: When the PLL is locked or in the detection disabled mode.	UL0, UL1 ULa, ULb
3	IF counter binary data C19 to C0	• Indicates the value of the IF counter (20-bit binary counter). C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTE GT0 GT1
4	IF counter selection data LCT	• Data that reflects the LCTS bit in the serial input data. The LCT output data allows applications to verify the IF counter input pin selection (IFIN1 or IFIN2). LCT = 0: IFIN1 selected. LCT = 1: IFIN2/I1 selected.	LCTS

Serial Data Input (IN1/IN2/IN3) t_{SU}, t_{HD}, t_{EL}, t_{ES}, $t_{EH} \geq 0.75$ µs $t_{LC} < 0.75$ µs

• CL: Normal (high)

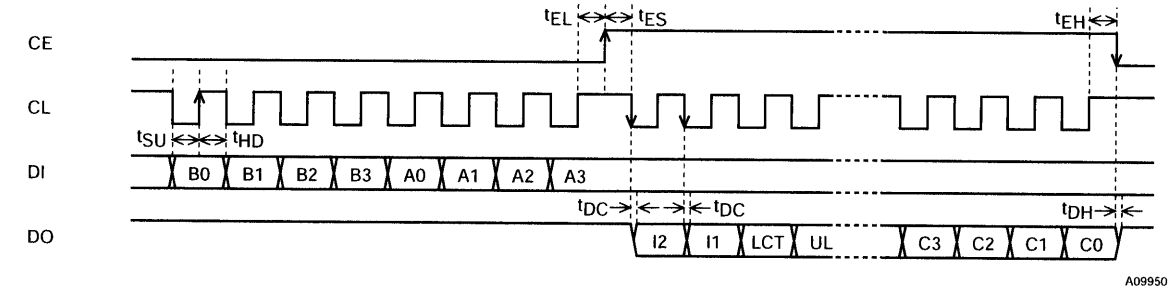


• CL: Normal (low)

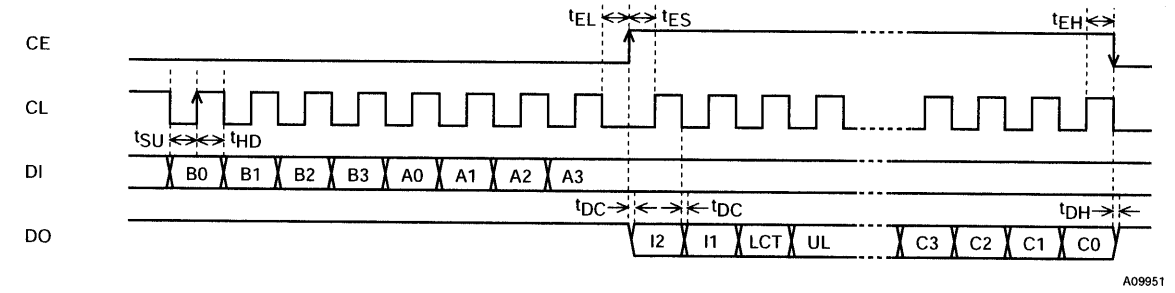


Serial Data Output (Out) t_{SU}, t_{HD}, t_{EL}, t_{ES}, $t_{EH} \geq 0.75$ µs t_{DC}, $t_{DH} < 0.35$ µs

• CL: Normal (high)

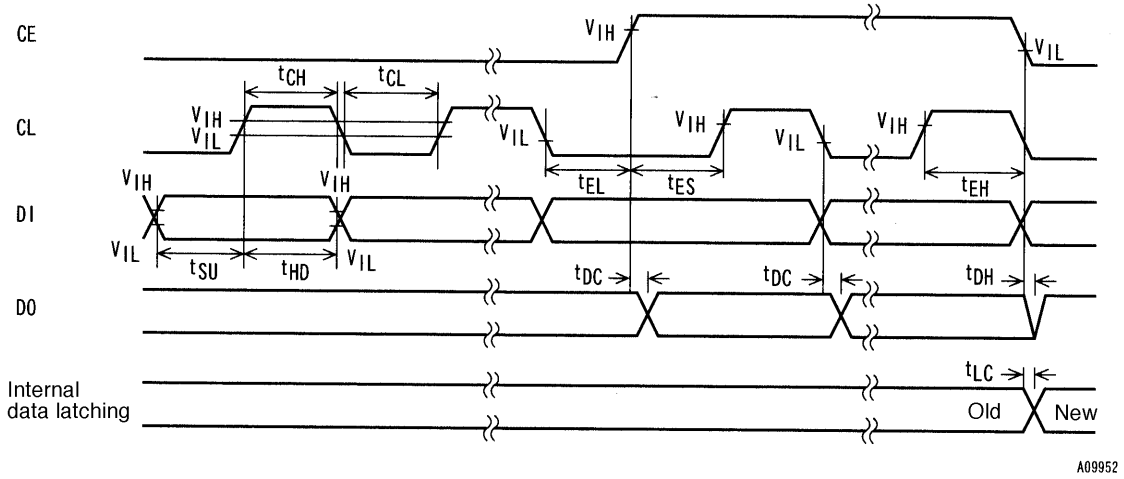


• CL: Normal (low)

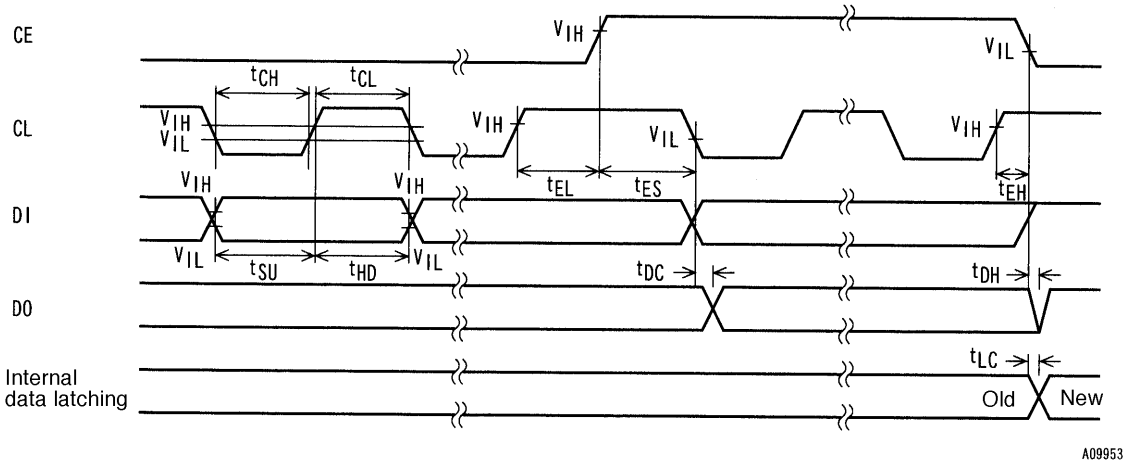


Note: The data conversion times (t_{DC} and t_{DH}) depend on the value of the pull-up resistor and the printed circuit board capacitance since the DO pin is an n-channel open-drain circuit.

Serial Data Timing



When CL is stopped at the low level

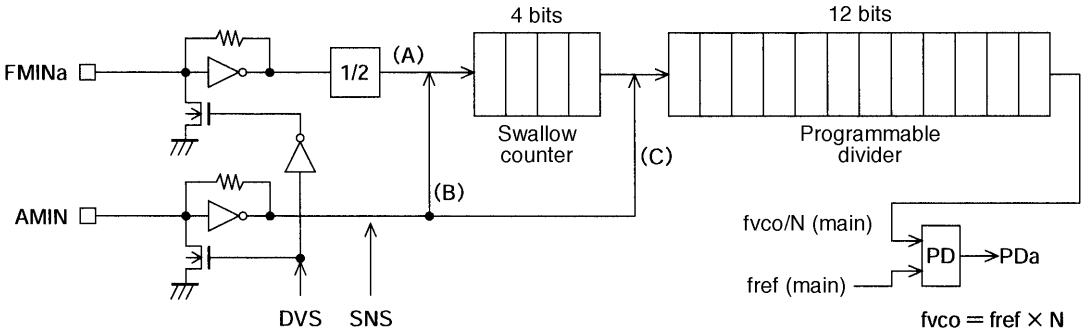


When CL is stopped at the high level

Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Data setup time	t_{SU}	DI, CL		0.75			µs
Data hold time	t_{HD}	DI, CL		0.75			µs
Clock low level time	t_{CL}	CL		0.75			µs
Clock high level time	t_{CH}	CL		0.75			µs
CE wait time	t_{EL}	CE, CL		0.75			µs
CE setup time	t_{ES}	CE, CL		0.75			µs
CE hold time	t_{EH}	CE, CL		0.75			µs
Data latch change time	t_{LC}					0.75	µs
Data output time	t_{DC}	DO, CL	These values differ depending on the value of the pull-up resistor used and the printed circuit board capacitance			0.35	µs
	t_{DH}	DO, CE				0.35	µs

Structure of the Programmable Divider

Structure of the Main PLL Programmable Divider



	DVS	SNS	Input pin	Set divisor	Actual divisor	Input frequency range
A	1	*	FMINa	272 to 65535	Twice the set value	10 to 160 MHz
B	0	1	AMIN	272 to 65537	The set value	2 to 40 MHz
C	0	0	AMIN	4 to 4095	The set value	0.5 to 10 MHz

*: Don't care

Sample Main Programmable Divider Divisor Calculations

- For FM with a step size of 50 kHz (DVS = 1, SNS = *: FMINa selected)
  FM RF = 90.0 MHz (IF = +10.7 MHz)
  FM VCO = 100.7 MHz
  Main PLL fref = 25 kHz (R0 = 1, R1 = 1, R2 = 0, R3 = 0)
  100.7 MHz (FM VCO) ÷ 25 kHz (fref) ÷ 2 (for the FMIN 1/2 prescaler) = 2014 → 07DE (hexadecimal)

	E				D				7				0											
	0	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	*	1			1	1	0	0
	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A09955

- For SW with a step size of 5 kHz (DVS = 0, SNS = 1: AMIN high-speed operation selected)
  SW RF = 21.75 MHz (IF = +450 kHz)
  SW VCO = 22.20 MHz
  Main PLL fref = 5 kHz (R0 = 0, R1 = 1, R2 = 0, R3 = 1)
  22.2 MHz (SW VCO) ÷ 5 kHz (fref) = 4440 → 1158 (hexadecimal)

	8				5				1				1											
	0	0	0	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0			0	1	0	1
	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

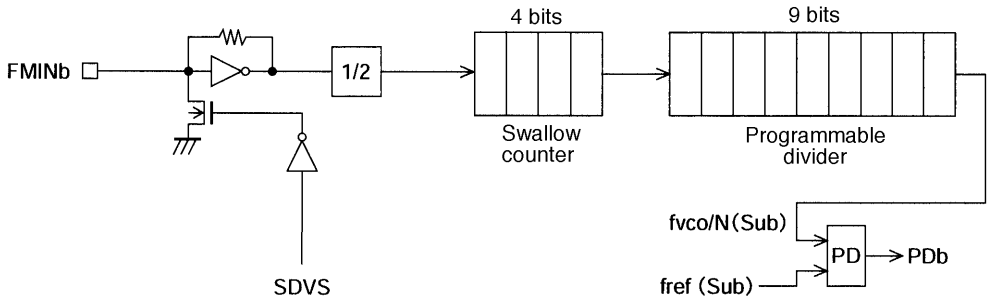
A09956

- For MW with a step size of 10 kHz (DVS = 0, SNS = 0: AMIN low-speed operation selected)
  MW RF = 1000 kHz (IF = +450 kHz)
  WM VCO = 1450 kHz
  Main PLL fref = 10 kHz (R0 = 0, R2 = 0, R3 = 1)
  1450 kHz (MW VCO) ÷ 10 kHz (fref) = 145 → 091 (hexadecimal)

					1				9				0											
	*	*	*	*	1	0	0	0	1	0	0	1	0	0	0	0	0	0			0	0	0	1
	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A09957

Structure of the Sub PLL Programmable Divider



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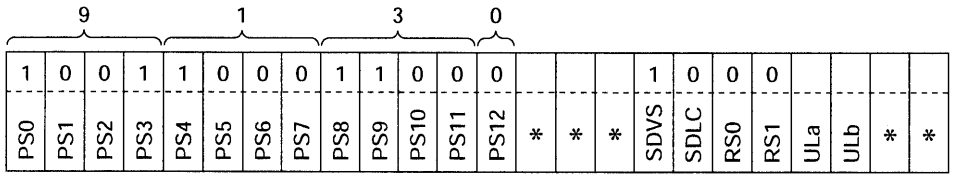
SDVS	Operating state	Set divisor	Actual divisor: N	Input frequency range
1	FMINb operating	272 to 8191	Twice the set value	10 to 160 MHz
0	FMINb stopped (pulled down)	—	—	—

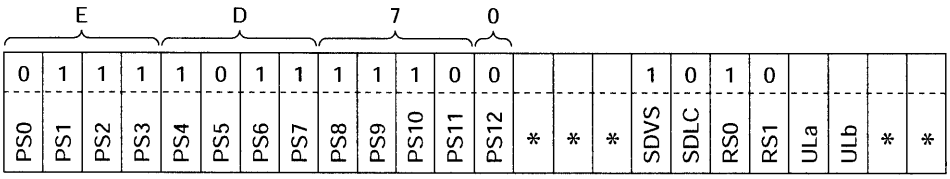
Sample Sub PLL Programmable Divider Divisor Calculations

- For FM with a step size of 100 kHz (SDVS = 1: FMINb operating)
  FM RF = 90.0 MHz (IF = –10.7 MHz)
  FM VCO = 79.3 MHz
  Sub PLL fref = 50 kHz (RS0 = 0, RS1 = 0)
  79.3 MHz (FM VCO) ÷ 50 kHz (fref) ÷ 2 (for the FMINb 1/2 prescaler) = 793 → 0319 (hexadecimal)



A09959

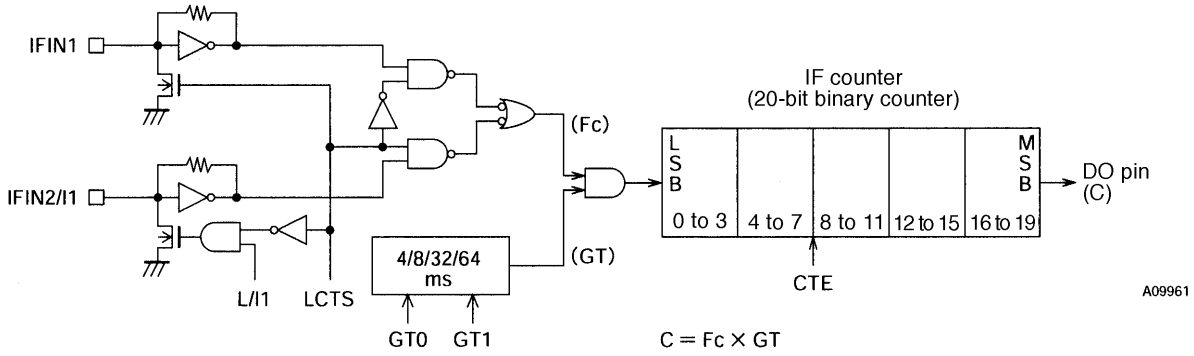
- For FM with a step size of 50 kHz (SDVS = 1: FMINb operating)
  FM RF = 90.0 MHz (IF = +10.7 MHz)
  FM VCO = 100.7 MHz
  Sub PLL fref = 25 kHz (RS0 = 1, RS1 = 0)
  100.7 MHz (FM VCO) ÷ 25 kHz (fref) ÷ 2 (for the FMINb 1/2 prescaler) = 2014 → 07DE (hexadecimal)



A09960

Structure of the IF Counter

The LC72134M IF counter is a 20-bit binary counter, and takes the IF signal from the IFIN1 or IFIN2/I1 pin as its input. The result of the count can be read out serially MSB first from the DO pin.



GT1	GT0	Measurement time	
		Measurement time (GT)	Wait time (t_{WU})
0	0	4 ms	3 to 4 ms
0	1	8	3 to 4
1	0	32	7 to 8
1	1	64	7 to 8

The IF frequency (FC) is measured by determining how many pulses were input to the IF counter in the stipulated measurement time, GT.

$Fc = \frac{C}{GT}$ $(C = Fc \times GT)$ C: Counted value (the number of pulses)

IF Counter Frequency Measurement Examples

- When the measurement time (GT) is 32 ms and the counted value (C) is 53980 (hexadecimal) or 342,400 decimal.
  IF frequency (FC) = 342400 ÷ 32 ms = 10.7 MHz

				5				3				9				8				0			
				0	1	0	1	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0
I2	I1	LCT	UL	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

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- When the measurement time (GT) is 8 ms and the counted value (C) is E10 (hexadecimal) or 3600 decimal.
  IF frequency (FC) = 3600 ÷ 8 ms = 450 kHz

				0				0				E				1				0			
				0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0
I2	I1	LCT	UL	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

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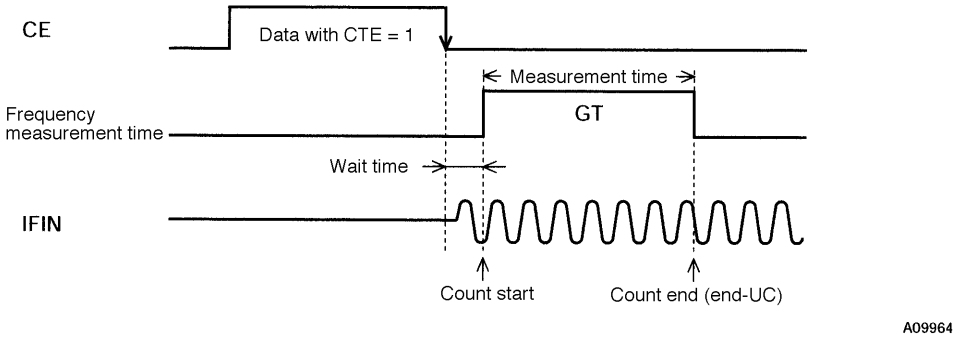
IF Counter Operation



Applications must first, before starting an IF count operation reset the IF counter by setting CTE in the serial data to 0.
The IF counter operation is started setting CTE in the serial data from 0 to 1. Although the serial data is determined by dropping the CE pin from high to low, the IF signal input to the IFIN pin must be provided within the wait time from the point CE goes low. Next, the readout of the IF counter after measurement is complete must be performed while CTE is still 1, since the counter will be reset if CTE is set to 0.

Note: If IF counting is used, applications must determine whether or not the IF IC SD (station detect) signal is present in the microcontroller software, and perform the IF count only if that signal is asserted. This is because auto-search techniques that only use IF counting are subject to incorrect stopping at points where there is no station due to IF buffer leakage.

Unlocked State Detection Timing

- Unlocked state detection timing

  Unlocked state detection is performed during the reference frequency (fref) period (interval). This means that a period at least as long as the period of the reference frequency is required to recognize the locked/unlocked state. However, applications must wait at least twice the period of the reference frequency immediately after changing the divisor (N) (which is applied to the frequency) before checking the locked/unlocked state.

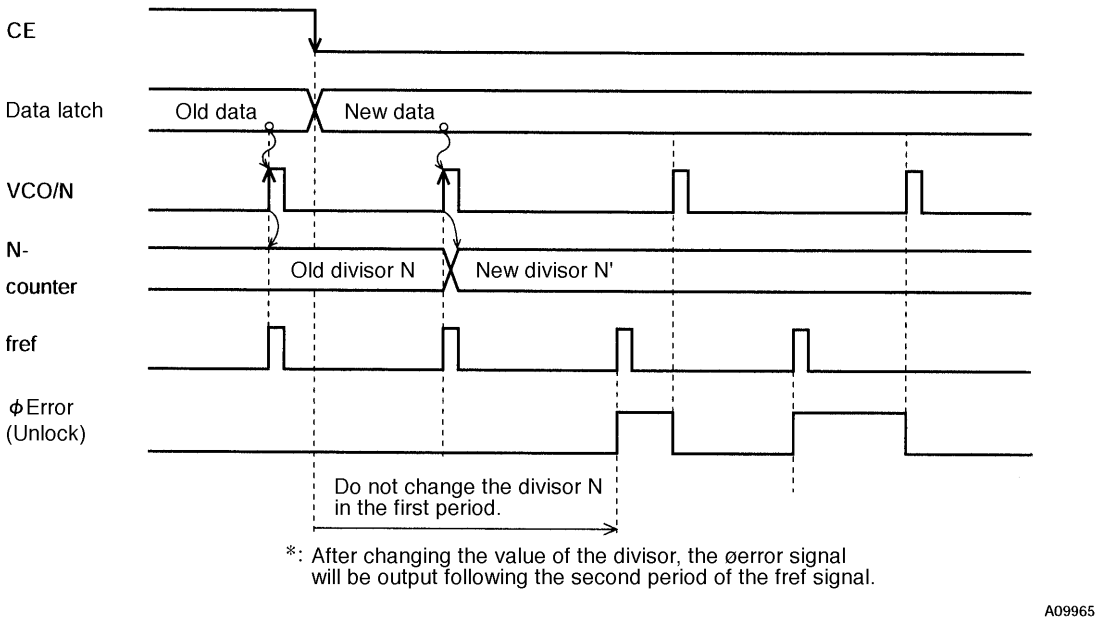


Figure 1 Unlocked State Detection Timing

For example, if fref is 1 kHz (a period of 1 ms) applications must wait at least 2 ms after the divisor N is changed before performing a locked/unlocked check.

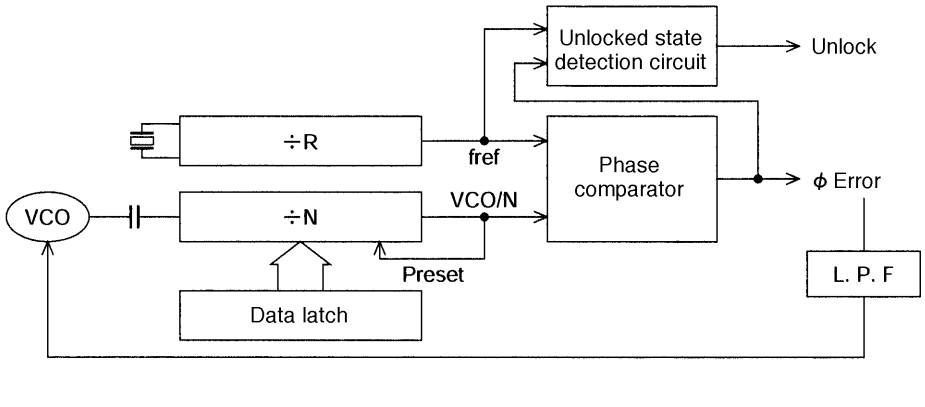


Figure 2 Circuit Structure

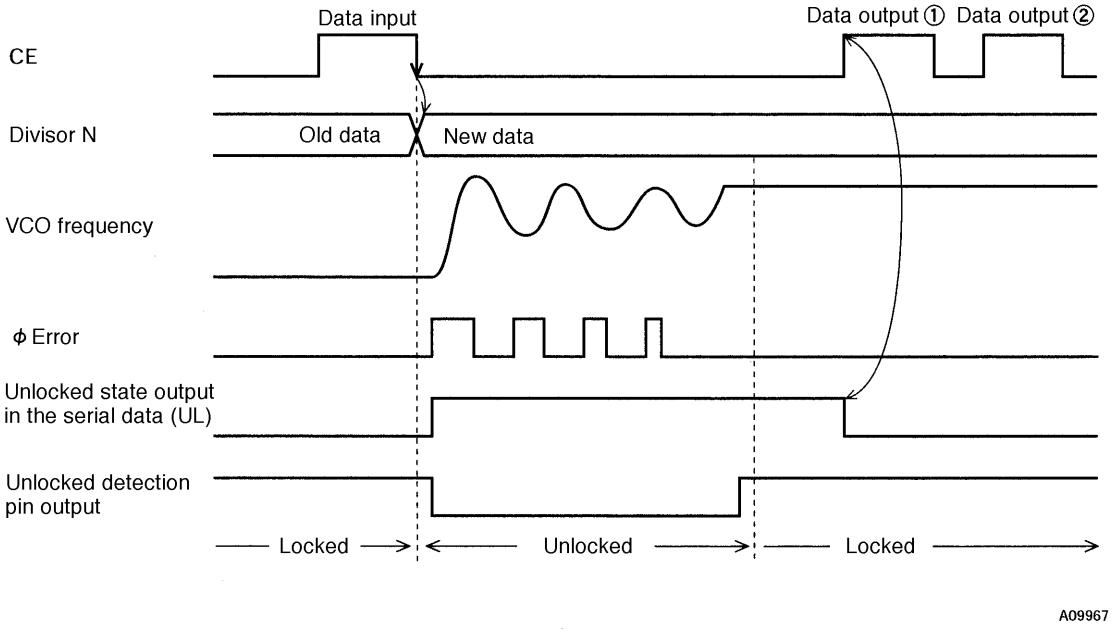
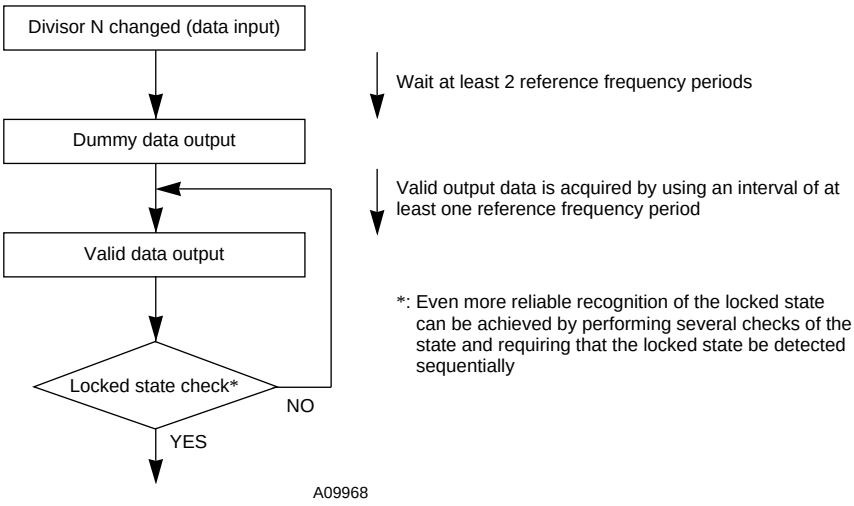


Figure 3 Combining with Software

- Outputting the unlocked state data in the serial data
  In the LC72134M, the unlocked state data (UL), once set to the unlocked state, is not reset unless data is output (or input). At the point of data output (1) in figure 3, the VCO frequency will be stable (locked), but since the divisor N was changed and a data output operation has not yet been performed, the unlocked state data will indicate the unlocked state. Thus even though the loop is stable (locked), the data will indicate that it is not. In cases such as this, the application should treat the first data output after the value of N has been changed as dummy data, and consider the second data output (at point (2) in the figure) as valid data.

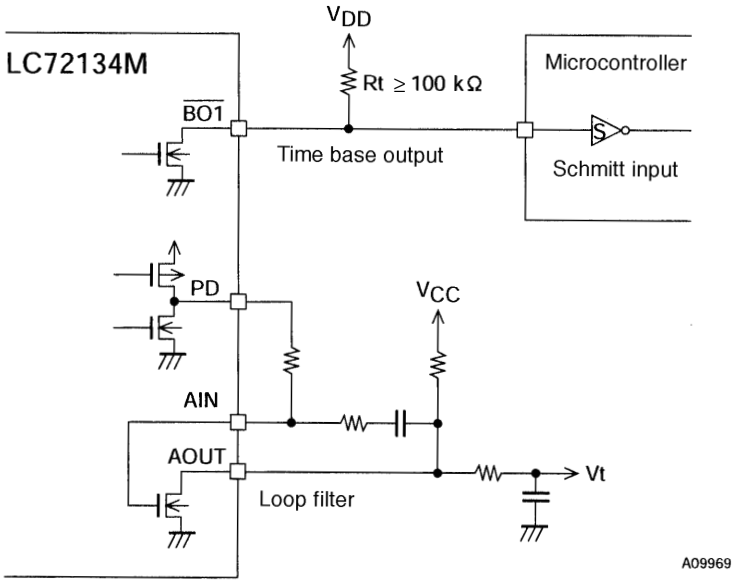
<Flowchart for Lock Detection>



- Directly outputting the unlocked state to the DO pin
  Since the unlocked state (high level when locked, low when unlocked) is output from the DO pin, the dummy data processing described above is not necessary. After N is changed, applications can check the locked state after waiting at least two periods of the reference frequency.

Clock Time Base Usage Notes

When using the clock time base output function, the output pin ($\overline{BO1}$) pull-up resistor must have a value of over 100 kΩ. The use of a Schmitt input in the microcontroller that accepts this signal is recommended to reduce chattering. This is to prevent degradation of the VCO C/N characteristics when combining with a loop filter that uses the internal transistor provided to form a low-pass filter. Since the ground for the clock time base output pin and the ground for the transistor are common internally on the chip, applications must take care to minimize current fluctuations in the time base pin to prevent degradation of the low-pass filter characteristics.



Other Items

- Notes on the phase comparator dead zone

DZ1	DZ0	Dead band mode	Charge pump	Dead band
0	0	DZA	ON/ON	– –0s
0	1	DZB	ON/ON	–0s
1	0	DZC	OFF/OFF	+0s
1	1	DZD	OFF/OFF	+ +0s

When the charge pump is used with one of the ON/ON modes, correction pulses are generated from the charge pump even if the PLL is locked. As a result, it is easy for the loop to become unstable, and special care is required in application design. The following problems can occur if an ON/ON mode is used.

— Sidebands may be created by reference frequency leakage.

— Sidebands may be created by low-frequency leakage due to the correction pulse envelope.

Although the loop is more stable when a dead zone is present (i.e. when an OFF/OFF mode is used), a dead band makes it more difficult to achieve excellent C/N characteristics. On the other hand, while it is easy to achieve good C/N characteristics when there is no dead zone, achieving good loop stability is difficult. Accordingly, the DZA and DZB settings, in which there is no dead zone, can be effective in situations where a signal-to-noise ratio of 90 to 100 dB or higher is required in FM reception, or where it is desirable to increase the pilot margin in AM stereo reception. However, if such a high signal-to-noise ratio is not required for FM reception, if an adequate pilot margin can be acquired in AM stereo reception, or if AM stereo is not required, then either DZC or DZD, in which there is a dead band, should be chosen.

Dead Zone

As shown in figure 1, the phase comparator compares a reference frequency (fr) with fp. As shown in figure 2, the phase comparator's characteristics consist of an output voltage (V) that is proportional to the phase difference ø. However, due to internal circuit delay and other factors, an actual circuit has a region (the dead zone, B) where the circuit cannot actually compare the phases. To implement a receiver with a high S/N ratio, it is desirable that this region be as small as possible. However, it is often desirable to have the dead zone be slightly wider in popularly-priced models. This is because in certain cases, such as when there is a strong RF input, popularly-priced models can suffer from mixer to VCO RF leakage that modulates the VCO. When the dead zone is small, the circuit outputs signals to correct this modulation and this output further modulates the VCO. This further modulation may then generate beats with the RF signal.

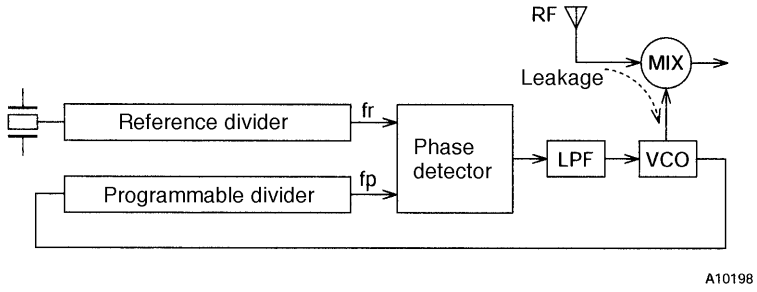


Figure 1

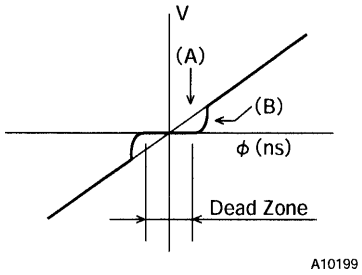


Figure 2

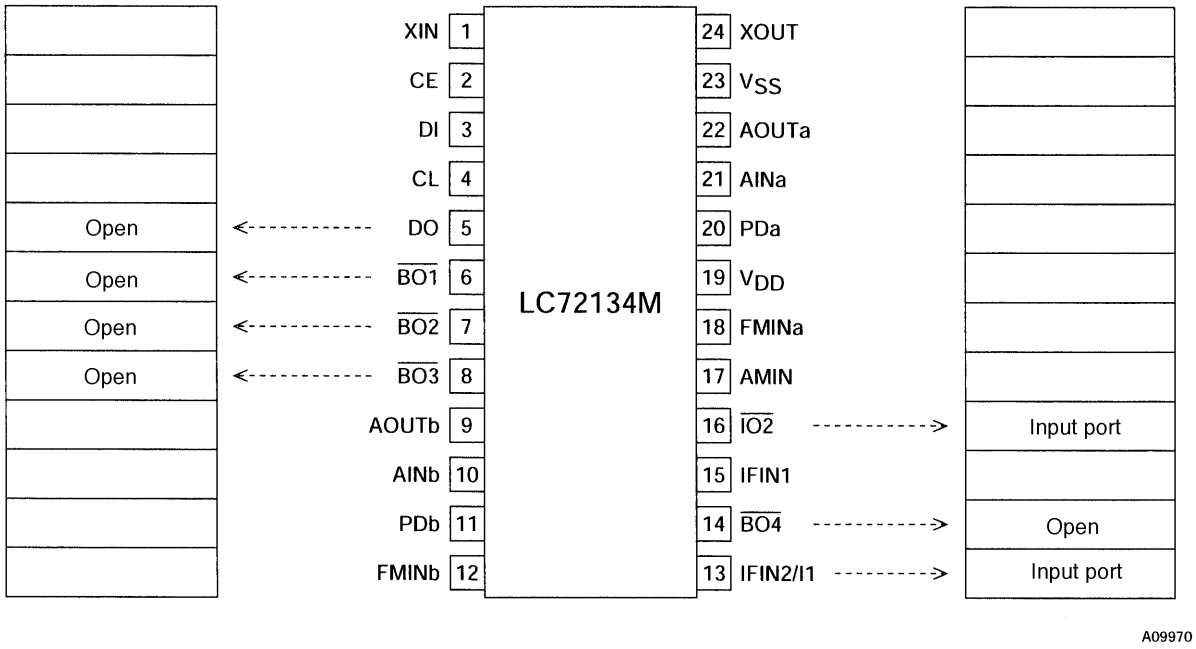
- Notes on the FMIN, AMIN, and IFIN pins
  Coupling capacitors should be placed as close to their pin as possible. A capacitance of about 100 pF is desirable for these capacitors. In particular, if the IFIN pin coupling capacitor is not held to under 100 pF, the time to reach the bias level may become too long and incorrect counts may result due to the relationship with the wait time.

- Notes on IF counting → Use the SD signal in conjunction with IF counting
  When counting the IF frequency, the microcontroller must determine the presence or absence of the IF IC SD (station detect) signal and turn on the IF counter buffer output and execute the IF count only if there is an SD signal. Auto-search techniques that only use the IF counter are subject to incorrect stopping at points where there is no station due to IF buffer leakage.

- DO pin usage
  The DO pin can be used for IF counter count completion checking and as an unlock detection output in addition to its use in data output mode. It is also possible to have the DO pin reflect the state of an input pin to input that state to the microcontroller.

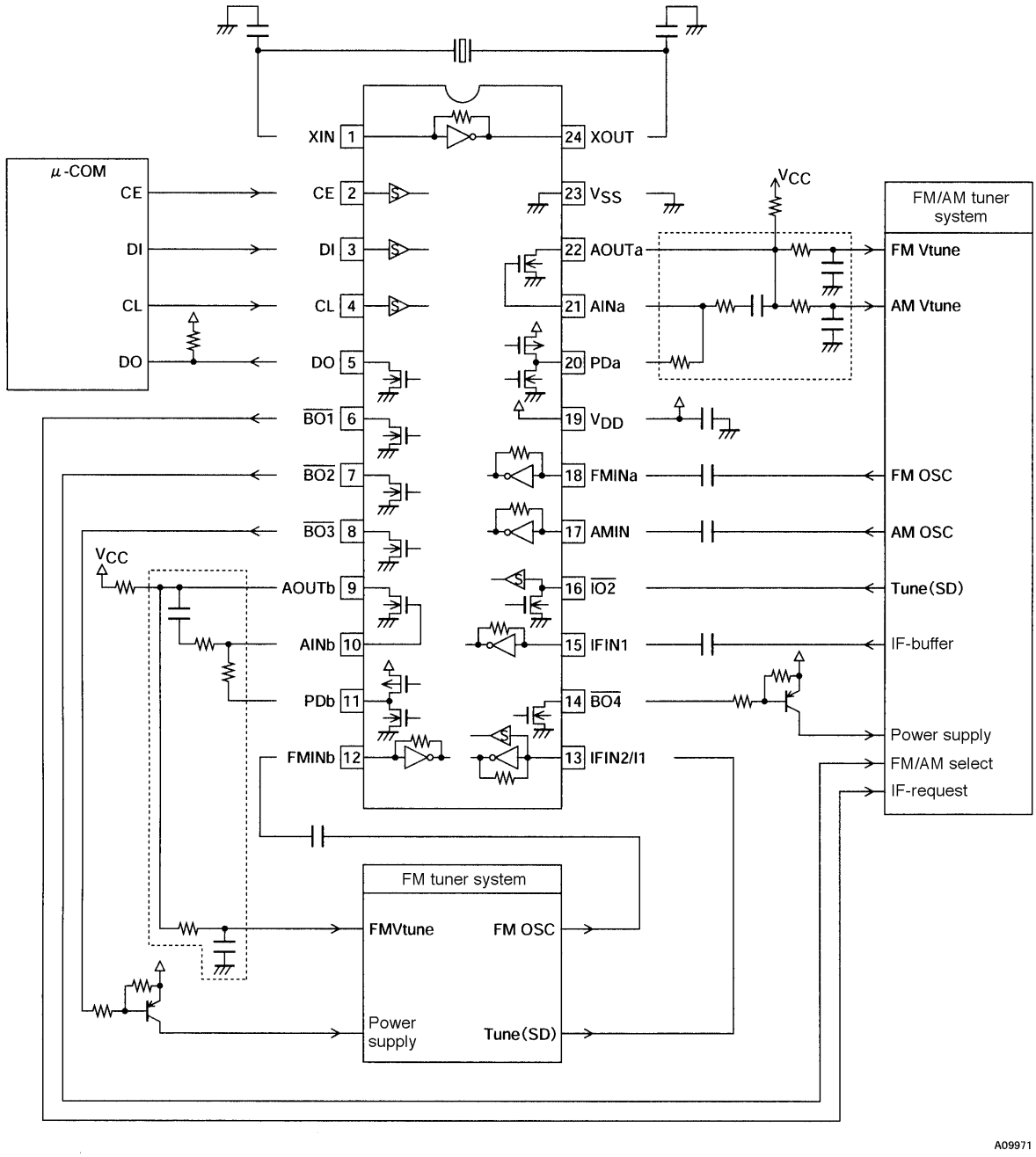
- Power supply pins
  A capacitor of at least 2000 pF must be inserted between the power supply V_{DD} and V_{SS} pins for noise exclusion. This capacitor must be placed as close as possible to the V_{DD} and V_{SS} pins.

Pin States after a Power on Reset



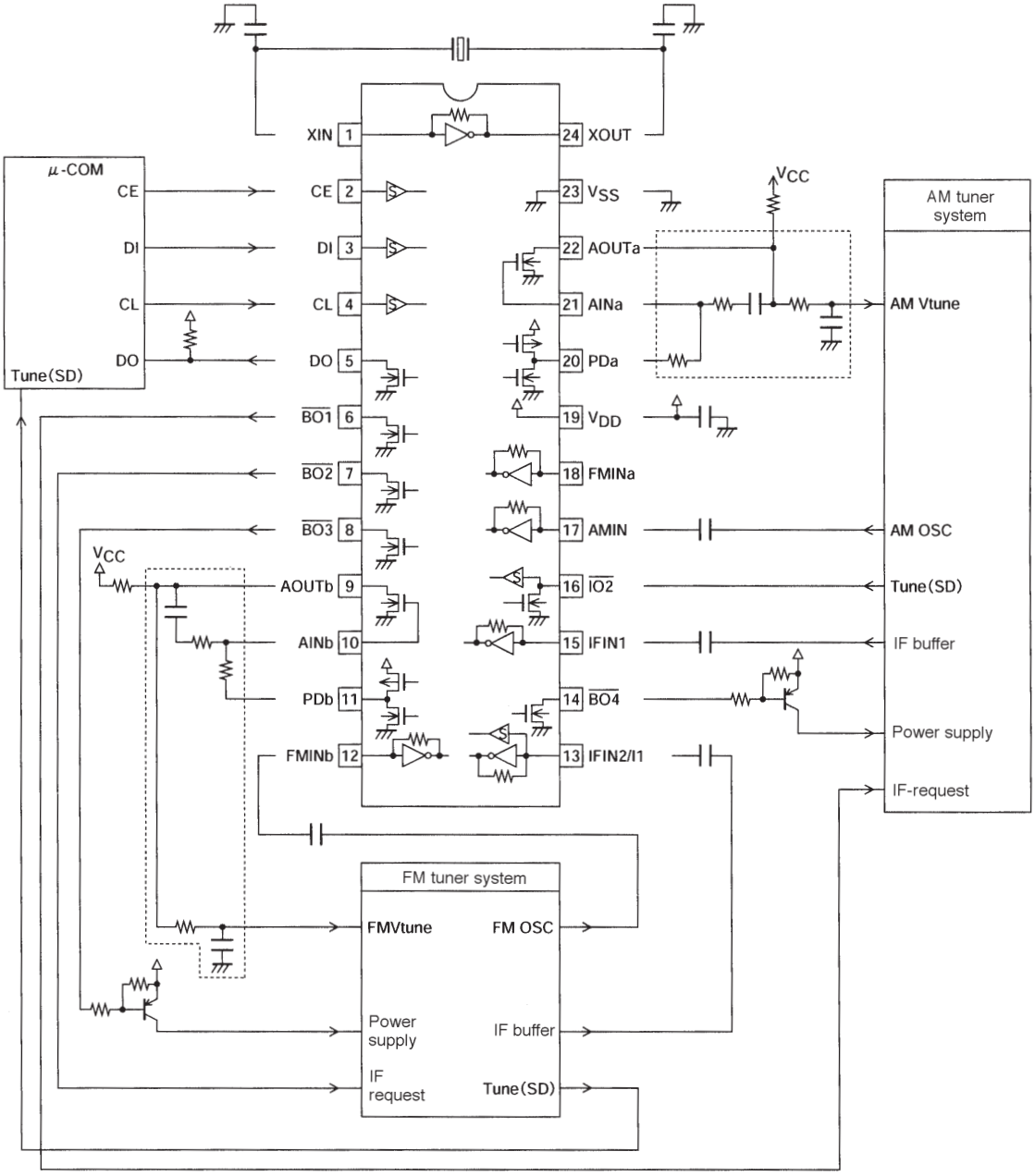
Sample Application Circuits

FM/AM Tuner + FM Tuner (for FM Subcarrier)



Note: Since the areas enclosed in dotted lines ( ) are high-impedance circuits, they are susceptible to noise. Therefore, lines in the printed circuit board pattern should be made as short as possible and these areas should be surrounded by the ground pattern.

AM Tuner + FM Tuner



Note: Since the areas enclosed in dotted lines ( ) are high-impedance circuits, they are susceptible to noise. Therefore, lines in the printed circuit board pattern should be made as short as possible and these areas should be surrounded by the ground pattern.

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