

General Purpose 133MHz System Clock

General Description

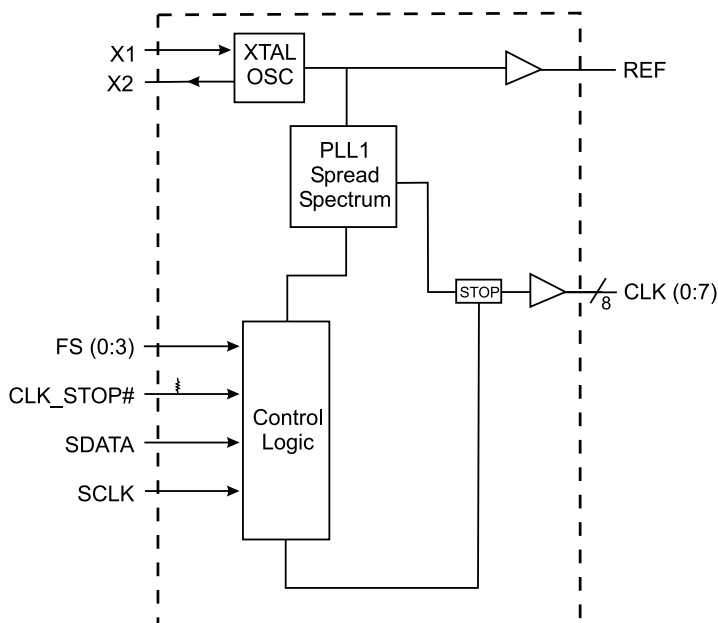
The **ICS9248-80** is a general purpose system clock. It provides 8 output CLKs, 1 REF CLK and excellent power management features through CLK_STOP#.

Spread spectrum may be enabled through I²C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-80 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

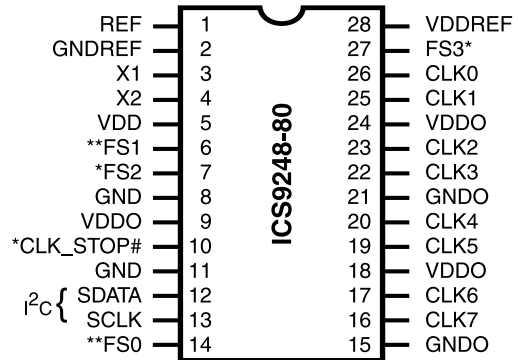
Features

- Extended temperature range (-20°C to +70°C)
- Output features:
 - 8 CLK outputs @ 3.3V, up to 133.34MHz.
 - 1-REF output @ 3.3V, 14.31818MHz.
- Spread Spectrum for EMI control
- I²C interface to stop clocks, select spread and frequency.
- Excellent power management feature through CLK_STOP# and individual stop clocks through I²C.
- Input is from a 14.31818MHz crystal.

Block Diagram



Pin Configuration



28-Pin 209 mil SSOP

- * These inputs have a 120K internal pull-up to 3.3V.
- ** These inputs have a 120K internal pull-down to GND.



Pin Descriptions

Pin number	Pin name	Type	Description
1	REF	OUT	14.318MHz reference clock outputs at 3.3V
2	GNDREF	PWR	Gnd pin for REF clocks
3	X1	IN	XTAL_IN 14.318MHz crystal input
4	X2	OUT	XTAL_OUT Crystal output
5	VDD	PWR	3.3V power input
6, 7, 14, 27	FS (0:3)	IN	Logic - input for frequency selection
8, 11	GND	PWR	Ground
9, 18, 24	VDDO	PWR	3.3V power for CLK outputs
10	CLK_STOP#	IN	Stops all clock outputs
12	SDATA	IN	Data input for I ² C serial input.
13	SCLK	IN	Clock input of I ² C input
15, 21	GND0	PWR	Ground for CLK outputs
16, 17, 19, 20, 22, 23, 25, 26	CLK (0:7)	OUT	Clock outputs up to 133.34MHz
28	VDDREF	PWR	Power pin for REF clocks

Frequency Selection

FS3	FS2	FS1	FS0	CLK (MHz)
0	0	0	0	133.34
0	0	0	1	125.01
0	0	1	0	120.00
0	0	1	1	114.99
0	1	0	0	109.99
0	1	0	1	105.00
0	1	1	0	100.00
0	1	1	1	95.00
1	0	0	0	90.00
1	0	0	1	85.01
1	0	1	0	75.00
1	0	1	1	70.00
1	1	0	0	66.67
1	1	0	1	60.00
1	1	1	0	54.99
1	1	1	1	33.33



General I²C serial interface information

The information in this section assumes familiarity with I²C programming. For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 _(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte (*Byte 0*) through *byte 5*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 _(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

ICS9248-80



Byte 0: Functionality and frequency select register (Default=0)

(1 = Running, 0 = Stopped Low)

Bit	Description	PWD																																																																																									
Bit7	0: 0 to -0.5% down spread	0																																																																																									
	1: 0 to -1.0% down spread																																																																																										
Bit (2, 6:4)	<table border="1"> <thead> <tr> <th colspan="4">Bits</th> <th rowspan="2">CLK frequency</th> </tr> <tr> <th>2</th> <th>6</th> <th>5</th> <th>4</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>133.34</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>125.01</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>120.00</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>114.99</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>109.99</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>105.00</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>100.00</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>95.00</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>91.00</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>85.01</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>75.00</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>70.00</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>66.67</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>60.00</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>54.99</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>33.33</td></tr> </tbody> </table>	Bits				CLK frequency	2	6	5	4	0	0	0	0	133.34	0	0	0	1	125.01	0	0	1	0	120.00	0	0	1	1	114.99	0	1	0	0	109.99	0	1	0	1	105.00	0	1	1	0	100.00	0	1	1	1	95.00	1	0	0	0	91.00	1	0	0	1	85.01	1	0	1	0	75.00	1	0	1	1	70.00	1	1	0	0	66.67	1	1	0	1	60.00	1	1	1	0	54.99	1	1	1	1	33.33	Note 1
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Bit3	0: Frequency is selected by hardware FS(0:3) 1: frequency is selected by bits 2, 6:4 of I ² C	0																																																																																									
Bit1	0: Normal 1: Spread	0																																																																																									
Bit0	0: Outputs running 1: Outputs tri-stated	0																																																																																									

Notes:

1. Default is for frequency control thru hardware pins.

Byte 1: CLK output control register

(1 = Running, 0 = Stopped Low)

Bit	Pin#	PWD	Description
Bit 7	16	1	CLK7
Bit 6	17	1	CLK6
Bit 5	19	1	CLK5
Bit 4	20	1	CLK4
Bit 3	22	1	CLK3
Bit 2	23	1	CLK2
Bit 1	25	1	CLK1
Bit 0	26	1	CLK0



Absolute Maximum Ratings

- Core Supply Voltage 4.6 V
- I/O Supply Voltage 3.6V
- Logic Inputs GND-0.5 V to V_{DD}+0.5 V
- Ambient Operating Temperature -20°C to +70°C
- Storage Temperature -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = -20°C - +70° C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V _{IH}		2		V _{DD} +0.3	V
Input Low Voltage	V _{IL}		V _{SS} -0.3		0.8	V
Input High Current	I _{IH}	V _{IN} = V _{DD}		0.1	5	μA
Input Low Current	I _{IL1}	V _{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		μA
Input Low Current	I _{IL2}	V _{IN} = 0 V; Inputs with pull-up resistors	-200	-100		μA
Operating Supply Current	I _{DD2.5OP}	C _L = 0 pF; Select @ 66 MHz		50	100	mA
Input frequency	F _i	V _{DD} = 3.3 V;		14.318		MHz
Input Capacitance ¹	C _{IN}	Logic Inputs			5	pF
	C _{INX}	X1 & X2 pins		6		pF
Transition Time ¹	T _{Trans}	To first crossing of target Freq.		1.3	2	ms
Settling Time ¹	T _S	From first crossing to 1% of target Freq.		0.3		ms
Clk Stabilization ¹	T _{STAB}	From V _{DD} = 3.3 V to 1% target Freq.		< 3	3	ms

¹Guaranteed by design, not 100% tested in production.

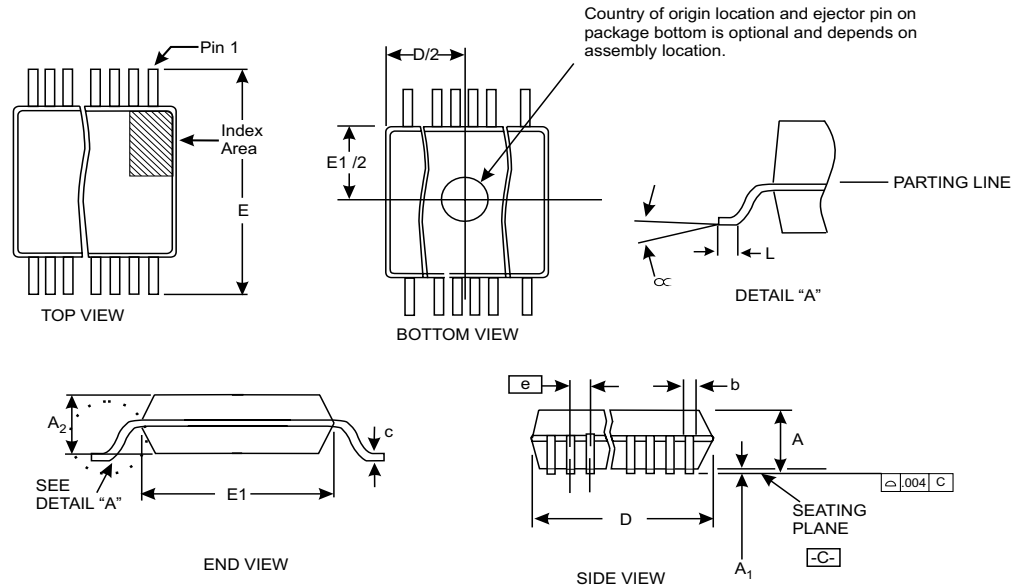


Electrical Characteristics - CLK

$T_A = -20^{\circ}\text{C} - +70^{\circ}\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	$I_{OH} = -1\text{ mA}$	2			V
Output Low Voltage	V_{OL3}	$I_{OL} = 1\text{ mA}$			0.4	V
Output High Current	I_{OH3}	$V_{OH@Min} = 1.0\text{ V}, V_{OH@Max} = 2375\text{ V}$	-27		27	mA
Output Low Current	I_{OL3}	$V_{OL@Min} = 1.2\text{ V}, V_{OL@Max} = 0.3\text{ V}$	27		30	mA
Rise Time	T_{r3}^1	$V_{OL} = 0.4\text{ V}, V_{OH} = 2.0\text{ V}$			1.33	ns
Fall Time	T_{f3}^1	$V_{OH} = 2.0\text{ V}, V_{OL} = 0.4\text{ V}$			1.4	ns
Duty Cycle	D_{t3}^1	$V_T = 1.25\text{ V}$	45	55	58	%
Skew ¹	T_{sk1}	$V_T = 1.25\text{ V}$			250	ps
Jitter, cyc-cyc	t_{jcy}	$V_T = 1.25\text{ V}$			250	ps
Jitter, Absolute ¹	t_{jabs1}	$V_T = 1.25\text{ V}$			250	ps

¹Guarenteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	-	-	0.078	14	0.232	0.244	0.256
A1	0.002	-	-	16	0.232	0.244	0.256
A2	0.065	0.069	0.073	20	0.272	0.284	0.295
b	0.009	0.012	0.015	24	0.311	0.323	0.335
c	0.004	-	0.010	28	0.390	0.402	0.413
D	See Variations			30	0.390	0.402	0.413
E1	0.197	0.209	0.220	Dimensions in inches 209 mil SSOP Package			
e	0.0256 BSC						
E	0.291	0.307	0.323				
L	0.022	0.030	0.037				
N	See Variations						
∞	0°	4°	8°				
∞	0°	4°	8°				

Ordering Information

ICS9248yF-80-T

Example:

ICS XXXX y F - PPP - T

