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P1 98.2

N-CHANNEL POWER MOS FET ARRAY
SWITCHING TYPE

DESCRIPTION

The μ PA1522 is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
 $I_{D(pulse)} = \pm 8$ A
 $R_{DS(on)} \leq 0.17 \Omega$ TYP. ($V_{GS} = 10$ V)
 $R_{DS(on)} \leq 0.29 \Omega$ TYP. ($V_{GS} = 4$ V)
- 2.54 mm Pitch (0.1 inch)

ORDERING INFORMATION

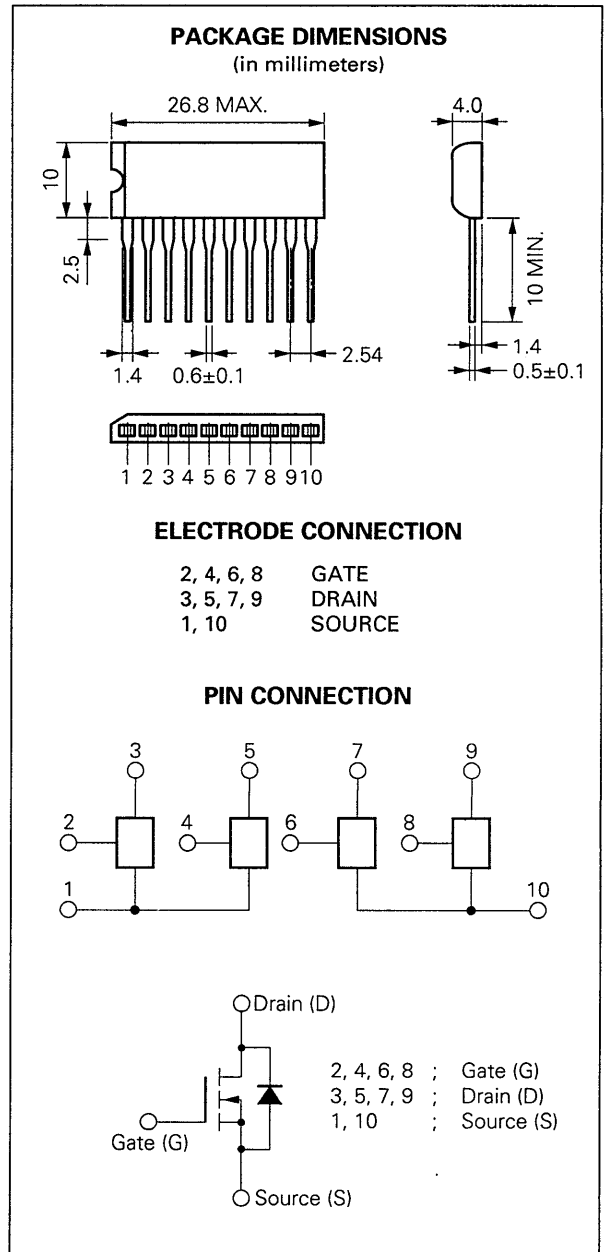
Part Number	Package	Quality Grade
μ PA1522H	10-Pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DS}	60	V
Gate to Source Voltage	$V_{GS(AC)}$	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 2.0	A/unit
Drain Current (pulse)	$I_{D(pulse)*}$	± 8.0	A/unit
Total Power Dissipation (4 circuits) < $T_c = 25^\circ\text{C}$ >	PT_1	28	W
Total Power Dissipation (4 circuits) < $T_a = 25^\circ\text{C}$ >	PT_2	3.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

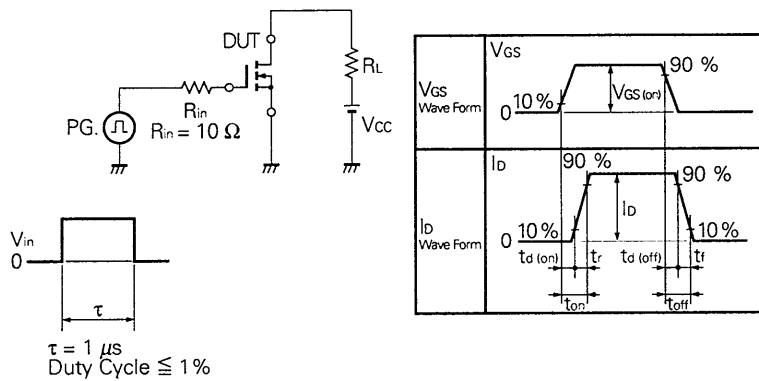
* $PW \leq 10$ ms, Duty Cycle $\leq 1\%$



ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

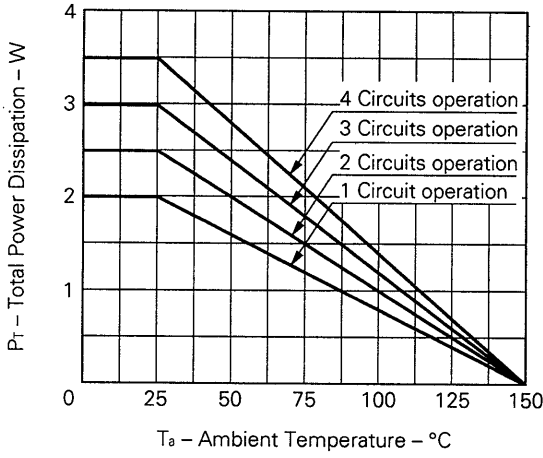
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 60 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±20 V, V _{DS} = 0
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	1.0			S	V _{DS} = 10 V, I _D = 1 A
Drain to Source On-state Resistance	R _{DS(on)1}		0.17	0.25	Ω	V _{GS} = 10 V, I _D = 1 A
Drain to Source On-state Resistance	R _{DS(on)2}		0.29	0.35	Ω	V _{GS} = 4 V, I _D = 0.8 A
Input Capacitance	C _{iss}		550		pF	V _{DS} = 10 V V _{GS} = 0 f = 1.0 MHz
Output Capacitance	C _{oss}		200		pF	
Reverse Transfer Capacitance	C _{rss}		60		pF	
Turn-On Delay Time	t _{d(on)}		10		ns	I _D = 1 A V _{GS} = 10 V V _{CC} = 50 V R _L = 50 Ω, R _{in} = 10 Ω See Fig. 1
Rise Time	t _r		20		ns	
Turn-Off Delay Time	t _{d(off)}		80		ns	
Fall Time	t _f		20		ns	

Fig. 1 Switching Test Circuit

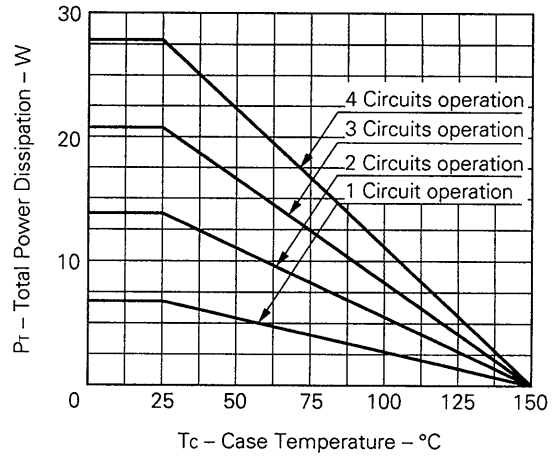


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

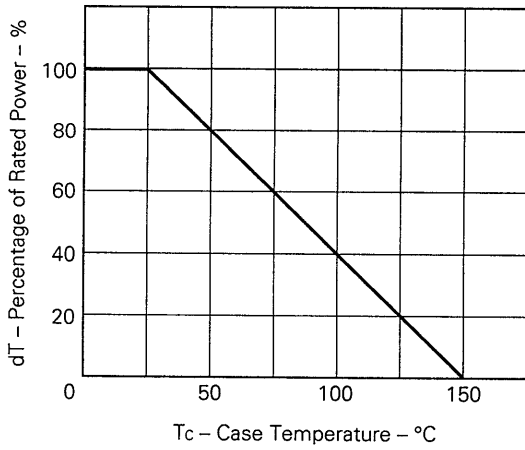
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



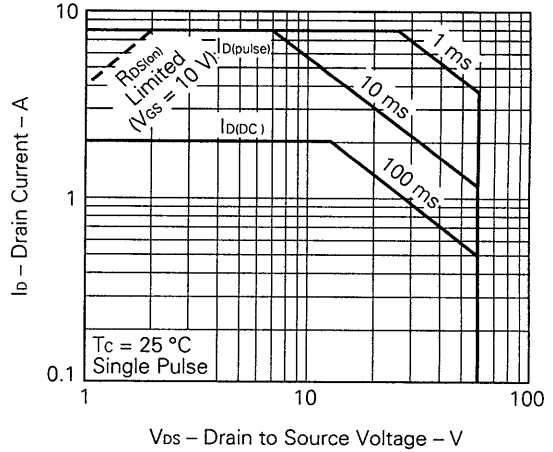
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



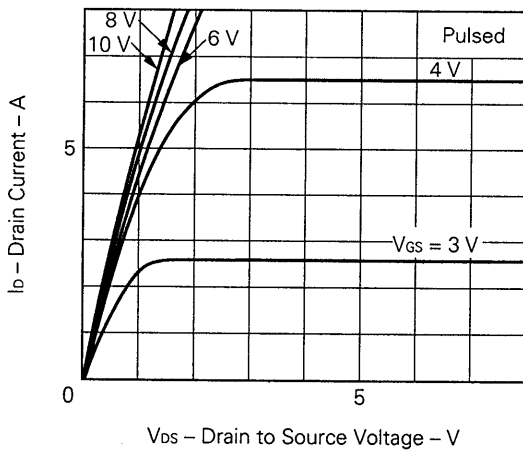
DERATING CURVE OF SAFE OPERATING AREA



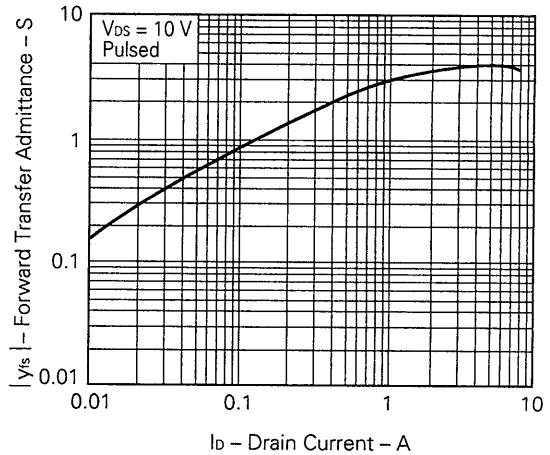
FORWARD BIAS SAFE OPERATING AREA



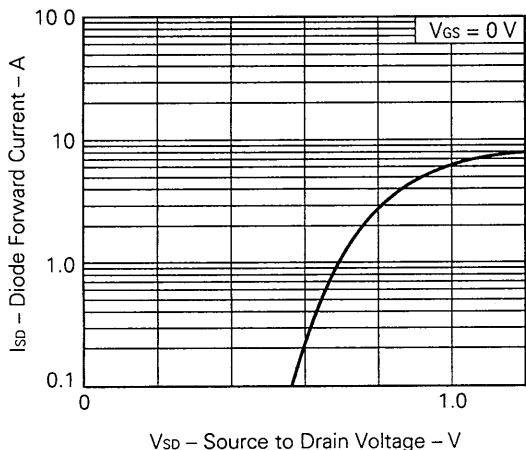
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



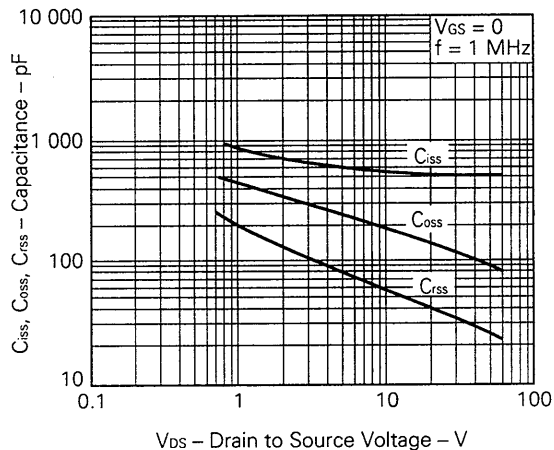
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



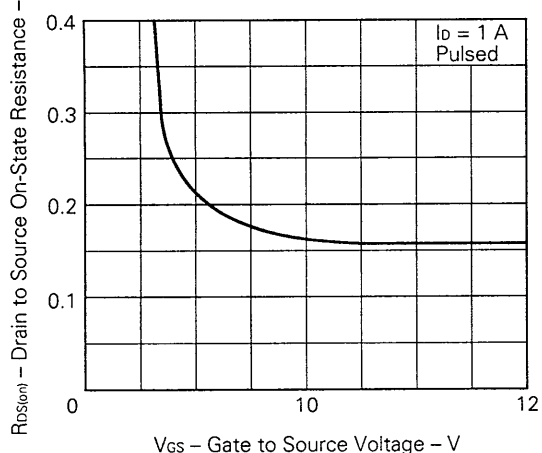
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



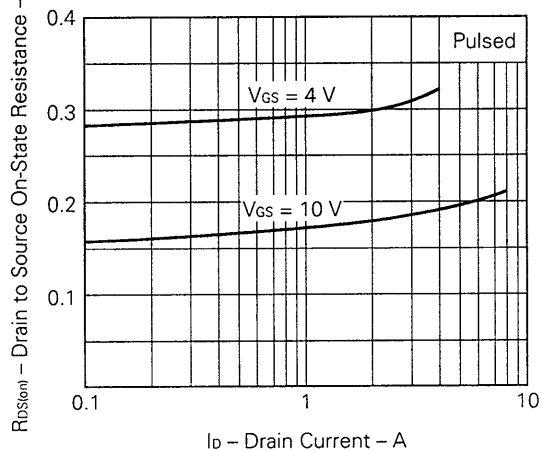
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



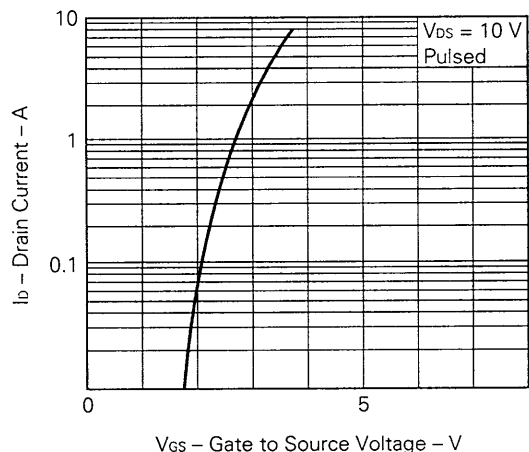
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



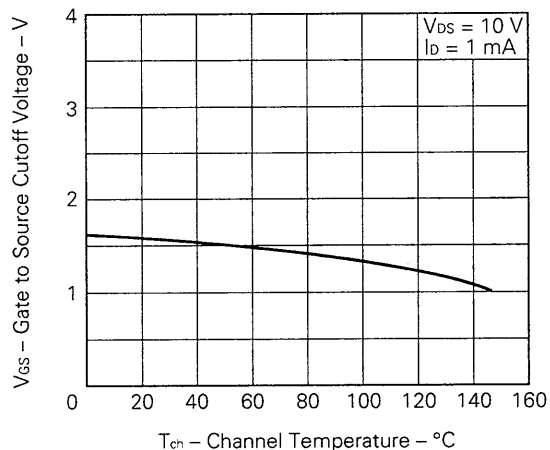
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

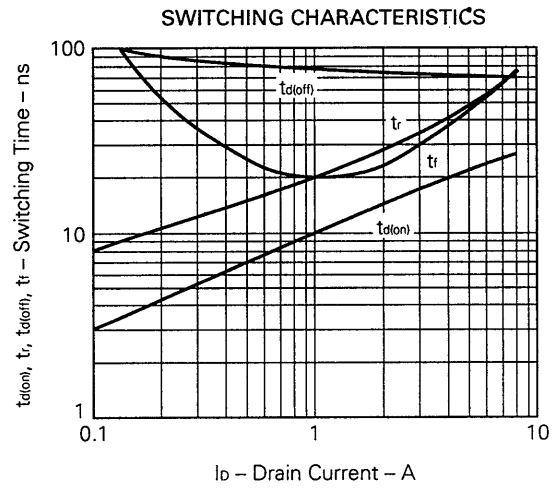
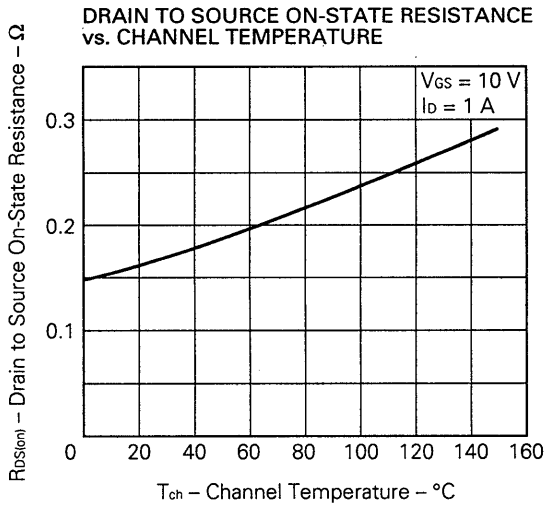


TYPICAL TRANSFER CHARACTERISTICS



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Application circuit using Power MOS FET	TEB-1035

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