

N-CHANNEL POWER MOS FET ARRAY  
SWITCHING USE

DESCRIPTION

The  $\mu$ PA1500B is N-channel Power MOS FET Array that built in 4 circuits and surge absorber designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance  
 $I_{D(DC)} = \pm 3$  A  
 $R_{DS(on)1} \leq 0.18 \Omega$  MAX. ( $V_{GS} = 10$  V,  $I_D = 2$  A)  
 $R_{DS(on)2} \leq 0.24 \Omega$  MAX. ( $V_{GS} = 4$  V,  $I_D = 2$  A)
- Low Input Capacitance  $C_{iss} = 200$  pF TYP.
- Surge Absorber, built in

ORDERING INFORMATION

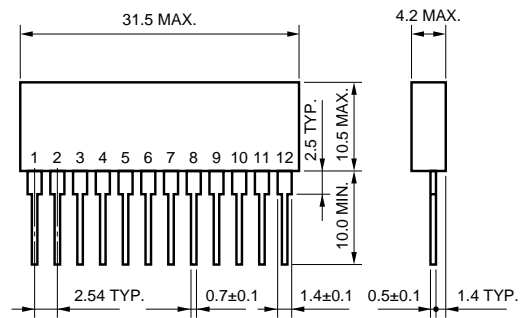
Type Number	Package
$\mu$ PA1500BH	12 Pin SIP

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ )

Drain to Source Voltage	$V_{DSS}$ <b>Note 1</b>	60	V
Gate to Source Voltage	$V_{GSS}$ <b>Note 2</b>	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 3.0$	A/unit
Drain Current (pulse)	$I_{D(pulse)}$ <b>Note 3</b>	$\pm 12$	A/unit
Repetitive peak Reverse Voltage	$V_{RRM}$ <b>Note 4</b>	65	V
Diode Forward Current	$I_{F(av)}$ <b>Note 4</b>	3.0	A/unit
Total Power Dissipation	$P_{T1}$ <b>Note 5</b>	28	W
Total Power Dissipation	$P_{T2}$ <b>Note 6</b>	4.0	W
Channel Temperature	$T_{CH}$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55 to 150	$^\circ C$
Single Avalanche Current	$I_{AS}$ <b>Note 7</b>	3.0	A
Single Avalanche Energy	$E_{AS}$ <b>Note 7</b>	0.9	mJ

- Notes**
1.  $V_{GS} = 0$
  2.  $V_{DS} = 0$
  3.  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$
  4. Rating of Surge Absorber
  5. 4 Circuits,  $T_C = 25^\circ C$
  6. 4 Circuits,  $T_A = 25^\circ C$
  7. Starting  $T_{CH} = 25^\circ C$ ,  $V_{DD} = 30$  V,  $V_{GS} = 20$  V  $\rightarrow$  0,  $R_G = 25 \Omega$ ,  $L = 100 \mu H$

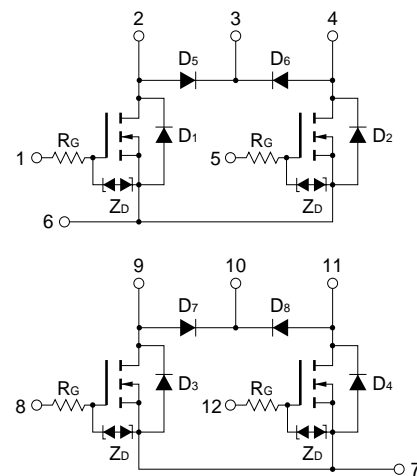
PACKAGE DIMENSIONS  
(in millimeters)



ELECTRODE CONNECTION

- 1, 5, 8, 12 GATE
- 2, 4, 9, 11 DRAIN, ANODE
- 6, 7 SOURCE
- 3, 10 CATHODE

CONNECTION DIAGRAM



- D1 to D4 : Body Diode
- D5 to D8 : Surge Absorber
- Zb : Gate to Source Protection Diode
- Rg : Gate Input Resistance 330  $\Omega$  TYP.

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

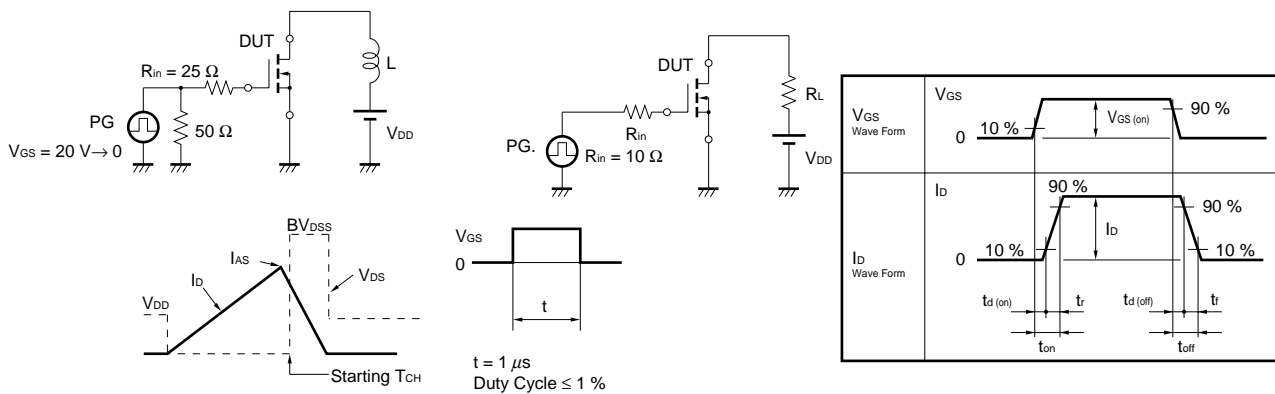
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μA
Gate Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 mA	1.0		2.0	V
Forward Transfer Admittance	Y <sub>fs</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A	2.0			S
Drain to Source On-State Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A		0.10	0.18	Ω
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 2.0 A		0.14	0.24	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1.0 MHz		200		pF
Output Capacitance	C <sub>oss</sub>			150		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			55		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 2.0 A, V <sub>GS</sub> = 10 V, V <sub>DD</sub> ≐ 30 V, R <sub>L</sub> = 15 Ω		20		ns
Rise Time	t <sub>r</sub>			100		ns
Turn-off Delay Time	t <sub>d(off)</sub>			735		ns
Fall Time	t <sub>f</sub>			350		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.0 A, V <sub>DD</sub> = 48 V		13		nC
Gate to Source Charge	Q <sub>GS</sub>			2		nC
Gate to Drain Charge	Q <sub>GD</sub>			4.7		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0		1.0		V

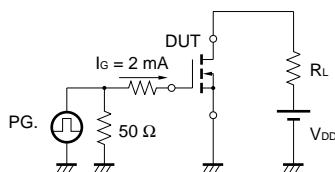
**SURGE ABSORBER (Diode, builtin) 1 Unit**

Repetitive peak Reverse Current	I <sub>RRM</sub>	V <sub>R</sub> = 65 V			10	μA
Diode Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 3.0 A			1.5	V

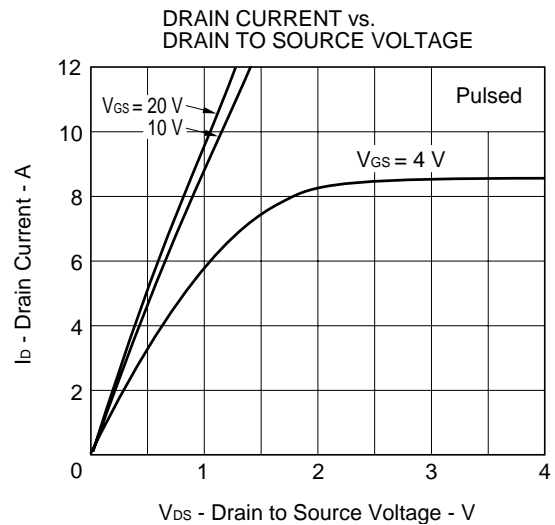
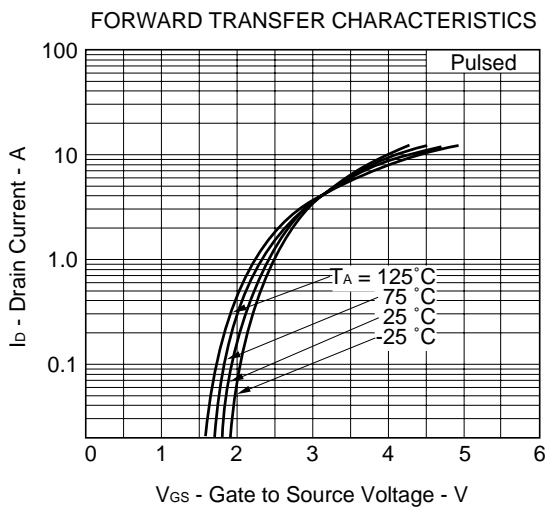
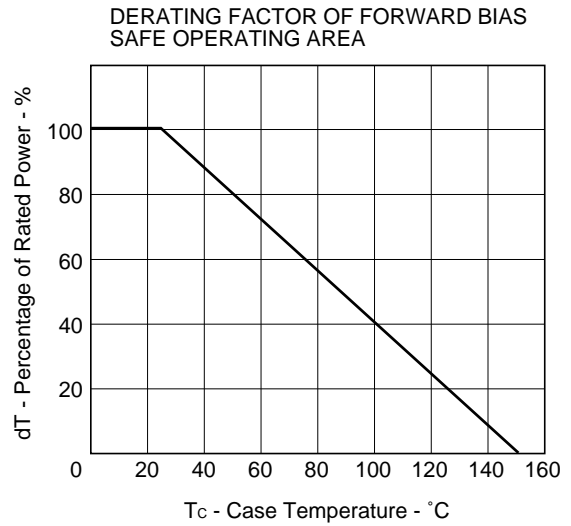
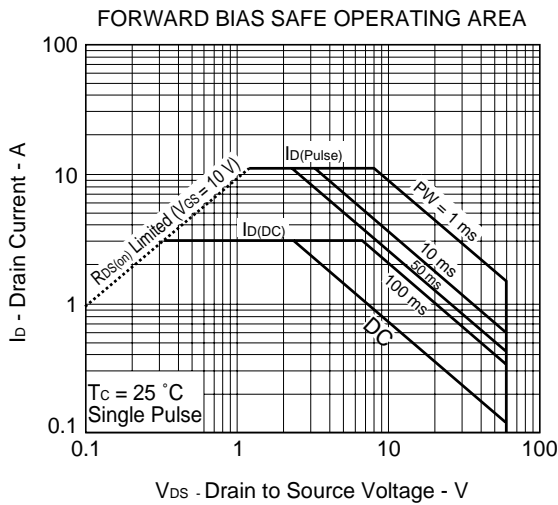
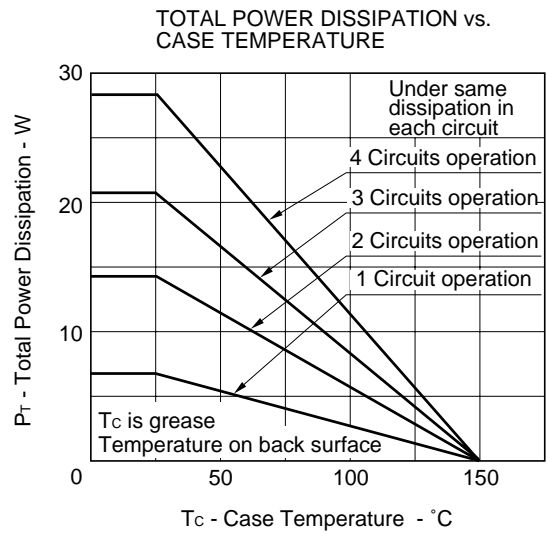
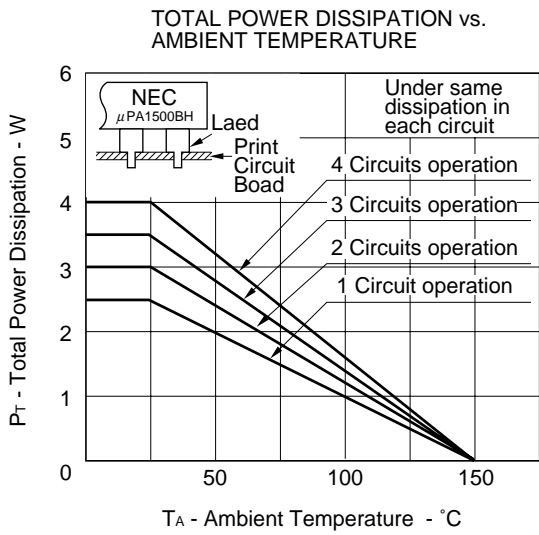
**Test Circuit 1 Avalanche Capability    Test Circuit 2 Switching Time**



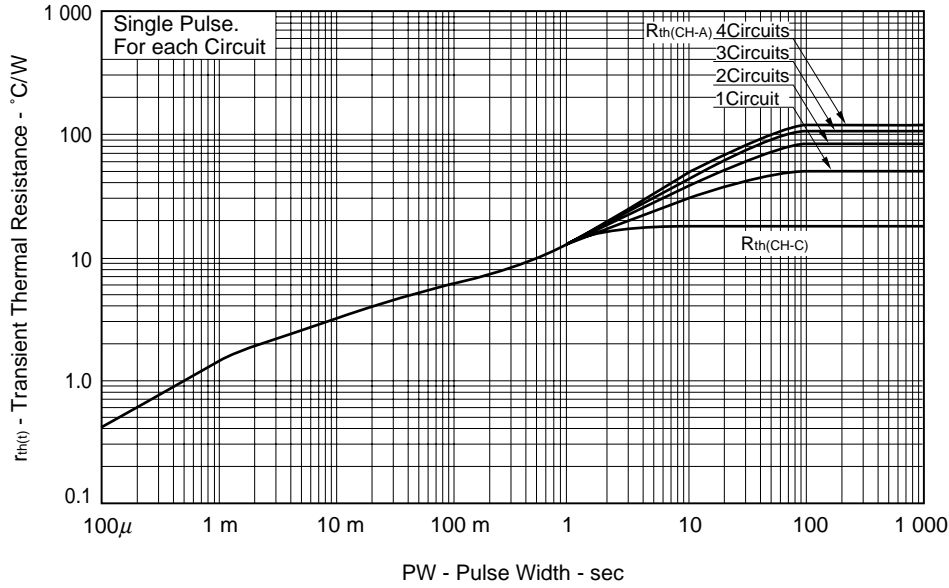
**Test Circuit 3 Gate Charge**



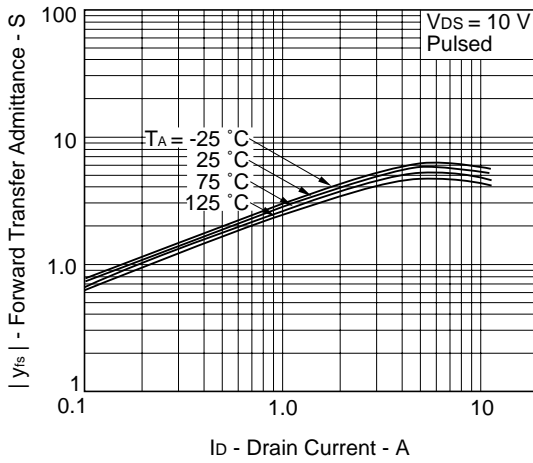
TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



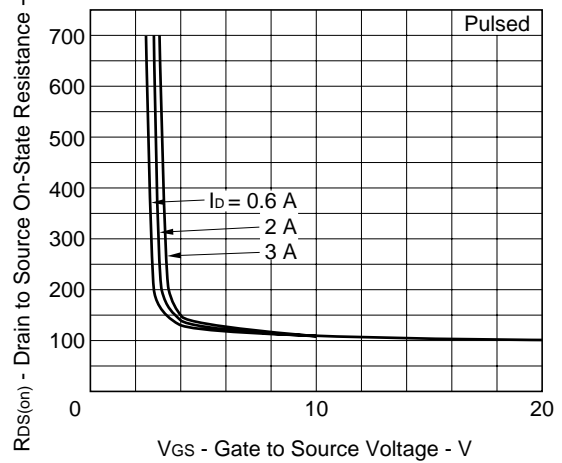
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



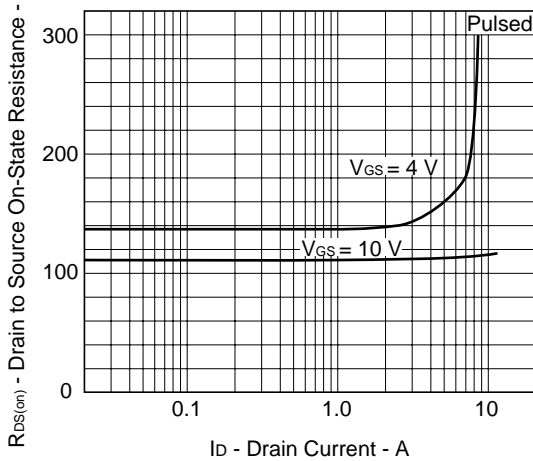
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



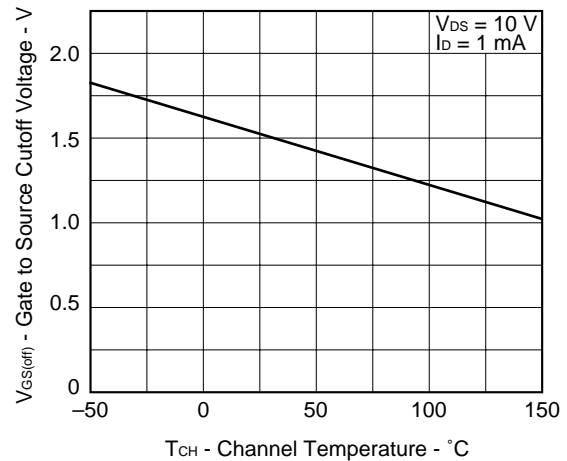
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

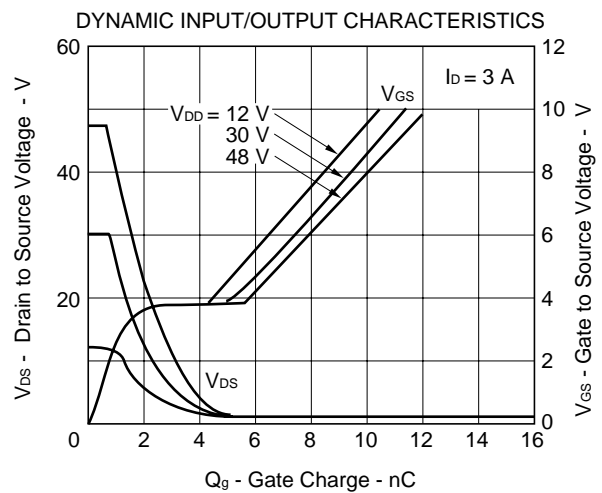
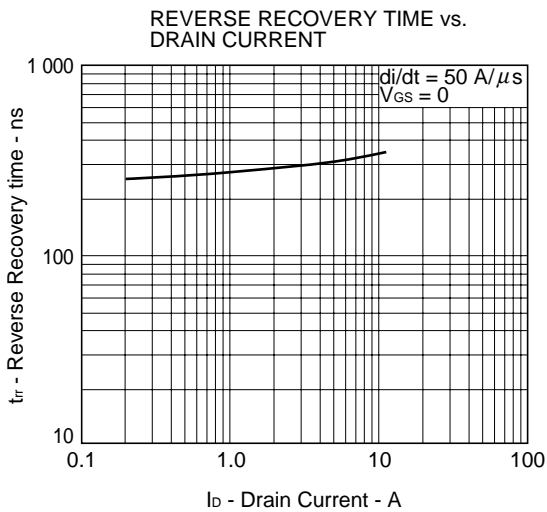
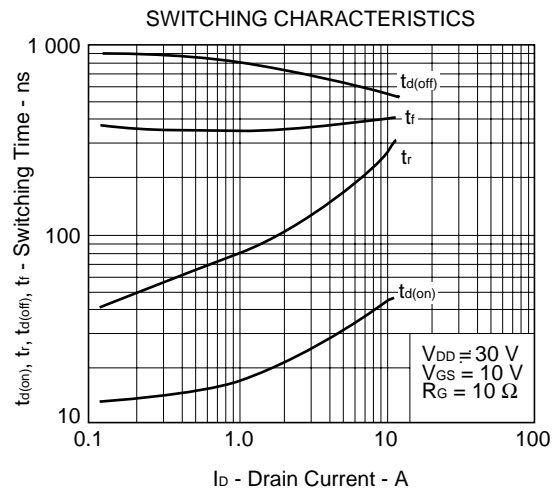
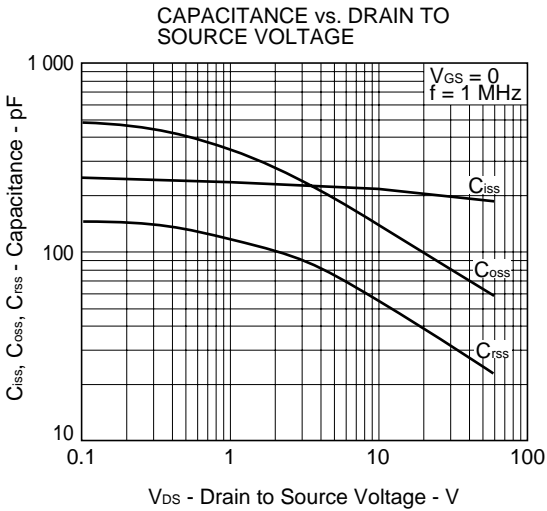
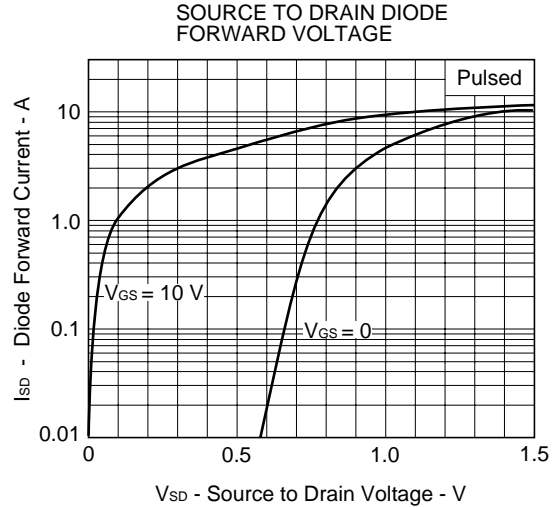
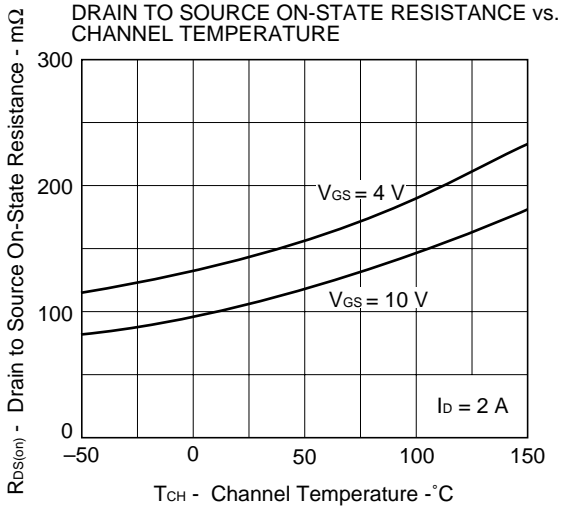


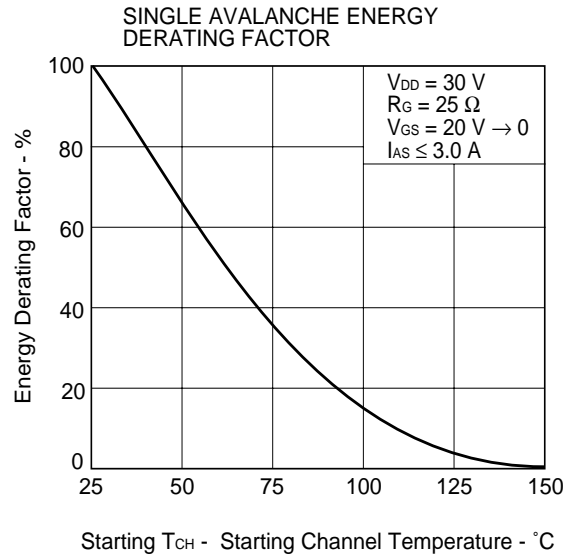
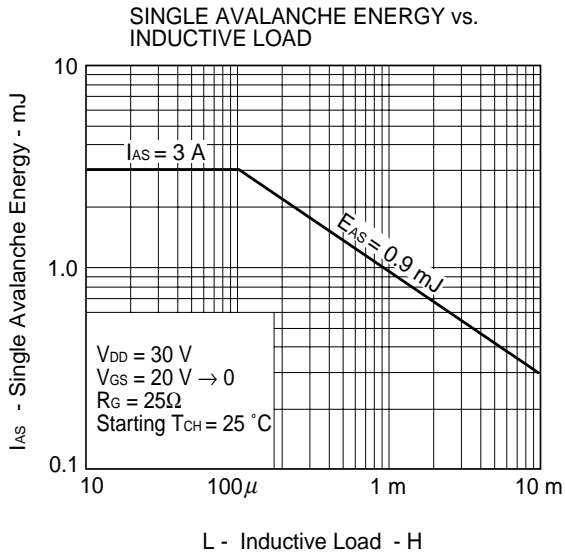
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	IEI-1207
Semiconductor device package manual	IEI-1213
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	MF-1134
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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