



# ESDA6V1W5

Application Specific Discretes  
A.S.D.<sup>TM</sup>

## QUAL TRANSIL<sup>TM</sup> ARRAY FOR ESD PROTECTION

### MAIN APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems
- GSM handsets and accessories
- Other telephone sets
- Set top boxes

### FEATURES

- 4 unidirectional TRANSIL<sup>TM</sup> functions.
- Breakdown voltage :  $V_{BR} = 6.1 \text{ V min.}$
- Low leakage current :  $< 1 \mu\text{A.}$
- Very low PCB space consuming :  $4.2 \text{ mm}^2$  typically.

### DESCRIPTION

The ESDA6V1W5 is a 4-bit wide monolithic suppressor which is designed to protect component connected to data and transmission lines against ESD.

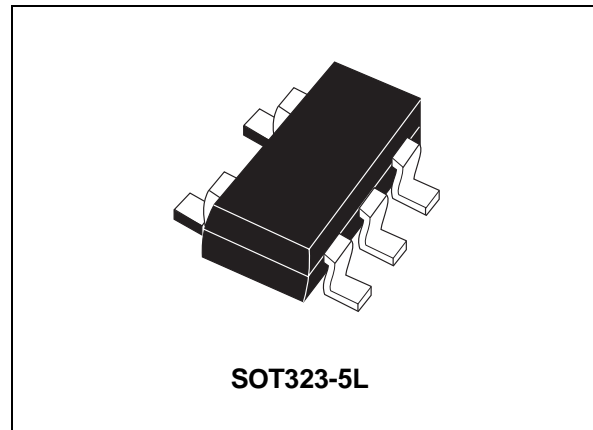
It clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients.

### BENEFITS

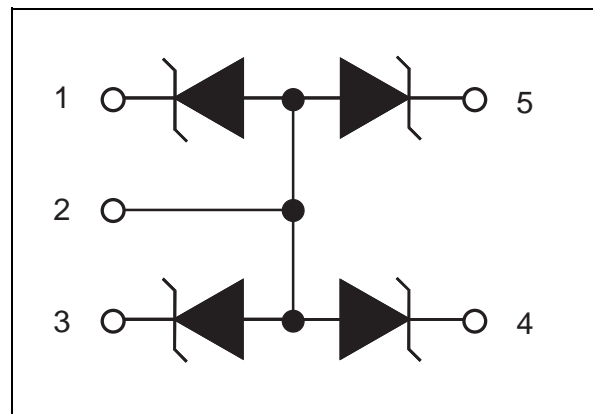
- High ESD protection level : up to 25 kV.
- High integration.
- Suitable for high density boards.

### COMPLIES WITH THE FOLLOWING STANDARDS :

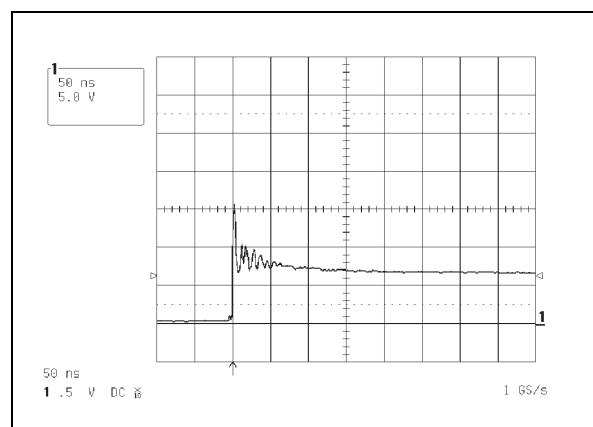
- IEC 1000-4-2 level 4
- MIL STD 883C-Method 3015-6 : class 3.  
(human body model)



### FUNCTIONAL DIAGRAM



### ESD RESPONSE TO IEC1000-4-2 (air discharge 16 kV, positive surge)



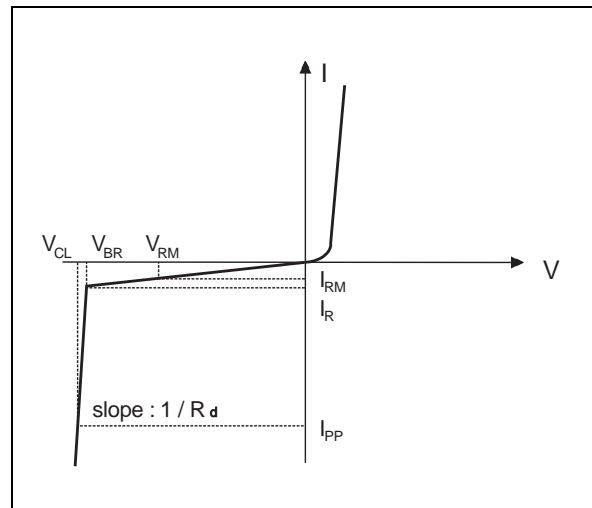
## ESDA6V1W5

### ABSOLUTE MAXIMUM RATINGS ( $T_{amb} = 25^{\circ}\text{C}$ )

| Symbol    | Parameter                                      | Test conditions  | Value         | Unit               |
|-----------|--|--|---------------|--------------------|
| $V_{PP}$  | ESD discharge                                  | MIL STD 883C - Method 3015-6<br>IEC1000-4-2, air discharge<br>IEC1000-4-2, contact discharge | 25<br>16<br>9 | kV                 |
| $P_{PP}$  | Peak pulse power (8/20 $\mu\text{s}$ )         |  | 150           | W                  |
| $T_{op}$  | Operating temperature range                    |  | - 40 to + 85  | $^{\circ}\text{C}$ |
| $T_j$     | Junction temperature                           |  | 150           | $^{\circ}\text{C}$ |
| $T_{stg}$ | Storage temperature range                      |  | - 55 to + 150 | $^{\circ}\text{C}$ |
| $T_L$     | Lead solder temperature (10 secondes duration) |  | 260           | $^{\circ}\text{C}$ |

### ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^{\circ}\text{C}$ )

| Symbol     | Parameter                       |
|------------|---------------------------------|
| $V_{RM}$   | Stand-off voltage               |
| $V_{BR}$   | Breakdown voltage               |
| $V_{CL}$   | Clamping voltage                |
| $I_{RM}$   | Leakage current                 |
| $I_{PP}$   | Peak pulse current              |
| $\alpha T$ | Voltage temperature coefficient |
| C          | Capacitance per line            |
| $R_d$      | Dynamic resistance              |
| $V_F$      | Forward voltage drop            |



| Types     | $V_{BR}$ @ |      | $I_R$ | $I_{RM}$ @ $V_{RM}$ |   | $R_d$<br>typ.<br>note 1 | $\alpha T$<br>max.<br>note 2 | C<br>typ.<br>0V bias | $V_F$ @ $I_F$ |     |
|-----------|------------|------|-------|---------------------|---|-------------------------|------------------------------|----------------------|---------------|-----|
|           | min.       | max. |       | max.                |   |                         |                              |                      | max.          |     |
|           | V          | V    | mA    | $\mu\text{A}$       | V | $\text{m}\Omega$        | $10^{-4}/^{\circ}\text{C}$   | pF                   | V             | mA  |
| ESDA6V1W5 | 6.1        | 7.2  | 1     | 1                   | 3 | 350                     | 6                            | 90                   | 1.25          | 200 |

note 1 : Square pulse  $I_{pp} = 15\text{A}$ ,  $t_p = 2.5\mu\text{s}$ .

note 2 :  $\Delta V_{BR} = \alpha T * (T_{amb} - 25^{\circ}\text{C}) * V_{BR}(25^{\circ}\text{C})$

## CALCULATION OF THE CLAMPING VOLTAGE

### USE OF THE DYNAMIC RESISTANCE

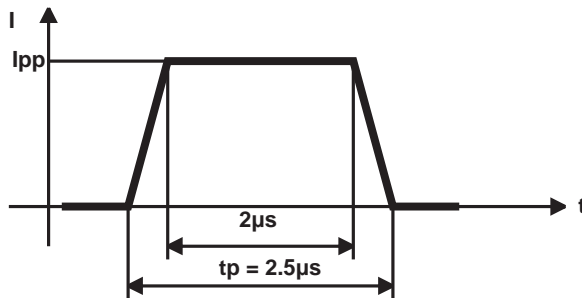
The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage  $V_{CL}$ . This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

$$V_{CL} = V_{BR} + R_d I_{PP}$$

Where  $I_{PP}$  is the peak current through the ESDA cell.

### DYNAMIC RESISTANCE MEASUREMENT

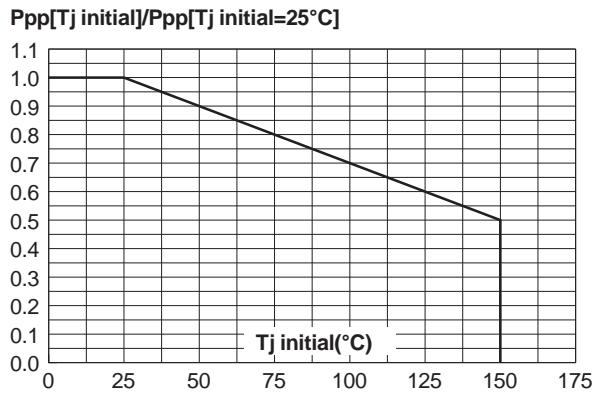
The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20 $\mu$ s and 10/1000 $\mu$ s surges.



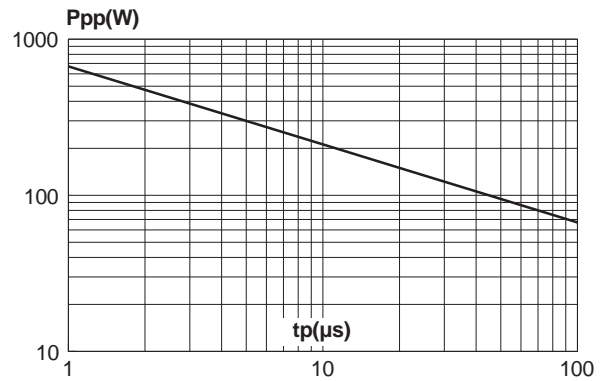
2.5 $\mu$ s duration measurement wave.

As the value of the dynamic resistance remains stable for a surge duration lower than 20 $\mu$ s, the 2.5 $\mu$ s rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of  $R_d$ .

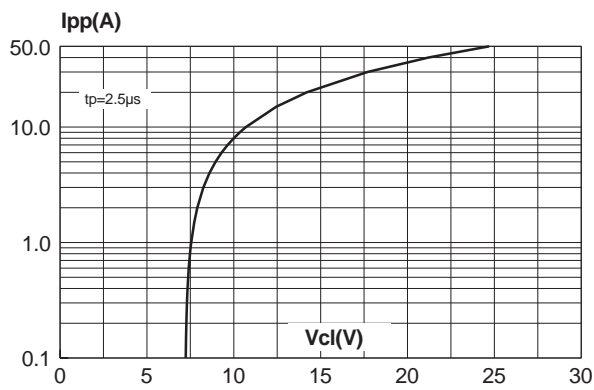
**Fig. 1 :** Peak power dissipation versus initial junction temperature



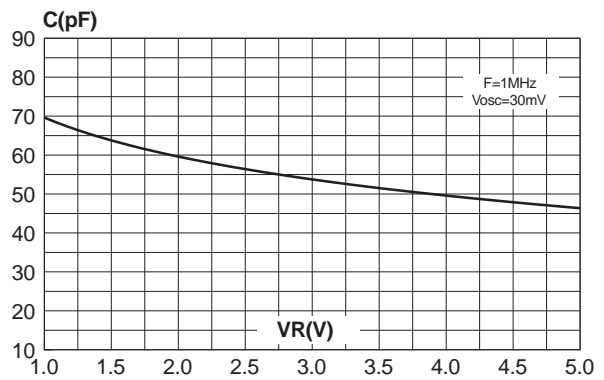
**Fig. 2 :** Peak pulse power versus exponential pulse duration (Tj initial = 25 °C)



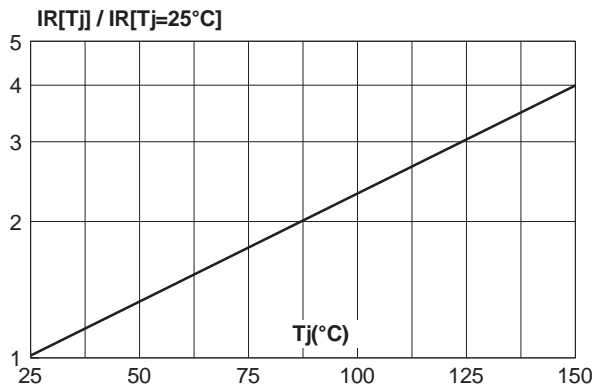
**Fig. 3 :** Clamping voltage versus peak pulse current (Tj initial = 25 °C). Rectangular waveform tp = 2.5 μs.



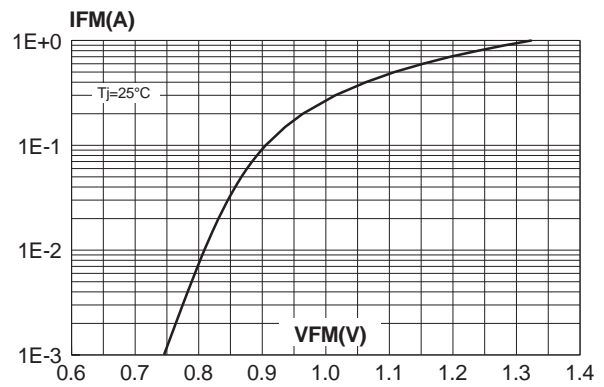
**Fig. 4 :** Capacitance versus reverse applied voltage (typical values).



**Fig. 5 :** Relative variation of leakage current versus junction temperature (typical values).



**Fig. 6 :** Peak forward voltage drop versus peak forward current (typical values).



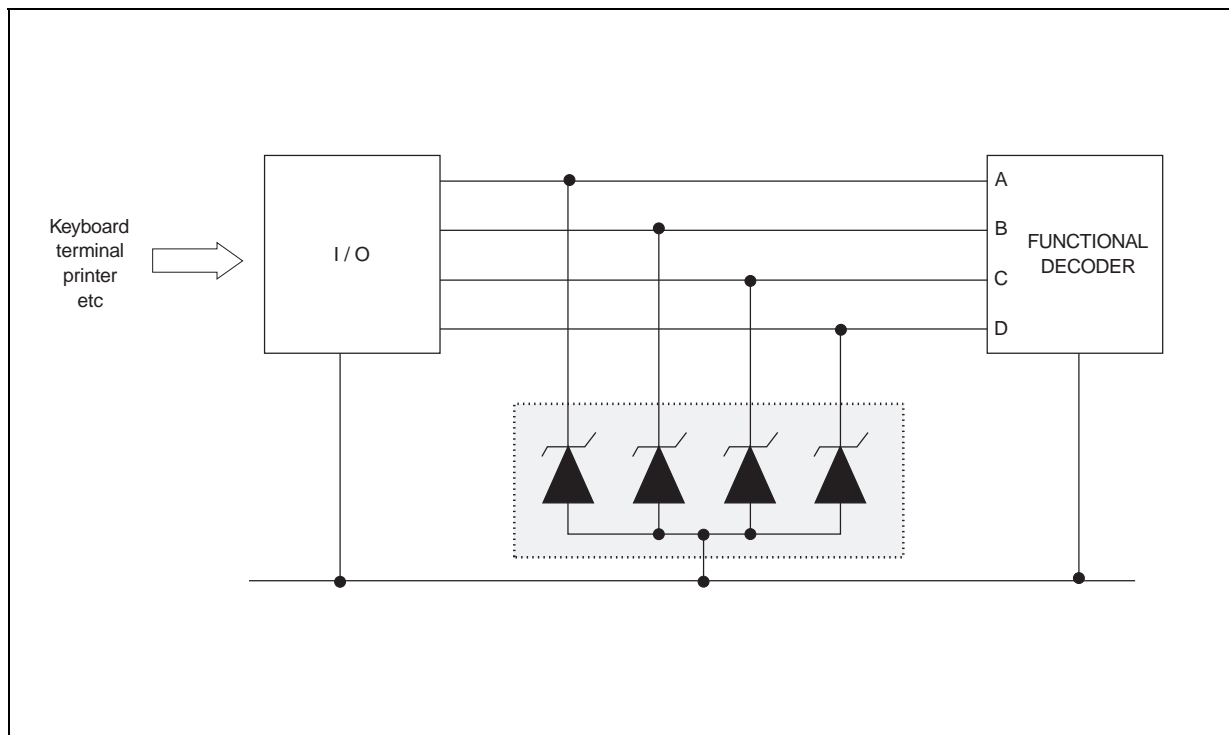
## 1. ESD protection by the ESDA6V1W5

With the focus of lowering the operation levels, the problem of malfunction caused by the environment is critical. Electrostatic discharge (ESD) is a major cause of failure in electronic system.

Transient Voltage Suppressors are an ideal choice for ESD protection and have proven capable in suppressing ESD events. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented.

Surface mount TVS arrays offer the best choice for minimal lead inductance.

They serve as parallel protection elements, connected between the signal line to ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground.



The ESDA6V1W5 array is the ideal product for use as board level protection of ESD sensitive semiconductor components.

The tiny SOT323-5L package makes the ESDA6V1W5 device some of the smallest ESD protection devices available. It also allows design flexibility in the design of "crowded" boards where the space saving is at a premium. This enables to shorten the routing and can contribute to improved ESD performance.

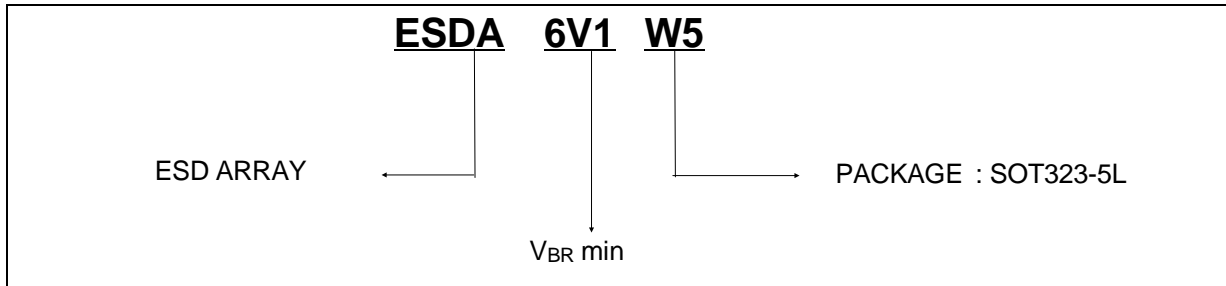
## 2. Circuit Board Layout

Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended :

- The ESDA6V1W5 should be placed as near as possible to the input terminals or connectors.
- Minimise the path length between the ESD suppressor and the protected device
- Minimise all conductive loops, including power and ground loops
- The ESD transient return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

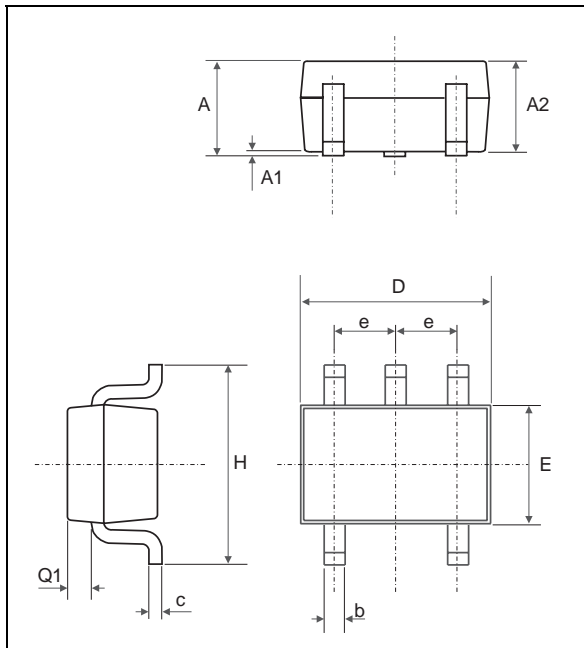
# ESDA6V1W5

## ORDER CODE



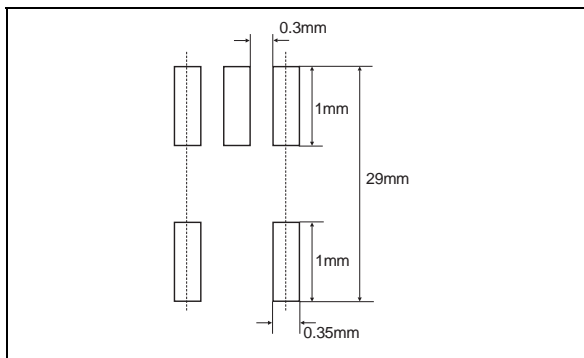
| Ordering type | Marking | Package   | Weight  | Base qty | Delivery mode |
|---------------|---------|-----------|---------|----------|---------------|
| ESDA6V1W5     | E61     | SOT323-5L | 5.4 mg. | 3000     | Tape & reel   |

## PACKAGE MECHANICAL DATA SOT323-5L



| REF. | DIMENSIONS  |      |            |       |
|------|-------------|------|------------|-------|
|      | Millimeters |      | Inches     |       |
|      | Min.        | Max. | Min.       | Max.  |
| A    | 0.8         | 1.1  | 0.031      | 0.043 |
| A1   | 0           | 0.1  | 0          | 0.004 |
| A2   | 0.8         | 1    | 0.031      | 0.039 |
| b    | 0.15        | 0.3  | 0.006      | 0.012 |
| c    | 0.1         | 0.18 | 0.004      | 0.007 |
| D    | 1.8         | 2.2  | 0.071      | 0.086 |
| E    | 1.15        | 1.35 | 0.045      | 0.053 |
| e    | 0.65 Typ.   |      | 0.026 Typ. |       |
| H    | 1.8         | 2.4  | 0.071      | 0.094 |
| Q1   | 0.1         | 0.4  | 0.004      | 0.016 |

## FOOT PRINT (in millimeters)



| Mechanical specifications |                            |
|---------------------------|----------------------------|
| Lead plating              | Tin-lead                   |
| Lead plating thickness    | 5µm min.<br>25 µm max.     |
| Lead material             | Sn / Pb<br>(70% to 90% Sn) |
| Lead coplanarity          | 10µm max.                  |
| Body material             | Molded epoxy               |
| Epoxy meets               | UL94,V0                    |

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