# CMOS 300 MHz Complete-DDS

# AD9852

**FEATURES**

**300 MHz Internal Clock Rate**
**Integrated 12-Bit Output DACs**
**Ultrahigh-Speed, 3 ps RMS Jitter Comparator**
**Excellent Dynamic Performance: 80 dB SFDR @ 100 MHz (±1 MHz) $A_{OUT}$**
**4× to 20× Programmable Reference Clock Multiplier**
**Dual 48-Bit Programmable Frequency Registers**
**Dual 14-Bit Programmable Phase Offset Registers**
**12-Bit Amplitude Modulation and Programmable Shaped On/Off Keying Function**
**Single Pin FSK and PSK Data Interface**
**Linear or Nonlinear FM Chirp Functions with Single Pin Frequency "Hold" Function**
**Frequency-Ramped FSK**
**<25 ps RMS Total Jitter in Clock Generator Mode**
**Automatic Bidirectional Frequency Sweeping**
**SIN(x)/x Correction**
**Simplified Control Interface**
**10 MHz Serial, 2-Wire or 3-Wire SPI-Compatible or 100 MHz Parallel 8-Bit Programming**
**3.3 V Single Supply**
**Multiple Power-Down Functions**
**Single-Ended or Differential Input Reference Clock**
**Small 80-Lead LQFP Packaging**

**APPLICATIONS**

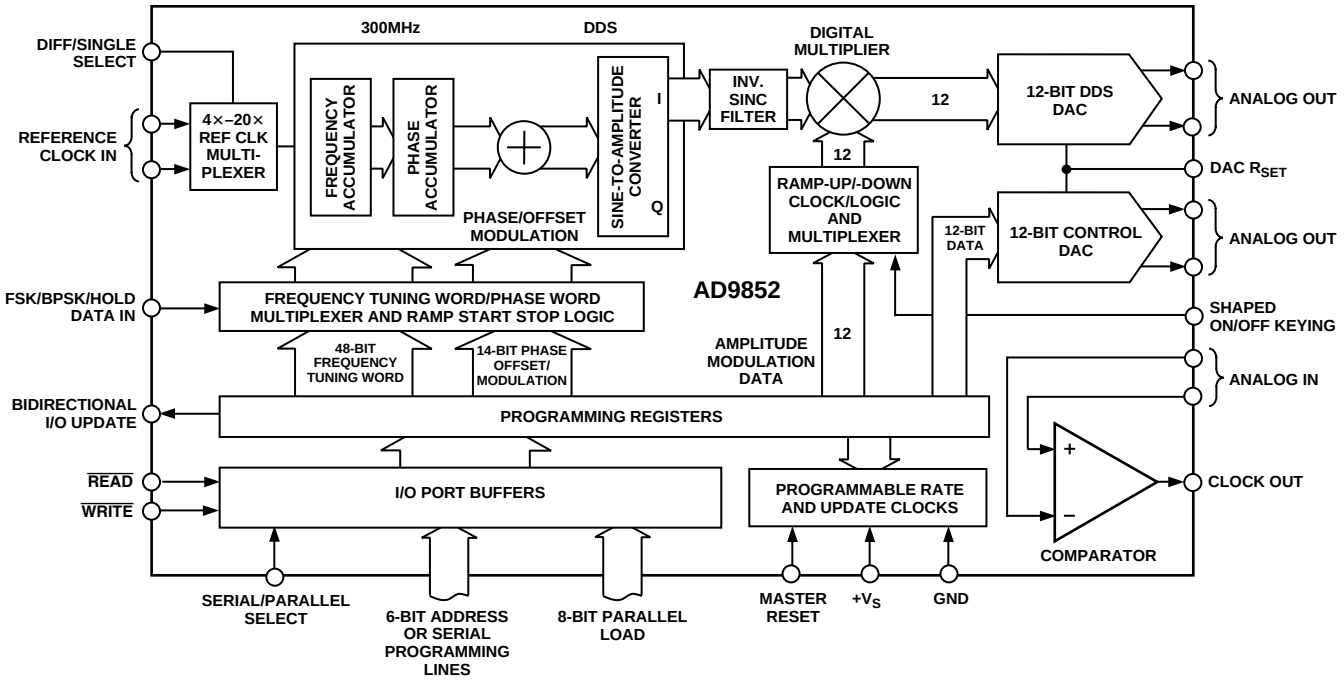
**Agile, L.O. Frequency Synthesis**
**Programmable Clock Generator**
**FM Chirp Source for Radar and Scanning Systems**
**Test and Measurement Equipment**
**Commercial and Amateur RF Exciter**

**GENERAL DESCRIPTION**

The AD9852 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with an internal high-speed, high-performance D/A converters and a comparator to form a digitally-programmable agile synthesizer function. When referenced to an accurate clock source, the AD9852 generates a highly stable, frequency-phase amplitude-programmable sine wave output that can be used as an agile L.O. in communications, radar, and many other applications. The AD9852's innovative high-speed DDS core provides 48-bit frequency resolution (1 microHertz tuning steps). Phase truncation to 17 bits assures excellent SFDR. The AD9852's circuit architecture allows the

(*continued on page 13*)

**FUNCTIONAL BLOCK DIAGRAM**




REV. 0



**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781/329-4700 World Wide Web Site: http://www.analog.com**
**Fax: 781/326-8703**

# AD9852–SPECIFICATIONS ($V_S$ = 3.3 V ± 5%, $R_{SET}$ = 3.9 kΩ external reference clock frequency = 30 MHz with REFCLK Multiplier enabled at 10× for AD9852ASQ, external reference clock frequency = 20 MHz with REFCLK Multiplier enabled at 10× for AD9852AST, unless otherwise noted.)

| Parameter | Temp | Test Level | AD9852ASQ Min | AD9852ASQ Typ | AD9852ASQ Max | AD9852AST Min | AD9852AST Typ | AD9852AST Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| REF CLOCK INPUT CHARACTERISTICS[1] | | | | | | | | | |
| Internal Clock Frequency Range | FULL | VI | 5 | | 300 | 5 | | 200 | MHz |
| External REF Clock Frequency Range | | | | | | | | | |
| REFCLK Multiplier Enabled | FULL | VI | 5 | | 75 | 5 | | 50 | MHz |
| REFCLK Multiplier Disabled | FULL | VI | 5 | | 300 | 5 | | 200 | MHz |
| Duty Cycle | 25°C | V | | 50 | | | 50 | | % |
| Input Capacitance | 25°C | IV | | 3 | | | 3 | | pF |
| Input Impedance | 25°C | IV | | 100 | | | 100 | | kΩ |
| Differential Mode Common-Mode Voltage Range | | | | | | | | | |
| Minimum Signal Amplitude | 25°C | IV | 800 | | | 800 | | | mV p-p |
| Common-Mode Range | 25°C | IV | 1.6 | 1.75 | 1.9 | 1.6 | 1.75 | 1.9 | V |
| $V_{IH}$ (Single-Ended Mode) | 25°C | IV | 2.3 | | | 2.3 | | | V |
| $V_{IL}$ (Single-Ended Mode) | 25°C | IV | | | 1 | | | 1 | V |
| DAC STATIC OUTPUT CHARACTERISTICS | | | | | | | | | |
| Output Update Speed | FULL | I | | | 300 | | | 200 | MSPS |
| Resolution | 25°C | IV | | 12 | | | 12 | | Bits |
| Sine and Aux. DAC Full-Scale Output Current | 25°C | IV | 5 | 10 | 20 | 5 | 10 | 20 | mA |
| Gain Error | 25°C | I | –6 | | +2.25 | –6 | | +2.25 | % FS |
| Output Offset | 25°C | I | | | 2 | | | 2 | µA |
| Differential Nonlinearity | 25°C | I | | 0.3 | 1.25 | | 0.3 | 1.25 | LSB |
| Integral Nonlinearity | 25°C | I | | 0.6 | 1.66 | | 1 | 1.66 | LSB |
| Output Impedance | 25°C | I | | 100 | | | 100 | | kΩ |
| Voltage Compliance Range | 25°C | I | –0.5 | | +1.0 | –0.5 | | +1.0 | V |
| DAC WIDEBAND SFDR | | | | | | | | | |
| 1 MHz to 20 MHz $A_{OUT}$ | 25°C | V | | 58 | | | 58 | | dBc |
| 20 MHz to 40 MHz $A_{OUT}$ | 25°C | V | | 56 | | | 56 | | dBc |
| 40 MHz to 60 MHz $A_{OUT}$ | 25°C | V | | 52 | | | 52 | | dBc |
| 60 MHz to 80 MHz $A_{OUT}$ | 25°C | V | | 48 | | | 48 | | dBc |
| 80 MHz to 100 MHz $A_{OUT}$ | 25°C | V | | 48 | | | 48 | | dBc |
| 100 MHz to 120 MHz $A_{OUT}$ | 25°C | V | | 50 | | | | | dBc |
| DAC NARROWBAND SFDR | | | | | | | | | |
| 10 MHz $A_{OUT}$ (±1 MHz) | 25°C | V | | 83 | | | 83 | | dBc |
| 10 MHz $A_{OUT}$ (±250 kHz) | 25°C | V | | 83 | | | 83 | | dBc |
| 10 MHz $A_{OUT}$ (±50 kHz) | 25°C | V | | 91 | | | 91 | | dBc |
| 41 MHz $A_{OUT}$ (±1 MHz) | 25°C | V | | 82 | | | 82 | | dBc |
| 41 MHz $A_{OUT}$ (±250 kHz) | 25°C | V | | 84 | | | 84 | | dBc |
| 41 MHz $A_{OUT}$ (±50 kHz) | 25°C | V | | 89 | | | 89 | | dBc |
| 119 MHz $A_{OUT}$ (±1 MHz) | 25°C | V | | 71 | | | 71 | | dBc |
| 119 MHz $A_{OUT}$ (±250 kHz) | 25°C | V | | 77 | | | 77 | | dBc |
| 119 MHz $A_{OUT}$ (±50 kHz) | 25°C | V | | 83 | | | 83 | | dBc |
| RESIDUAL PHASE NOISE | | | | | | | | | |
| ($A_{OUT}$ = 5 MHz, Ext. CLK = 30 MHz, | | | | | | | | | |
| REFCLK Multiplier Engaged at 10×) | | | | | | | | | |
| 1 kHz Offset | 25°C | V | | 140 | | | 140 | | dBc/Hz |
| 10 kHz Offset | 25°C | V | | 138 | | | 138 | | dBc/Hz |
| 100 kHz Offset | 25°C | V | | 142 | | | 142 | | dBc/Hz |
| ($A_{OUT}$ = 5 MHz, Ext. CLK = 300 MHz, | | | | | | | | | |
| REFCLK Multiplier Bypassed) | | | | | | | | | |
| 1 kHz Offset | 25°C | V | | 142 | | | 142 | | dBc/Hz |
| 10 kHz Offset | 25°C | V | | 148 | | | 148 | | dBc/Hz |
| 100 kHz Offset | 25°C | V | | 152 | | | 152 | | dBc/Hz |
| PIPELINE DELAYS | | | | | | | | | |
| Phase Accumulator and DDS Core | 25°C | IV | | 17 | | | 17 | | SysClk Cycles |
| Inverse Sinc Filter | 25°C | IV | | 12 | | | 12 | | SysClk Cycles |
| Digital Multiplier | 25°C | IV | | 10 | | | 10 | | SysClk Cycles |

| Parameter | Temp | Test Level | AD9852ASQ Min | AD9852ASQ Typ | AD9852ASQ Max | AD9852AST Min | AD9852AST Typ | AD9852AST Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| MASTER RESET DURATION | 25°C | IV | 10 | | | 10 | | | SysClk Cycles |
| COMPARATOR INPUT CHARACTERISTICS | | | | | | | | | |
| Input Capacitance | 25°C | V | | 3 | | | 3 | | pF |
| Input Resistance | 25°C | IV | | 500 | | | 500 | ±1 | kΩ |
| Input Current | 25°C | I | | ±1 | ±5 | | ±1 | ±5 | µA |
| Hysteresis | 25°C | IV | | 10 | 20 | | 10 | 20 | mV p-p |
| COMPARATOR OUTPUT CHARACTERISTICS | | | | | | | | | |
| Logic "1" Voltage, High Z Load | FULL | VI | 3.10 | | | 3.10 | | | V |
| Logic "0" Voltage, High Z Load | FULL | VI | | | 0.16 | | | 0.16 | V |
| Output Power, 50 Ω Load, 120 MHz Toggle Rate | 25°C | I | 9 | 11 | | 9 | 11 | | dBm |
| Propagation Delay | 25°C | IV | | 3 | | | 3 | | ns |
| Output Duty Cycle Error[2] | 25°C | I | –10 | ±1 | +10 | –10 | ±1 | +10 | % |
| Rise/Fall Time, 5 pF Load | 25°C | V | | 2 | | | 2 | | ns |
| Toggle Rate, High Z Load | 25°C | IV | 300 | 350 | | 300 | 350 | | MHz |
| Toggle Rate, 50 Ω Load | 25°C | IV | 375 | 400 | | 375 | 400 | | MHz |
| Output Cycle-to-Cycle Jitter[3] | 25°C | IV | | | 3 | | | 3 | ps rms |
| COMPARATOR NARROWBAND SFDR[4] | | | | | | | | | |
| 10 MHz (±1 MHz) | 25°C | V | | 84 | | | 84 | | dBc |
| 10 MHz (±250 kHz) | 25°C | V | | 84 | | | 84 | | dBc |
| 10 MHz (±50 kHz) | 25°C | V | | 92 | | | 92 | | dBc |
| 41 MHz (±1 MHz) | 25°C | V | | 76 | | | 76 | | dBc |
| 41 MHz (±250 kHz) | 25°C | V | | 82 | | | 82 | | dBc |
| 41 MHz (±50 kHz) | 25°C | V | | 89 | | | 89 | | dBc |
| 119 MHz (±1 MHz) | 25°C | V | | 73 | | | 73 | | dBc |
| 119 MHz (±250 kHz) | 25°C | V | | 73 | | | 73 | | dBc |
| 119 MHz (±50 kHz) | 25°C | V | | 83 | | | 83 | | dBc |
| CLOCK GENERATOR OUTPUT JITTER[4] | | | | | | | | | |
| 5 MHz $A_{OUT}$ | 25°C | V | | 23 | | | 23 | | ps rms |
| 40 MHz $A_{OUT}$ | 25°C | V | | 12 | | | 12 | | ps rms |
| 100 MHz $A_{OUT}$ | 25°C | V | | 7 | | | 7 | | ps rms |
| PARALLEL I/O TIMING CHARACTERISTICS | | | | | | | | | |
| $T_{ASU}$ (Address Setup Time to $\overline{WR}$ Signal Active) | FULL | IV | 4 | | | 4 | | | ns |
| $T_{ADHW}$ (Address Hold Time to $\overline{WR}$ Signal Inactive) | FULL | IV | 3 | | | 3 | | | ns |
| $T_{DSU}$ (Data Setup Time to $\overline{WR}$ Signal Inactive) | FULL | IV | 2 | | | 2 | | | ns |
| $T_{DHD}$ (Data Hold Time to $\overline{WR}$ Signal Inactive) | FULL | IV | 0 | | | 0 | | | ns |
| $T_{WRLOW}$ ($\overline{WR}$ Signal Minimum Low Time) | FULL | IV | 3 | | | 3 | | | ns |
| $T_{WRHIGH}$ ($\overline{WR}$ Signal Minimum High Time) | FULL | IV | 7 | | | 7 | | | ns |
| $T_{WR}$ ($\overline{WR}$ Signal Minimum Period) | FULL | IV | 10 | | | 10 | | | ns |
| $T_{ADV}$ (Address to Data Valid Time) | FULL | V | 15 | | 15 | 15 | | 15 | ns |
| $T_{ADHR}$ (Address Hold Time to $\overline{RD}$ Signal Inactive) | FULL | IV | 5 | | | 5 | | | ns |
| $T_{RDLOV}$ ($\overline{RD}$ Low-to-Output Valid) | FULL | IV | | | 15 | | | 15 | ns |
| $T_{RDHOZ}$ ($\overline{RD}$ High-to-Data Three-State) | FULL | IV | | | 10 | | | 10 | ns |
| SERIAL I/O TIMING CHARACTERISTICS | | | | | | | | | |
| $T_{PRE}$ ($\overline{CS}$ Setup Time) | FULL | IV | 30 | | | 30 | | | ns |
| $T_{SCLK}$ (Period of Serial Data Clock) | FULL | IV | 100 | | | 100 | | | ns |
| $T_{DSU}$ (Serial Data Setup Time) | FULL | IV | 30 | | | 30 | | | ns |
| $T_{SCLKPWH}$ (Serial Data Clock Pulsewidth High) | FULL | IV | 40 | | | 40 | | | ns |
| $T_{SCLKPWL}$ (Serial Data Clock Pulsewidth Low) | FULL | IV | 40 | | | 40 | | | ns |
| $T_{DHLD}$ (Serial Data Hold Time) | FULL | IV | 0 | | | 0 | | | ns |
| $T_{DV}$ (Data Valid Time) | FULL | V | | 30 | | | 30 | | ns |
| CMOS LOGIC INPUTS | | | | | | | | | |
| Logic "1" Voltage | 25°C | I | 2.7 | | | 2.7 | | | V |
| Logic "0" Voltage | 25°C | I | | | 0.4 | | | 0.4 | V |
| Logic "1" Current | 25°C | IV | | | ±5 | | | ±5 | µA |
| Logic "0" Current | 25°C | IV | | | ±5 | | | ±5 | µA |
| Input Capacitance | 25°C | V | | 3 | | | 3 | | pF |

# AD9852–SPECIFICATIONS

| Parameter | Temp | Test Level | AD9852ASQ Min | AD9852ASQ Typ | AD9852ASQ Max | AD9852AST Min | AD9852AST Typ | AD9852AST Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| POWER SUPPLY[5] | | | | | | | | | |
| $+V_S$ Current[6] | 25°C | I | | 815 | 922 | | 585 | 660 | mA |
| $+V_S$ Current[7] | 25°C | I | | 640 | 725 | | 465 | 520 | mA |
| $+V_S$ Current[8] | 25°C | I | | 585 | 660 | | 425 | 475 | mA |
| $P_{DISS}$[6] | 25°C | I | | 2.7 | 3.195 | | 1.93 | 2.385 | W |
| $P_{DISS}$[7] | 25°C | I | | 2.115 | 2.515 | | 1.53 | 1.805 | W |
| $P_{DISS}$[8] | 25°C | I | | 1.930 | 2.285 | | 1.400 | 1.650 | W |
| $P_{DISS}$ Power-Down Mode | 25°C | I | | | 50 | | | 50 | mW |

NOTES

[1]The reference clock inputs are configured to accept a 1 V p-p (minimum) dc offset sine wave centered at one-half the applied $V_{DD}$ or a 3 V TTL-level pulse input.

[2]Change in duty cycle from 1 MHz to 100 MHz with 1 V p-p sine wave input and 0.5 V threshold.

[3]Represents comparator's inherent cycle-to-cycle jitter contribution. Input signal is a 1 V, 40 MHz square wave. Measurement device Wavecrest DTS – 2075.

[4]Comparator input originates from Analog Out section via external 7-pole elliptic LPF. Single-ended input, 0.5 V p-p. Comparator output terminated in 50 Ω.

[5]Important: In the 80-lead LQFP package simultaneous operation at the maximum ambient temperature of 85°C and at the maximum internal clock frequency at 200 MHz may cause the maximum die junction temperature of 150°C to be exceeded. Refer to the section of the data sheet entitled Power Dissipation section and Thermal Considerations section for derating and thermal management information.

[6]All functions engaged.

[7]All functions except inverse sinc engaged.

[8]All functions except inverse sinc and digital multipliers engaged.

Specifications subject to change without notice.

**EXPLANATION OF TEST LEVELS**

**Test Level**

I – 100% Production Tested.

III – Sample Tested Only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

**ABSOLUTE MAXIMUM RATINGS***

Maximum Junction Temperature . . . . . 150°C
$V_S$ . . . . . 4 V
Digital Inputs . . . . . –0.7 V to $+V_S$
Digital Output Current . . . . . 5 mA
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . –40°C to +85°C
Lead Temperature (Soldering 10 sec) . . . . . 300°C
Maximum Clock Frequency . . . . . 300 MHz

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

**ORDERING GUIDE**

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD9852ASQ | –40°C to +85°C | Thermally-Enhanced 80-Lead LQFP | SQ-80 |
| AD9852AST | –40°C to +85°C | 80-Lead LQFP | ST-80 |
| AD9852/PCB | 0°C to 70°C | Evaluation Board | |

**CAUTION**

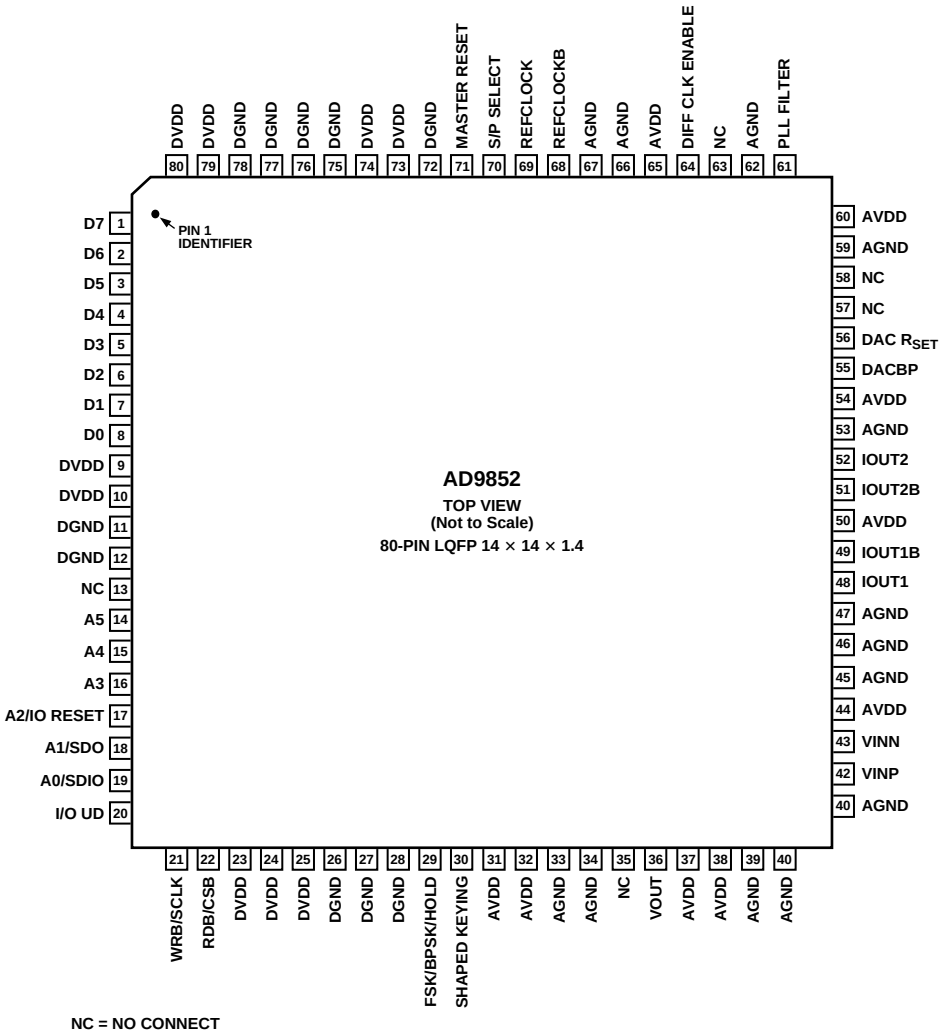
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9852 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**PIN FUNCTION DESCRIPTIONS**

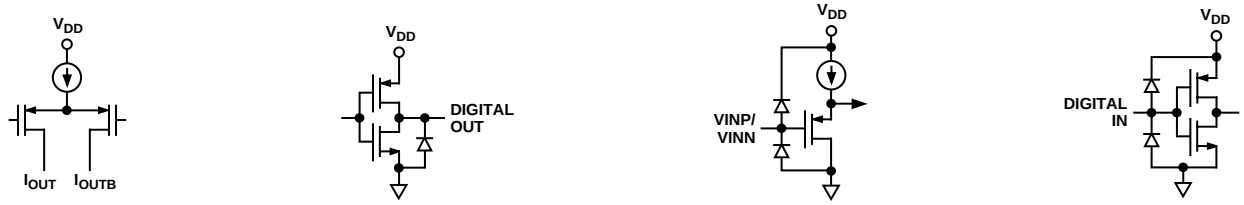
| Pin No. | Pin Name | Function |
|---|---|---|
| 1–8 | D7–D0 | Eight-Bit Bidirectional Parallel Programming Data Inputs. Used only in parallel programming mode. |
| 9, 10, 23, 24, 25, 73, 74, 79, 80 | DVDD | Connections for the Digital Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND. |
| 11, 12, 26, 27, 28, 72, 75, 76, 77, 78 | DGND | Connections for Digital Circuitry Ground Return. Same potential as AGND. |
| 13, 35, 57 58, 63 | NC | No Internal Connection. |
| 14–19 | A5–A0 | Six-Bit Parallel Address Inputs for Program Registers. Used only in parallel programming mode. A0, A1, and A2 have a second function when the serial programming mode is selected. See immediately below. |
| (17) | A2/IO RESET | Allows a RESET of the serial communications bus that is unresponsive due to improper programming protocol. Resetting the serial bus in this manner does not affect previous programming nor does it invoke the "default" programming values seen in the Table V. Active HIGH. |
| (18) | A1/SDO | Unidirectional Serial Data Output for Use in 3-Wire Serial Communication Mode. |
| (19) | A0/SDIO | Bidirectional Serial Data Input/Output for Use in 2-Wire Serial Communication Mode. |
| 20 | I/O UD | Bidirectional Frequency Update Signal. Direction is selected in control register. If selected as an input, a rising edge will transfer the contents of the programming registers to the internal works of the IC for processing. If I/O UD is selected as an output, an output pulse (low to high) of eight system clock cycle duration indicates that an internal frequency update has occurred. |
| 21 | WRB/SCLK | Write Parallel Data to Programming Registers. Shared function with SCLK. Serial clock signal associated with the serial programming bus. Data is registered on the rising edge. This pin is shared with WRB when the parallel mode is selected. |
| 22 | RDB/CSB | Read Parallel Data from Programming Registers. Shared function with CSB. Chip-select signal associated with the serial programming bus. Active LOW. This pin is shared with RDB when the parallel mode is selected. |
| 29 | FSK/BPSK/ HOLD | Multifunction Pin According to the Mode of Operation Selected in the Programming Control Register. If in the FSK mode logic low selects F1, logic high selects F2. If in the BPSK mode, logic low selects Phase 1, logic high selects Phase 2. If in the Chirp mode, logic high engages the HOLD function causing the frequency accumulator to halt at its current location. To resume or commence Chirp, logic low is asserted. |
| 30 | SHAPED KEYING | Must First Be Selected in the Programming Control Register to Function. A logic high will cause the cosine DAC output to ramp-up from zero-scale to full-scale amplitude at a preprogrammed rate. Logic low causes the full-scale output to ramp-down to zero-scale at the preprogrammed rate. |
| 31, 32, 37 38, 44, 50, 54, 60, 65 | AVDD | Connections for the Analog Circuitry Supply Voltage. Nominally 3.3 V more positive than AGND and DGND. |
| 33, 34, 39, 40, 41, 45, 46, 47, 53, 59, 62, 66, 67 | AGND | Connections for Analog Circuitry Ground Return. Same potential as DGND. |
| 36 | VOUT | Internal High-Speed Comparator's Noninverted Output Pin. Designed to drive 10 dBm to 50 Ω load as well as standard CMOS logic levels. |
| 42 | VINP | Voltage Input Positive. The internal high-speed comparator's noninverting input. |
| 43 | VINN | Voltage Input Negative. The internal high-speed comparator's inverting input. |
| 48 | IOUT1 | Unipolar Current Output of the Cosine DAC. |
| 49 | IOUT1B | Complementary Unipolar Current Output of the Cosine DAC. |
| 51 | IOUT2B | Complementary Unipolar Current Output of the Auxiliary DAC. |
| 52 | IOUT2 | Unipolar Current Output of the Auxiliary DAC. |

| Pin No. | Pin Name | Function |
|---|---|---|
| 55 | DACBP | Common Bypass Capacitor Connection for Both DACs. A 0.01 µF chip cap from this pin to AVDD improves harmonic distortion and SFDR slightly. No connect is permissible (slight SFDR degradation). |
| 56 | DAC $R_{SET}$ | Common Connection for Both DACs to Set the Full-Scale Output Current. $R_{SET}$ = 39.9/$I_{OUT}$. Normal $R_{SET}$ range is from 8 kΩ (5 mA) to 2 kΩ (20 mA). |
| 61 | PLL FILTER | This pin provides the connection for the external zero compensation network of the REFCLK Multiplier's PLL loop filter. The zero compensation network consists of a 1.3 kΩ resistor in series with a 0.01 µF capacitor. The other side of the network should be connected to AVDD as close as possible to Pin 60. For optimum phase noise performance, the REFCLK Multiplier can be bypassed by setting the "Bypass PLL" bit in control register 1E. |
| 64 | DIFF CLK | Differential REFCLK Enable. A high level of this pin enables the differential clock inputs, REFCLK and REFCLKB ENABLE (Pins 69 and 68 respectively). The minimum differential signal amplitude required is 800 mV p-p. The centerpoint or common-mode range of the differential signal ranges from 1.6 V to 1.9 V. |
| 68 | REFCLKB | The Complementary (180 Degrees Out-of-Phase) Differential Clock Signal. User should tie this pin high or low when single-ended clock mode is selected. Same signal levels as REFCLK. |
| 69 | REFCLK | Single-Ended Reference Clock Input or One of Two Differential Clock Signals. Normal 3.3 V CMOS logic levels or 1 V p-p sine wave centered about 1.6 V. |
| 70 | S/P SELECT | Selects Between Serial Programming Mode (Logic LOW) and Parallel Programming Mode (Logic High). |
| 71 | MASTER RESET | Initializes the serial/parallel programming bus to prepare for user programming; sets programming registers to a "do-nothing" state defined by the default values seen in the Table V. Active on logic high. Asserting MASTER RESET is essential for proper operation upon power-up. |

## PIN CONFIGURATION




NC = NO CONNECT




*a. DAC Outputs* *b. Comparator Output* *c. Comparator Input* *d. Digital Input*

*Figure 1. Equivalent Input and Output Circuits*

Figures 2–7 indicate the wideband harmonic distortion Performance of the AD9852 from 19.1 MHz to 119.1 MHz Fundamental Output, Reference Clock = 30 MHz, REFCLK Multiplier = 10. Each graph plotted from 0 MHz to 150 MHz.

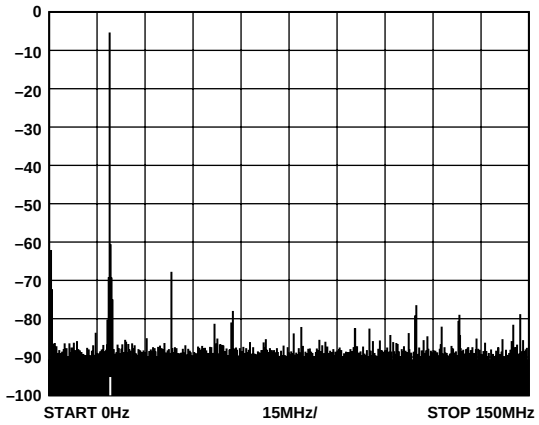



*Figure 2. Wideband SFDR, 19.1 MHz*

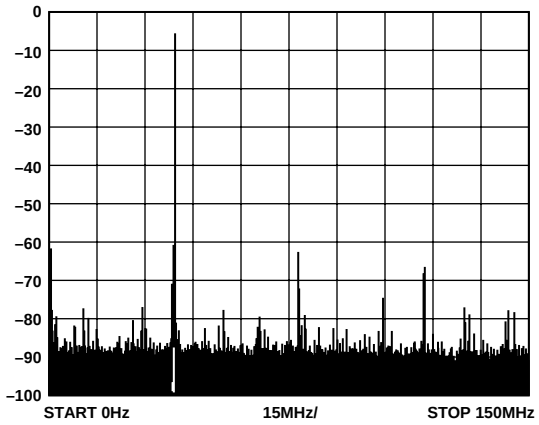



*Figure 3. Wideband SFDR, 39.1 MHz*

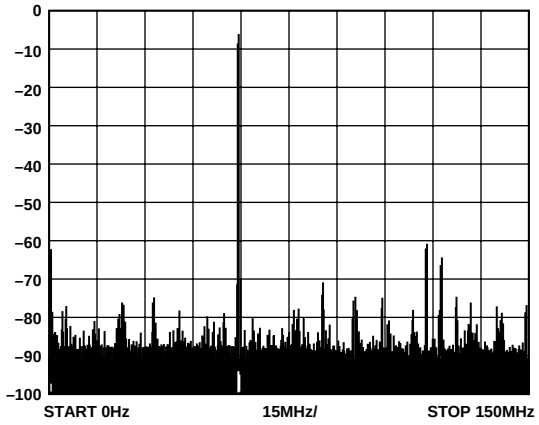



*Figure 4. Wideband SFDR, 59.1 MHz*

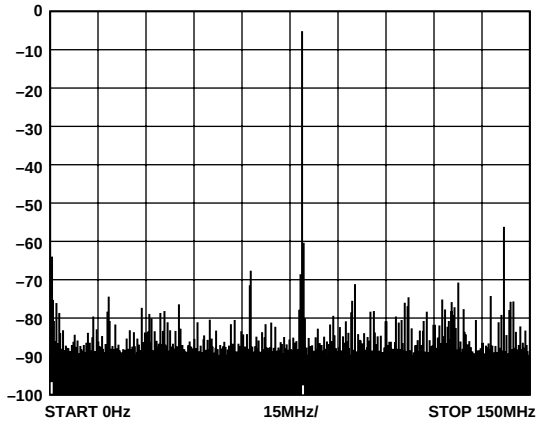



*Figure 5. Wideband SFDR, 79.1 MHz*

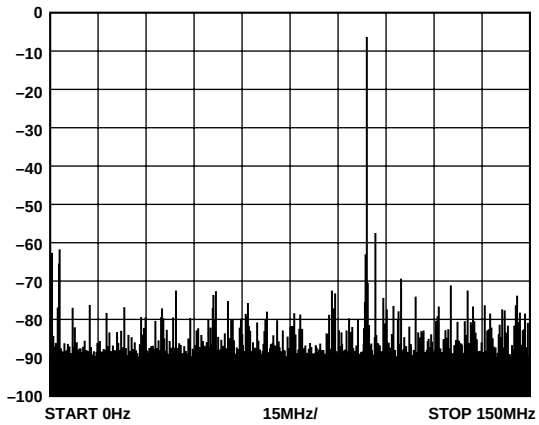



*Figure 6. Wideband SFDR, 99.1 MHz*

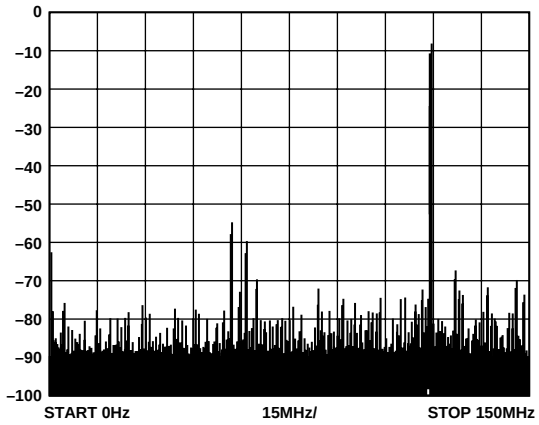



*Figure 7. Wideband SFDR, 119.1 MHz*

Figures 8–11 show the tradeoff in elevated noise floor, increased phase noise, and occasional discrete spurious energy when the internal REFCLK Multiplier circuit is engaged. Plots with wide (1 MHz) and narrow (50 kHz) spans are shown.

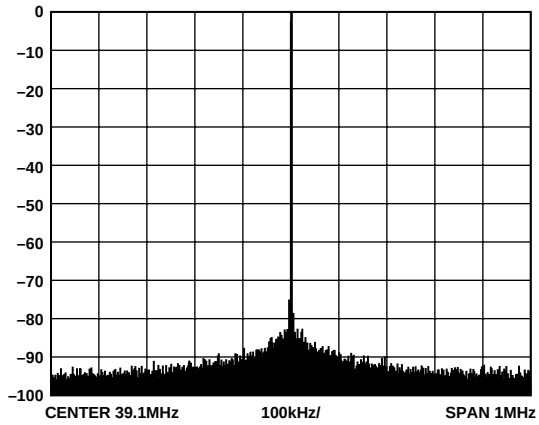



*Figure 8. Narrowband SFDR, 39.1 MHz, 1 MHz BW, 300 MHz EXTCLK with REFCLK Multiply Bypassed*

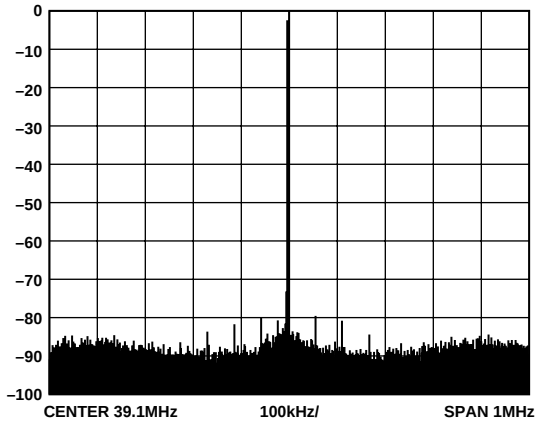



*Figure 10. Narrowband SFDR, 39.1 MHz, 1 MHz BW, 30 MHz EXTCLK with REFCLK Multiply = 10×*

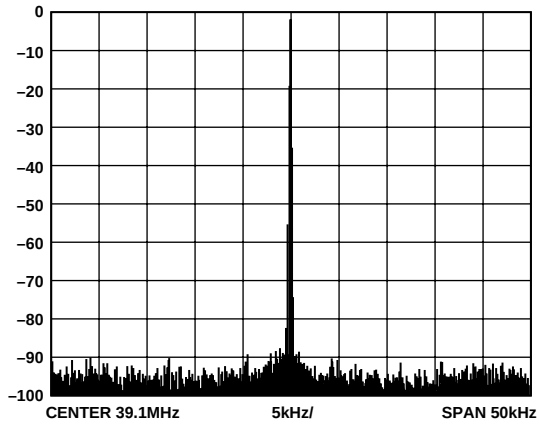



*Figure 9. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 300 MHz EXTCLK with REFCLK Multiplier Bypassed*

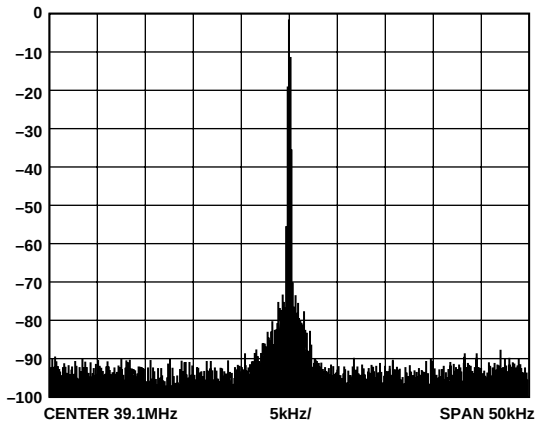



*Figure 11. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 30 MHz EXTCLK/REFCLK Multiplier = 10×*

Figures 12 and 13 show the slight increase in noise floor both with and without the PLL when slower clock speeds are used to generate the same fundamental frequency, that is, with a 100 MHz clock as opposed to a 300 MHz clock in Figures 9 and 11.

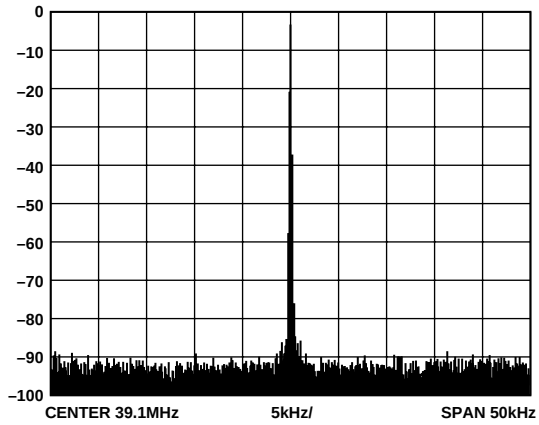



*Figure 12. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 100 MHz EXTCLK with REFCLK Multiplier Bypassed*

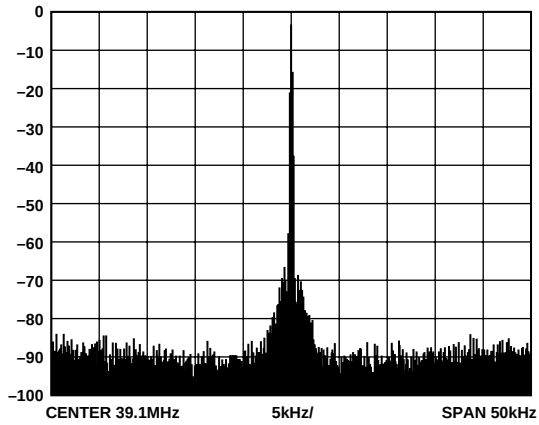



*Figure 13. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 10 MHz EXTCLK with REFCLK Multiplier = 10×*

Figures 14 and 15 show the effects of utilizing "sweet spots" in the tuning range of a DDS. Figure 14 represents a tuning word that accentuates the aberrations associated with truncation in the DDS algorithm. Figure 15 is essentially the same output frequency (a few tuning codes over), but it displays much fewer spurs on the output due to the selection of a tuning "sweet spot." Consideration should be given to all DDS applications to exploit the benefit of sweet spot tuning.

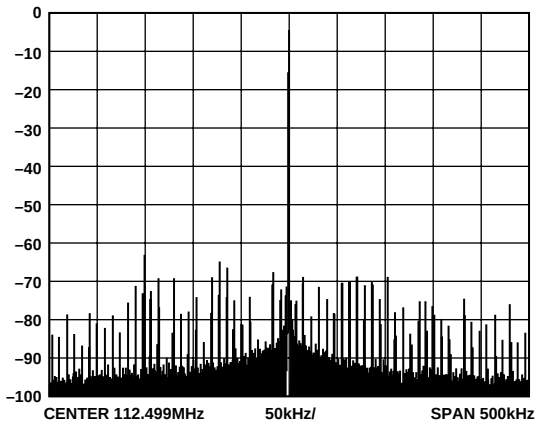



*Figure 14. The Opposite of a "Sweet Spot." 112.469 MHz with multiple high energy spurs close around the fundamental.*

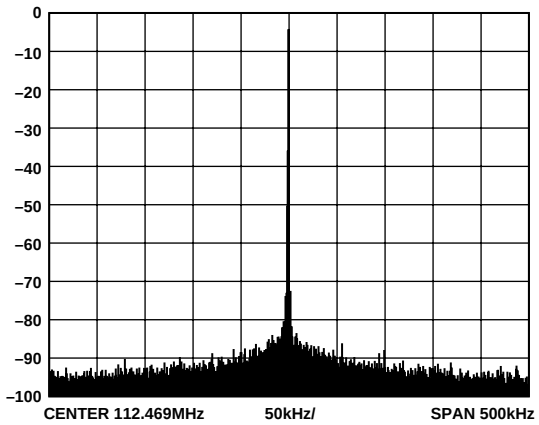



*Figure 15. A slight change in tuning word yields dramatically better results. 112.499 MHz with all spurs shifted out-of-band.*

Figures 16 and 17 show the narrowband performance of the AD9852 when operating with a 20 MHz reference clock and the REFCLK Multiplier enabled at 10× vs. a 200 MHz external reference clock.

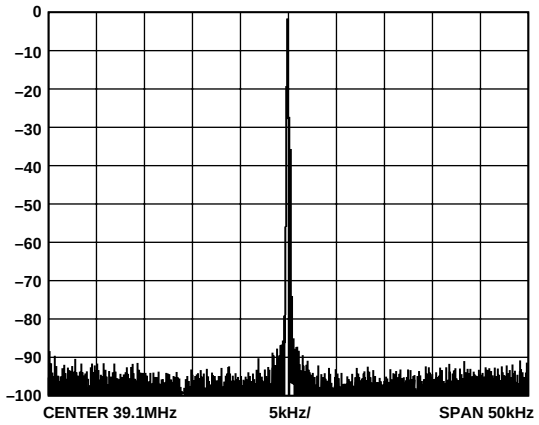



*Figure 16. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 200 MHz EXTCLK with REFCLK Multiplier Bypassed*

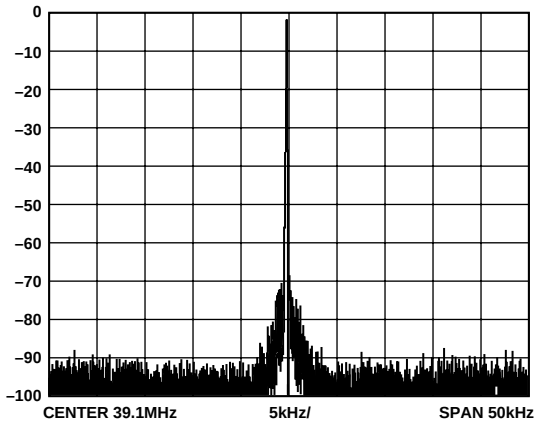
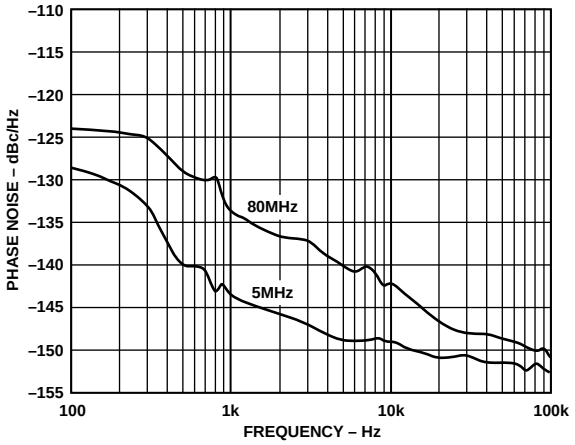
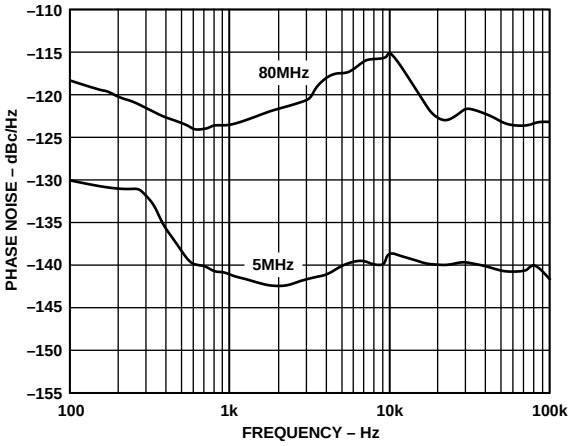



*Figure 17. Narrowband SFDR, 39.1 MHz, 50 kHz BW, 10 MHz EXTCLK with REFCLK Multiplier = 10×*




*a. Residual Phase Noise 300 MHz Direct Clocking*




*b. Residual Phase Noise, 300 MHz (10× REFCLK Multiplier Enabled)*

*Figure 18. Residual Phase Noise, EXTCLK = 300 MHz, REFCLK Multiplier Disabled/Enabled at 10×*

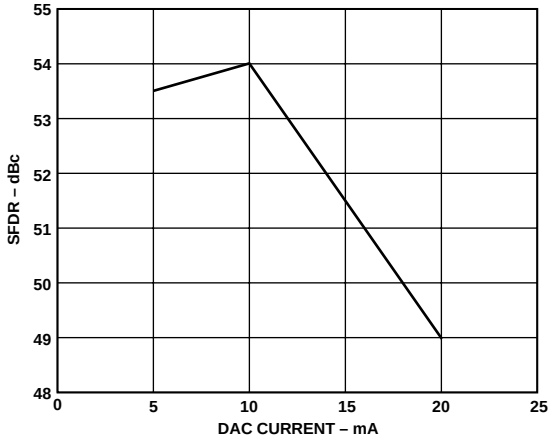



*Figure 19. SFDR vs. DAC Current, 59.1 MHz $A_{OUT}$, 300 MHz EXTCLK*

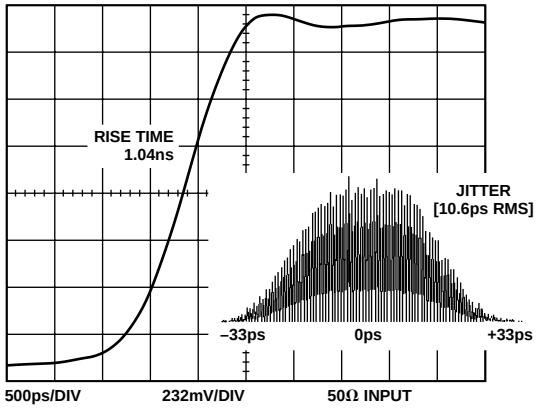



*Figure 21. Typical Comparator Output Jitter, 40 MHz $A_{OUT}$, 300 MHz EXTCLK/REFCLK Multiplier Disabled*

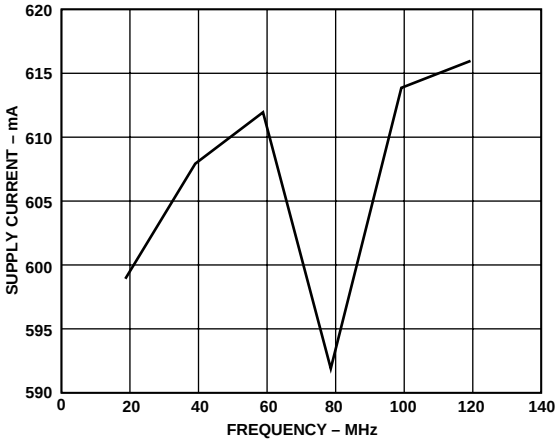



*Figure 20. Supply Current vs. Output Frequency; Variation Is Minimal as a Percentage and Heavily Dependent on Tuning Word*

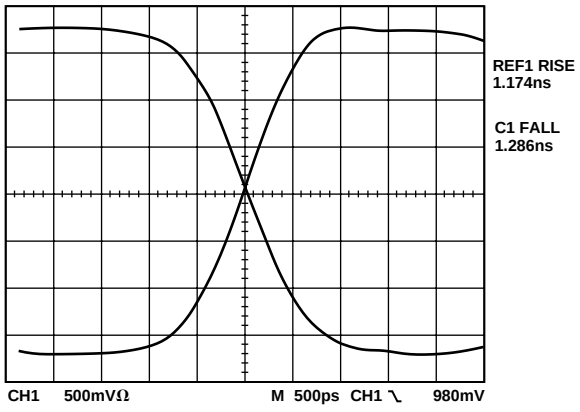



*Figure 22. Comparator Rise/Fall Times*

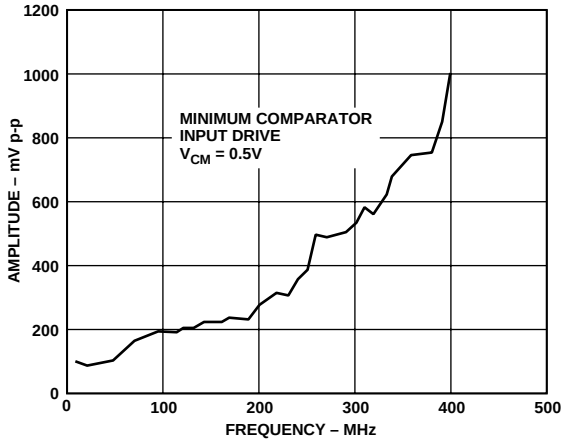



*Figure 23. Comparator Toggle Voltage Requirement*

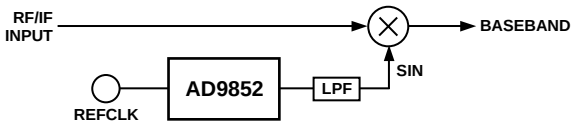



*Figure 24. Synthesized L.O. Application for the AD9852*

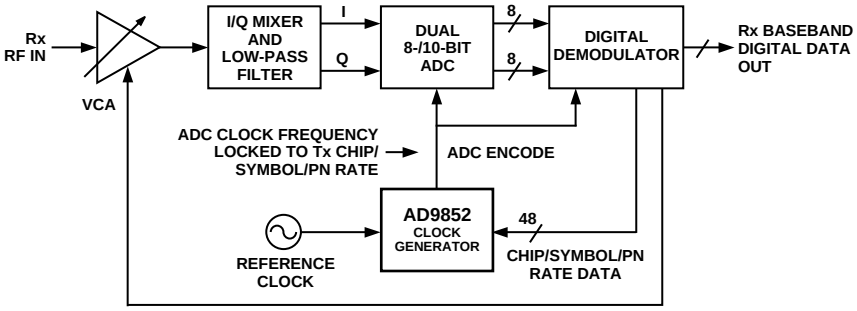



*Figure 25. Chip Rate Generator in Spread Spectrum Application*

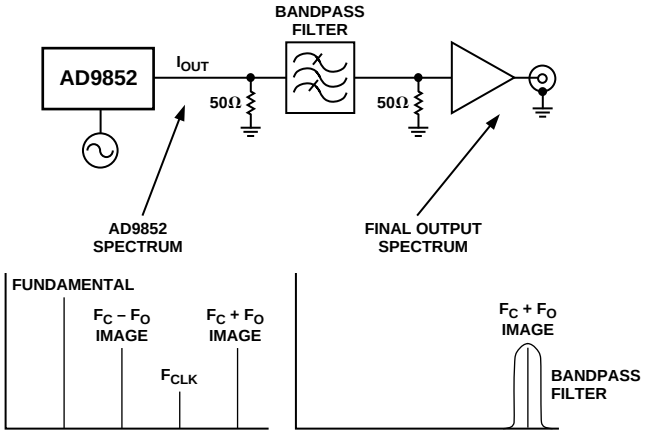



*Figure 26. Using an Aliased Image to Generate a High Frequency*

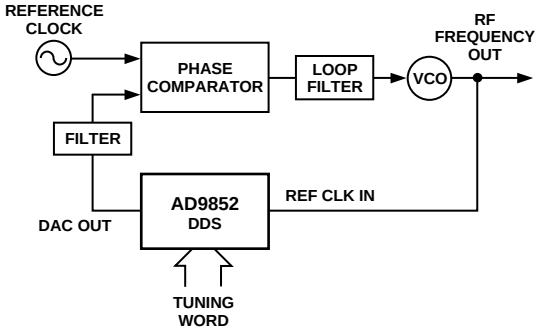



*Figure 27. Programmable "Divide-by-N" Synthesizer*

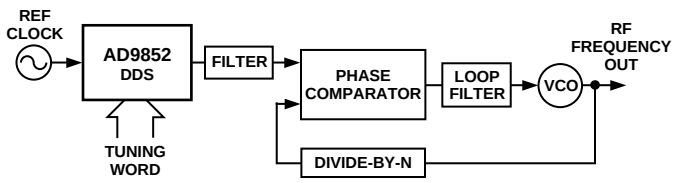



Figure 28. Agile High-Frequency Synthesizer

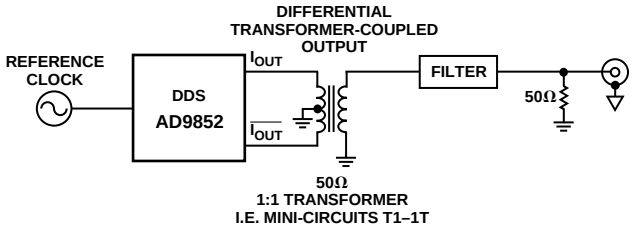



Figure 29. Differential Output Connection for Reduction of Common-Mode Signals

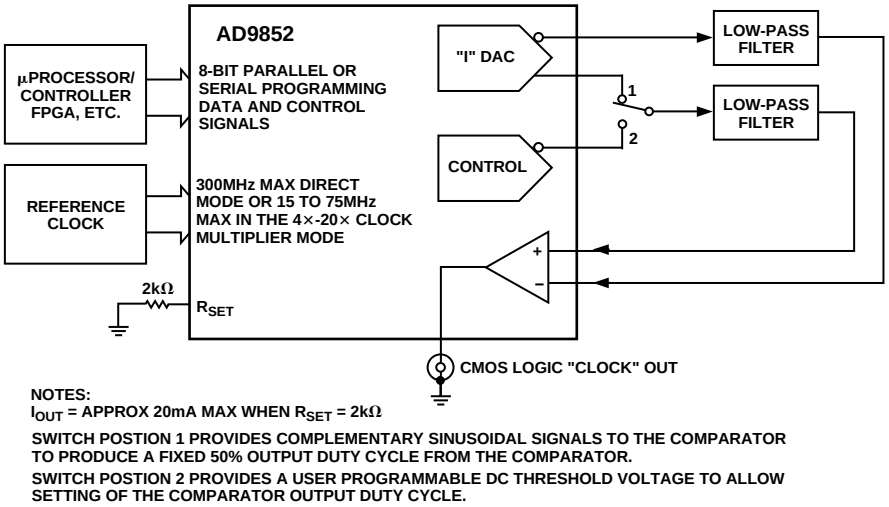



Figure 30. Frequency Agile Clock Generator Applications for the AD9852

*(continued from page 1)*

generation of a sine output at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to 100 million new frequencies per second. The (externally filtered) sine wave output can be converted to a square wave by the internal comparator for agile clock generator applications. The device provides 14 bits of digitally-controlled phase modulation and single-pin PSK. The on-board 12-bit DAC, coupled with the innovative DDS architecture, provide excellent wideband and narrowband output SFDR. There is also an auxiliary DAC that can be configured as a user-programmable control DAC. When configured with the on-board comparator, the 12-bit control DAC facilitates duty cycle control, in the high-speed clock generator application. A 12-bit digital multiplier permits programmable amplitude modulation, shaped on/off keying and precise amplitude control of the output. Chirp functionality is also included which facilitates wide bandwidth frequency sweeping applications. The AD9852's programmable 4×–20× REFCLK multiplier circuit generates the 300 MHz clock internally from a lower frequency external reference clock. This saves the user the expense and difficulty of implementing a 300 MHz clock source. Direct 300 MHz clocking is also accommodated with either single-ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of "ramped" FSK are supported. The AD9852 uses advanced 0.35 micron CMOS technology to provide this high level of functionality on a single 3.3 V supply.

The AD9852 is available in a space-saving 80-lead LQFP surface-mount package and a thermally-enhanced 80-lead LQFP package. The AD9852 is pin-for-pin compatible with the AD9854 quadrature output synthesizer device. It is specified to operate over the extended industrial temperature range of –40°C to +85°C.

## OVERVIEW

The AD9852 digital synthesizer is a highly flexible device that will address a wide range of applications. The device consists of an NCO with 48-bit phase accumulator, programmable reference clock multiplier, inverse sinc filters, digital multipliers, two 12-bit/300 MHz DACs, high-speed analog comparator, and interface logic. This highly integrated device can be configured to serve as a synthesized L.O., agile clock generator, and FSK/BPSK modulator. The theory of operation of the functional blocks of the device, and a technical description of the signal flow through a DDS device, can be found in a tutorial from Analog Devices, called, "A Technical Tutorial on Digital Signal Synthesis." This tutorial is available on CD-ROM and information on obtaining it can be found at the Analog Devices DDS website at **www.analog.com/dds**. The tutorial also provides basic applications information for a variety of digital synthesis implementations. The DDS background subject matter is not covered in this data sheet; the functions and features of the AD9852 will be individually discussed herein.

## USING THE AD9852

### Internal and External Update Clock

This function is comprised of a bidirectional I/O pin, Pin 20, and a programmable 32-bit down-counter. *In order for programming changes to be transferred from the I/O Buffer registers to the active core of the DDS, a clock signal (low-to-high edge) must be externally supplied to Pin 20 or internally generated by the 32-bit Update Clock.*

An externally generated Update Clock is internally synchronized with the system clock to prevent partial transfer of program register information due to violation of data setup or hold times. This mode gives the user complete control of when updated program information becomes effective. The default mode is set for internal update clock (Int Update Clk control register bit is logic high). To switch to external update clock mode, the Int Update Clk register bit must be set to logic low. The internal update mode generates automatic, periodic update pulses whose time period is set by the user.

An internally generated Update Clock can be established by programming the *32-bit Update Clock* registers (address 16–19 hex) and setting the *Int Update Clk* (address 1F hex) control register bit to logic high. The update clock down-counter function operates at the system clock/2 (150 MHz maximum) and counts down from a 32-bit binary value (programmed by the user). When the count reaches 0, an automatic I/O Update of the DDS output or functions is generated. The update clock is routed internally and externally on Pin 20 to allow users to synchronize programming of update information with the update clock rate. The time period between update pulses is given as:

$$(N+1) \times (SYSTEM\ CLOCK\ PERIOD \times 2)$$

where $N$ is the 32-bit value programmed by the user. Allowable range of N is from 1 to $(2^{32} - 1)$. The internally generated update pulse output on Pin 20 has a fixed high time of eight system clock cycles.

### Shaped On/Off Keying

Allows user to control the ramp-up and ramp-down time of an "on/off" emission from the I and Q DACs. This function is used in "burst transmissions" of digital data to reduce the adverse spectral impact of short, abrupt bursts of data. Users must first enable the digital multipliers by setting the OSK EN bit (control register address 20 hex) to logic high in the control register. Otherwise, if the OSK EN bit is set low, the digital multipliers responsible for amplitude control are bypassed and the I and Q DAC outputs are set to full-scale amplitude. In addition to setting the OSK EN bit, a second control bit, OSK INT (also at address 20 hex) must be set to logic high. Logic high selects the *linear* internal control of the output ramp-up or ramp-down function. A logic low in the OSK INT bit switches control of the digital multipliers to user programmable 12-bit registers allowing users to dynamically shape the amplitude transition in practically any fashion. These 12-bit registers, labeled "Output Shape Key" are located at addresses 21 through 24 hex in Table V. The maximum output amplitude is a function of the $R_{SET}$ resistor and is not programmable when OSK INT is enabled.

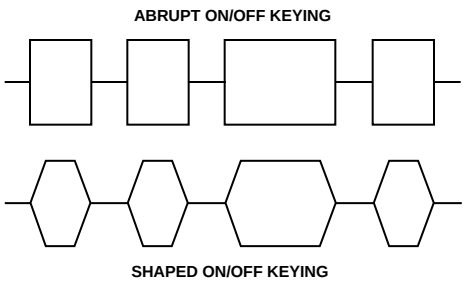



*Figure 31. Shaped On/Off Keying*

Next, the transition time from zero-scale to full-scale must be programmed. The transition time is a function of two fixed elements and one variable. The variable element is the program mable 8-bit RAMP RATE COUNTER. This is a down-counter being clocked at the system clock rate (300 MHz max) that outputs one pulse whenever the counter reaches zero. This pulse is routed to a 12-bit counter that increments one LSB for every pulse received. The outputs of the 12-bit counter are connected to the 12-bit digital multiplier. When the digital multiplier has a value of all zeros at its inputs, the input signal is multiplied by zero, producing zero-scale. When the multiplier has a value of all ones, the input signal is multiplied by a value of one, producing full-scale. There are 4094 remaining fractional multiplier values that will produce output amplitudes corresponding to their binary values.

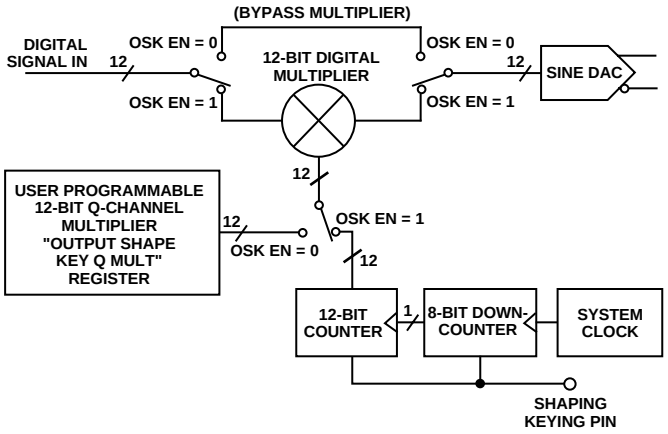



*Figure 32. Block Diagram of Data Pathway of the Digital Multiplier Section Responsible for Shaped Keying Function*

The two fixed elements are the clock period of the system clock, which drives the Ramp Rate Counter, and the 4096 amplitude steps between zero-scale and full-scale. To give an example, assume that the System Clock of the AD9852 is 100 MHz (10 ns period). If the Ramp Rate Counter is programmed for a minimum count of five, it will take two system clock periods (one rising edge loads the count-down value, the next edge decrements the counter from five to four). The relationship of the 8-bit count-down value to the time period between output pulses is given as:

$$(N+1) \times SYSTEM\ CLOCK\ PERIOD,$$

where $N$ is the 8-bit count-down value. It will take 4096 of these pulses to advance the 12-bit up-counter from zero-scale to full-scale. Therefore, the minimum shaped keying ramp time for a 100 MHz system clock is $4096 \times 6 \times 10$ ns = approximately 246 µs. The maximum ramp time will be $4096 \times 256 \times 10$ ns = approximately 10.5 µs.

Finally, changing the logic state of Pin 30, "shaped keying" will automatically perform the programmed output envelope functions when OSK INT is high. A logic high on Pin 30 causes the outputs to linearly ramp up to full-scale amplitude and hold until the logic level is changed to low, causing the outputs to ramp down to zero-scale.

**Cosine DAC**

The cosine DAC generates the 300 MSPS (maximum) cosine output of the DDS. The maximum output amplitude is set by the DAC $R_{SET}$ resistor at Pin 56. This is a current-out DAC with a full-scale maximum output of 20 mA; however, a nominal 10 mA output current provides best spurious-free dynamic range (SFDR) performance. The value of $R_{SET} = 39.93/I_{OUT}$, where $I_{OUT}$ is in amps. DAC output compliance specification limits the maximum voltage developed at the outputs to –0.5 V to +1 V. Voltages developed beyond this limitation will cause excessive DAC distortion and possibly permanent damage. The user must choose a proper load impedance to limit the output voltage swing to the compliance limits. For best SFDR, both DAC outputs should be terminated equally, especially at higher output frequencies where harmonic distortion errors are more prominent.

The cosine DAC is preceded by inverse SIN(x)/x filters (a.k.a. inverse sinc filter) that precompensate for DAC output amplitude variations over frequency to achieve flat amplitude response from dc to Nyquist. A digital multiplier follows the inverse sinc filters to allow amplitude control, amplitude modulation and amplitude shaped keying. The inverse sinc filter (address 20 hex, Bypass Inv Sinc bit)) and digital multiplier (address 20 hex, OSK EN bit) can be bypassed for power conservation by setting those bits high. Both DACs can be powered down by setting the DAC $\overline{PD}$ bit high (address 1D of control register) when not needed.

Cosine DAC outputs are designated as IOUT1 and IOUT1B, Pins 48 and 49 respectively.

**Control DAC**

The 12-bit auxiliary, or control DAC can provide dc control levels to external circuitry, generate ac signals, or duty cycle control, of the on-board comparator. The input twos complement data is channeled through the serial or parallel interface to the 12-bit register (address 26 and 27 hex) at a maximum 100 MHz data rate. This DAC is clocked at the system clock, 300 MSPS (maximum), and has the same maximum output current capability as that of the cosine DAC. The single $R_{SET}$ resistor on the AD9852 sets the full-scale output current for both cosine DAC and the control DACs. The control DAC can be separately powered down for power conservation when not needed by setting the Control DAC POWER-DOWN bit high (address 1D hex). Control DAC outputs are designated as IOUT2 and IOUT2B (Pins 52 and 51 respectively).

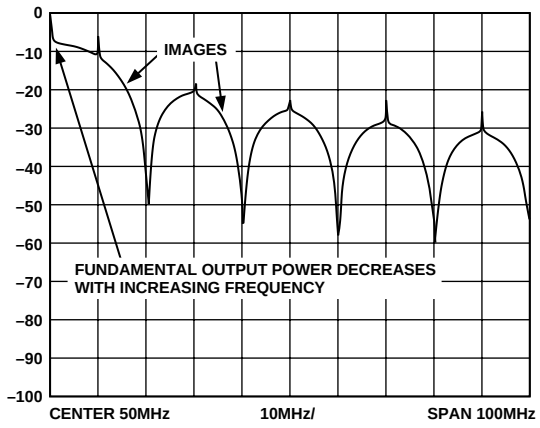



*Figure 33. Normal SIN(x)/x DAC Output Power Envelope Filter*

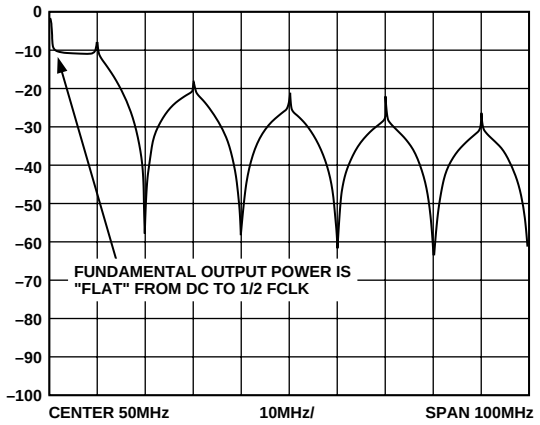



*Figure 34. Inverse SIN(x)/x (Inverse Sinc) Filter Engaged*

**Inverse SINC Function**

This filter precompensates input data to the cosine DAC for the SIN(x)/x roll-off function to allow wide bandwidth signals (such as QPSK) to be output from the DACs without appreciable amplitude variations that will cause increased EVM (error vector magnitude). The inverse SINC function may be bypassed to *significantly* reduce power consumption, especially at higher clock speeds. Inverse sinc is engaged by default and is bypassed by bringing the "Bypass Inv Sinc" bit high in control register 20 (hex) in Table V.

**REFCLK Multiplier**

This is a programmable PLL-based reference clock multiplier that allows the user to select an integer clock multiplying value over the range of 4× to 20× by which the REFCLK input will be multiplied. Use of this function allows users to input as little as 15 MHz to produce a 300 MHz internal system clock. Five bits in control register 1E hex set the multiplier value as follows in Table I.

**Table I. REFCLK Multiplier Control Register Values**

| Multiplier Value | Ref Mult 4 | Ref Mult 3 | Ref Mult 2 | Ref Mult 1 | Ref Mult 0 |
|---|---|---|---|---|---|
| 4 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 |
| 12 | 0 | 1 | 1 | 0 | 0 |
| 13 | 0 | 1 | 1 | 0 | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 |
| 15 | 0 | 1 | 1 | 1 | 1 |
| 16 | 1 | 0 | 0 | 0 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 |
| 18 | 1 | 0 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 1 |
| 20 | 1 | 0 | 1 | 0 | 0 |

The REFCLK Multiplier function can be bypassed to allow direct clocking of the AD9852 from an external clock source. The *system clock* for the AD9852 is either the output of the REFCLK Multiplier (if it is engaged) or the REFCLK inputs. REFCLK may be either a single-ended or differential input by setting Pin 64, DIFF CLK ENABLE**,** low or high respectively.

***PLL Range Bit***

The PLL Range Bit selects the frequency range of the REFCLK Multiplier PLL. For operation from 200 MHz to 300 MHz (internal system clock rate) the PLL Range Bit should be set to Logic 1. For operation below 200 MHz, the PLL Range Bit should be set to Logic 0. The PLL Range Bit adjusts the PLL loop parameters for optimized phase noise performance within each range.

***Pin 61, PLL FILTER***

This pin provides the connection for the external zero compensation network of the PLL loop filter. The zero compensation network consists of a 1.3 kΩ resistor in series with a 0.01 μF capacitor. The other side of the network should be connected to as close as possible to Pin 60, AVDD. For optimum phase noise performance the clock multiplier can be bypassed by setting the "Bypass PLL" bit in control register address 1E.

***Differential REFCLK Enable***

A high level on this pin enables the differential clock Inputs, REFCLOCK and REFCLOCKB (Pins 69 and 68 respectively). The minimum differential signal amplitude required is 800 mV p-p. The centerpoint or common-mode range of the differential signal can range from 1.6 V to 1.9 V.

When Pin 64 (*DIFF CLK ENABLE*) is tied low, REFCLK (Pin 69) is the only active clock input. This is referred to as the *single-ended* mode. In this mode, Pin 68 (REFCLKB) should be tied low or high, but not left floating.

***Parallel/Serial Programming Mode***

Setting Pin 70 high invokes parallel mode, whereas setting Pin 70 low will invoke the serial programming mode. Please refer to the text describing the serial and parallel programming protocol contained in this data sheet for further information.

Two control bits located at address 20 hex in the Table V apply only to the serial programming mode. *LSB First* when high, dictates that serial data will be loaded starting with the LSB of the word. When low (the default value), serial data is loaded starting with the MSB of the word. *SDO Active* when high indicates that the SDO pin, Pin 18, is dedicated to reading back data from the AD9852 registers. When SDO Active is low (default value), this indicates that the SDIO pin, Pin 19, acts as a bidirectional serial data input and output pin and Pin 18 has no function in the serial mode.

## DESCRIPTION OF AD9852 MODES OF OPERATION

There are five programmable modes of operation of the AD9852. Selecting a mode requires that three bits in the Control Register (parallel address 1F hex) be programmed as follows in Table II.

**Table II. Mode Selection Table**

| Mode 2 | Mode 1 | Mode 0 | Result |
|---|---|---|---|
| 0 | 0 | 0 | SINGLE-TONE |
| 0 | 0 | 1 | FSK |
| 0 | 1 | 0 | RAMPED FSK |
| 0 | 1 | 1 | CHIRP |
| 1 | 0 | 0 | BPSK |

In each mode, engaging certain functions may or may not be permitted. Shown in Table III is a listing of some important functions and their availability for each mode.

**Single-Tone (Mode 000)**
This is the default mode when master reset is asserted or when it is user-programmed into the control register. The Phase Accumulator, responsible for generating an output frequency, is presented with a 48-bit value from Frequency Tuning Word 1 registers whose default values are zero. Default values from the remaining applicable registers will further define the single-tone output signal qualities.

The default values after a master reset, define a safe, "no output" value resulting in an output signal of 0 Hertz, 0 phase. Upon power-up and reset the output from both I and Q DACs will be a dc value equal to the midscale output current. This is the default mode amplitude setting of zero. Refer to the digital multiplier section for further explanation of the output amplitude control. It will be necessary to program all or some of the 28 program registers to realize a user-defined output signal.

Figure 35 graphically shows the transition from the default condition (0 Hz) to a user-defined output frequency (F1).

As with all Analog Devices DDSs, the value of the frequency tuning word is determined using the following equation:

$$FTW = (Desired\ Output\ Frequency \times 2^N)/SYSCLK.$$

Where $N$ is the phase accumulator resolution (48 bits in this instance), frequency is expressed in Hertz, and the FTW, Frequency Tuning Word, is a decimal number. Once a decimal number has been calculated, it must be rounded to an integer and then converted to binary format—a series of 48 binary-weighted 1s or 0s. The fundamental sine wave DAC output frequency range is from dc to 1/2 SYSCLK.

Changes in frequency are phase continuous—that is, the new frequency uses the last phase of the old frequency as the reference point to compute the first new frequency phase.

The single-tone mode allows the user to control the following signal qualities:

- Output Frequency to 48-Bit Accuracy
- Output Amplitude to 12-Bit Accuracy
  - Fixed, User-Defined, Amplitude Control
  - Variable, Programmable Amplitude Control
  - Automatic, Programmable, Single-Pin-Controlled, "Shaped On/Off Keying"
- Output Phase to 14-Bit Accuracy

Furthermore, all of these qualities can be changed or modulated via the 8-bit parallel programming port at a 100 MHz parallel-byte rate, or at a 10 MHz serial rate. Incorporating this attribute will permit FM, AM, PM, FSK, PSK, ASK operation in the single-tone mode.

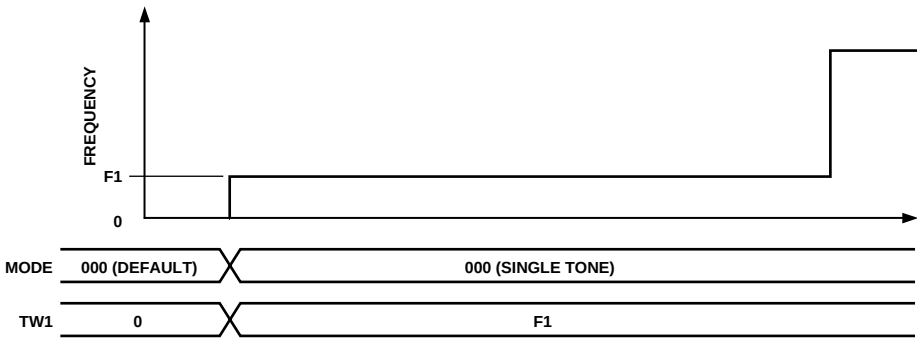



*Figure 35. Default State to User-Defined Output Transition*

**Table III. Function Availability vs. Mode of Operation**

| Mode | Phase Adjust 1 | Phase Adjust 2 | Single-Pin FSK/BPSK or HOLD | Single-Pin Shaped-Keying | Phase Offset or Modulation | Amplitude Control or Modulation | Inverse SINC Filter | Frequency Tuning Word 1 | Frequency Tuning Word 2 | Automatic Frequency Sweep |
|---|---|---|---|---|---|---|---|---|---|---|
| Single-Tone | ✓ | X | X | ✓ | ✓ | ✓ | ✓ | ✓ | X | X |
| FSK | ✓ | X | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | X |
| Ramped FSK | ✓ | X | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| CHIRP | ✓ | X | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | X | ✓ |
| BPSK | ✓ | ✓ | ✓ | ✓ | X | ✓ | ✓ | ✓ | X | X |

**Unramped FSK (Mode 001)**
When selected, the output frequency of the DDS is a function of the values loaded into Frequency Tuning Word registers 1 and 2 and the logic level of Pin 29 (FSK/BPSK/HOLD). A logic low on Pin 29 chooses F1 (frequency tuning word 1, parallel address 4–9 hex) and a logic high chooses F2 (frequency tuning word 2, parallel register address A–F hex). Changes in frequency are phase-continuous and practically instantaneous. (Please refer to pipeline delays in specification table.) Other than F2 and Pin 29 becoming active, this mode is identical to single-tone.

The unramped FSK mode, Figure 36, is representative of traditional FSK, RTTY (Radio Teletype) or TTY (Teletype) transmission of digital data. Frequency transitions occur nearly instantaneously from F1 to F2. This simple method works extremely well and is the most reliable form of digital communication, but it is also wasteful of RF spectrum.

See the following Ramped FSK section for an alternative FSK method that conserves bandwidth.

**Ramped FSK (Mode = 010)**
A method of FSK whereby changes from F1 to F2 are not instantaneous but instead are accomplished in a frequency sweep or "ramped" fashion. The "ramped" notation implies that the sweep is linear. While linear sweeping or frequency ramping is easily and automatically accomplished, it is only one of many possibilities. Other frequency transition schemes may be implemented by changing the ramp rate and ramp step size "on-the-fly," in piecewise fashion.

Frequency ramping, whether linear or nonlinear, necessitates that many intermediate frequencies between F1 and F2 will be output in addition to the primary F1 and F2 frequencies. Figures 37 and 38 graphically depict the frequency versus time characteristics of a linear ramped FSK signal.

The purpose of ramped FSK is to provide better bandwidth containment than traditional FSK by replacing the instantaneous frequency changes with more gradual, user-defined frequency changes. The dwell time at F1 and F2 can be equal to or much greater than the time spent at each intermediate frequency. The user controls the dwell time at F1 and F2, the number of intermediate frequencies and time spent at each frequency. Unlike unramped FSK, ramped FSK requires the lowest frequency to be loaded into F1 registers and the highest frequency into F2 registers.

Several registers must be programmed to instruct the DDS regarding the resolution of intermediate frequency steps (48 bits) and the time spent at each step (20 bits). Furthermore, the CLR ACC1 bit in the control register should be toggled (low-high-low) prior to operation to assure that the frequency accumulator is starting from an "all zeros" output condition. For piecewise, nonlinear frequency transitions, it is necessary to reprogram the registers *while* the frequency transition is in progress to affect the desired response.

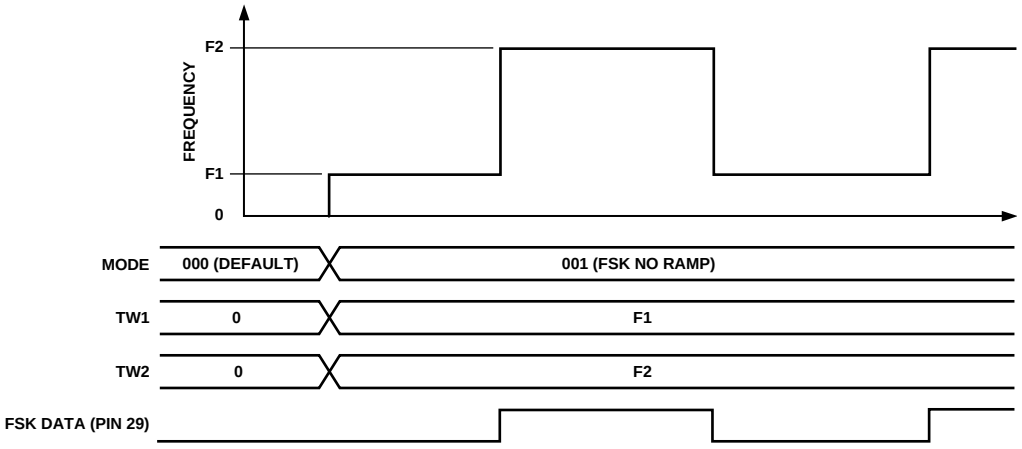



*Figure 36. Traditional FSK Mode*

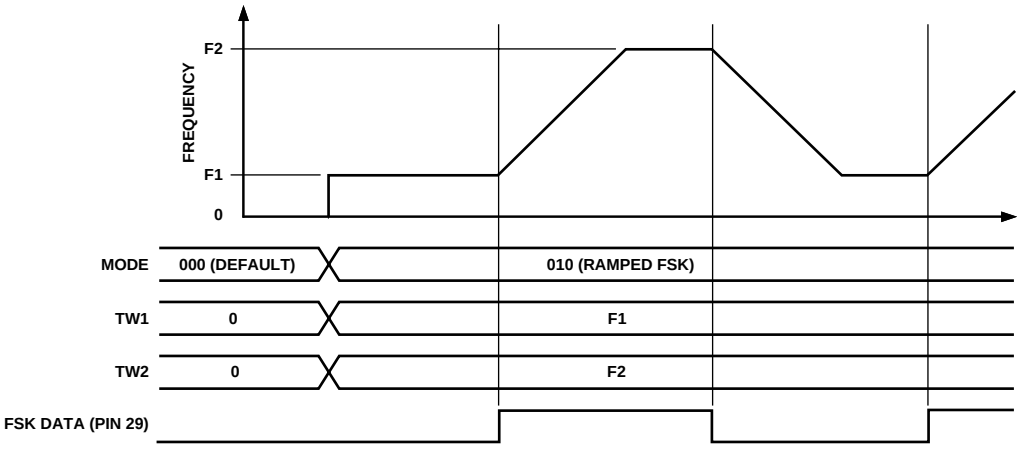



*Figure 37. Ramped FSK Mode*

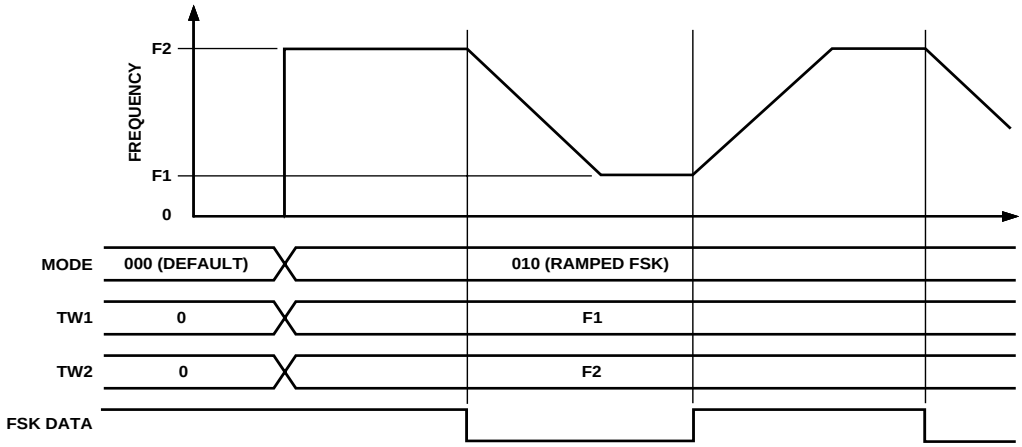



*Figure 38. Ramped FSK Mode*

Parallel register addresses 1A–1C hex comprise the 20-bit "Ramp Rate Clock" registers. This is a count-down counter that outputs a single pulse whenever the count reaches zero. The counter is activated any time a logic level change occurs on FSK input Pin 29. This counter is run at the System Clock Rate, 300 MHz maximum. The time period between each output pulse is given as

$$(N+1) \times (SYSTEM\ CLOCK\ PERIOD)$$

where $N$ is the 20-bit ramp rate clock value programmed by the user. Allowable range of N is from 1 to $(2^{20} - 1)$. The output of this counter clocks the 48-bit Frequency Accumulator shown below in Figure 39. The Ramp Rate Clock determines the amount of time spent at each intermediate frequency between F1 and F2. The counter stops automatically when the destination frequency is achieved. The "dwell time" spent at F1 and F2 is determined by the duration that the FSK input, Pin 29, is held high or low after the destination frequency has been reached.

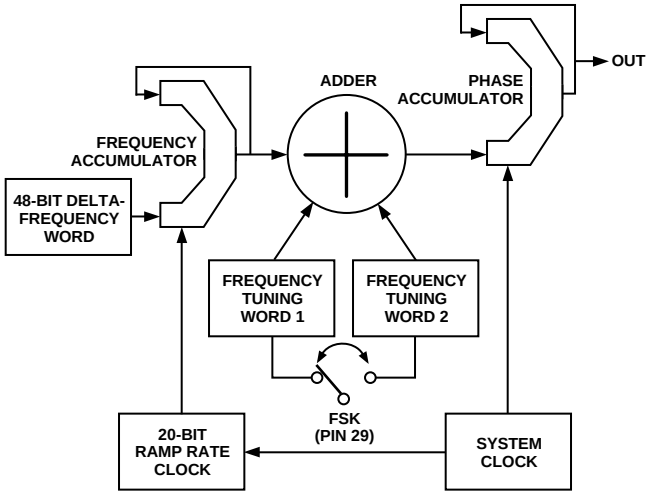



*Figure 39. Block Diagram of Ramped FSK Function*

Parallel register addresses 10–15 hex comprise the 48-bit, straight binary, "Delta Frequency Word" registers. This 48-bit word is accumulated (added to the accumulator's output) every time it receives a clock pulse from the ramp rate counter. The output of this accumulator is then added to or subtracted from the F1 or F2 frequency word, which is then fed to the input of the 48-bit Phase Accumulator that forms the numerical phase steps for the sine and cosine wave outputs. In this fashion, the output frequency is ramped up and down in frequency, according to the logic-state of Pin 29. The rate at which this happens is a function of the 20-bit ramp rate clock. Once the destination frequency is achieved, the ramp rate clock is stopped, which halts the frequency accumulation process.

Generally speaking, the Delta Frequency Word will be a much smaller value as compared to that of the F1 or F2 tuning word. For example, if F1 and F2 are 1 kHz apart at 13 MHz, the Delta Frequency Word might be only 25 Hz.

Figure 41 shows that premature toggling causes the ramp to immediately reverse itself and proceed at the same rate and resolution back to originating frequency.

The control register contains a Triangle bit at parallel register address 1F hex. Setting this bit high in Mode 010 causes an *automatic* ramp-up and ramp-down between F1 and F2 to occur without having to toggle Pin 29 as shown in Figure 40. In fact, the logic state of Pin 29 has no effect once the Triangle bit is set high. This function uses the ramp-rate clock time period and the delta-frequency-word step size to form a continuously sweeping linear ramp from F1 to F2 and back to F1 with equal dwell times at every frequency. Using this function, one can automatically sweep from dc to the Nyquist limit or any other two frequencies between dc and Nyquist.

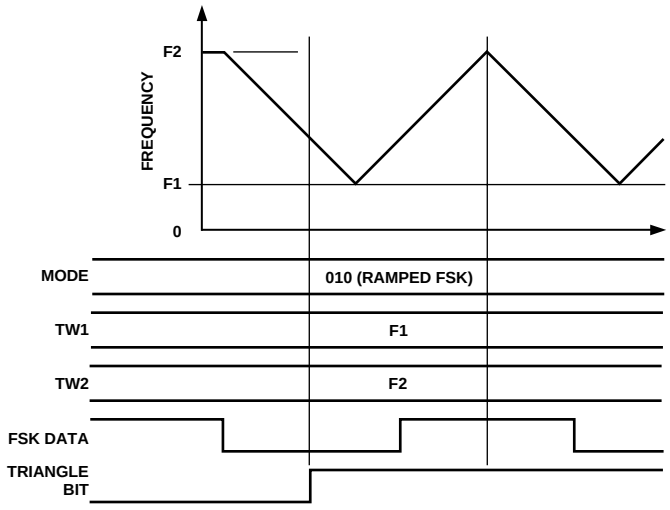



*Figure 40. Effect of Triangle Bit in Ramped FSK Mode*

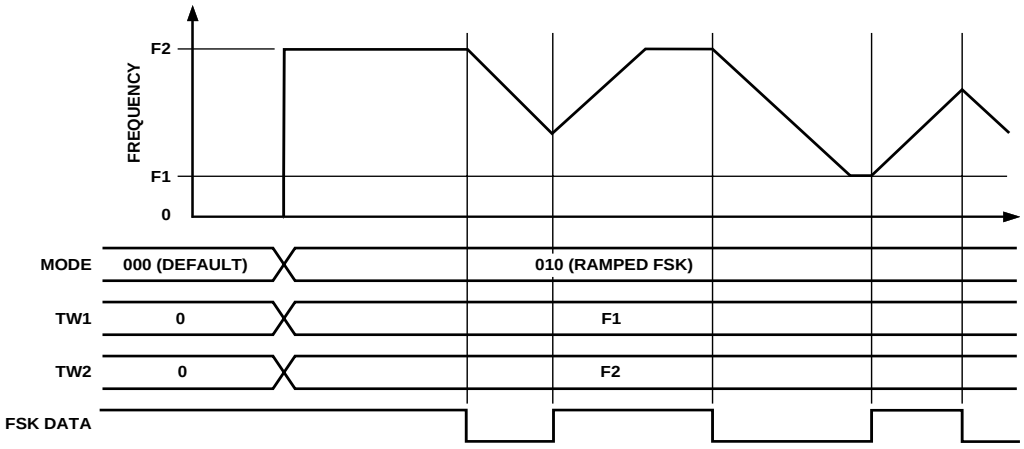



*Figure 41. Effect of Premature Ramped FSK Data*

In the ramped FSK mode with the triangle bit set high an automatic frequency sweep will begin at either F1 or F2, according to the logic level on Pin 29 (FSK input pin) when the triangle bit's rising edge occurs as shown in Figure 42. If the FSK data bit had been high instead of low, F2 would have been chosen instead of F1 as the start frequency.

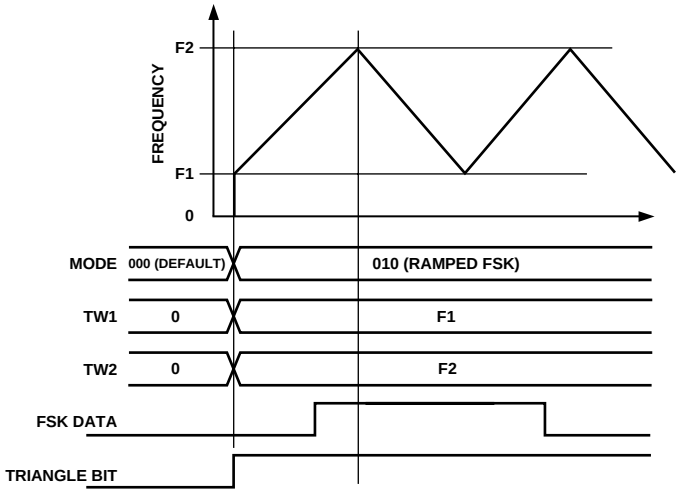



*Figure 42. Automatic Linear Ramping Using the Triangle Bit*

Additional flexibility in the ramped FSK mode is provided in the ability to respond to changes in the 48-bit delta frequency word and/or the 20-bit ramp-rate counter on-the-fly *during* the ramping from F1 to F2 or vice versa. To create these nonlinear frequency changes it is necessary to combine several linear ramps in a piecewise fashion whose slopes are different. This is done by programming and executing a linear ramp at some rate or "slope" and then altering the slope (by changing the ramp rate clock or delta frequency word or both). Changes in slope are made as often as needed to form the desired nonlinear frequency sweep response *before* the destination frequency has been reached. These piecewise changes can be precisely timed using the 32-bit Internal Update Clock (see detailed description elsewhere in this data sheet).

Nonlinear ramped FSK will have the appearance of a chirp function that is graphically illustrated in Figure 43. The major difference between a ramped FSK function and a chirp function is that FSK is limited to operation between F1 and F2. Chirp operation has no F2 limit frequency.

Two additional control bits are available in the ramped FSK mode that allow even more options. CLR ACC1, register address 1F hex, will, if set high, clear the 48-bit *frequency accumulator* (ACC1) output with a retriggerable one-shot pulse of one system clock duration. If the CLR ACC1 bit is left high, a one-shot pulse will be delivered on the rising edge of every Update Clock. The effect is to interrupt the current ramp, reset the frequency back to the start point, F1 or F2, and then continue to ramp up (or down) at the previous rate. This will occur even when a static F1 or F2 destination frequency has been achieved. (See Figure 43.)

Next, CLR ACC2 control bit (register address 1F hex) is available to clear both the *frequency accumulator* (ACC1) and the *phase accumulator* (ACC2). When this bit is set high, the output of the phase accumulator will result in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators will be cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low.

**Chirp (Mode 011)**

This mode is also known as pulsed FM. Most chirp systems use a linear FM sweep pattern although any pattern may be used. This is a type of spread spectrum modulation that can realize "processing gain." In radar applications, use of chirp or pulsed FM allows operators to significantly reduce the output power needed to achieve the same result as a single-frequency radar system would produce. Figure 43 represents a very low-resolution nonlinear chirp meant to demonstrate the different "slopes" that are created by varying the time steps (ramp rate) and frequency steps (delta frequency word).

The AD9852 permits precise, internally generated linear or externally programmed nonlinear pulsed or continuous FM over a user-defined frequency range, duration, frequency resolution and sweep direction(s). A block diagram of the FM chirp components is shown in Figure 44.

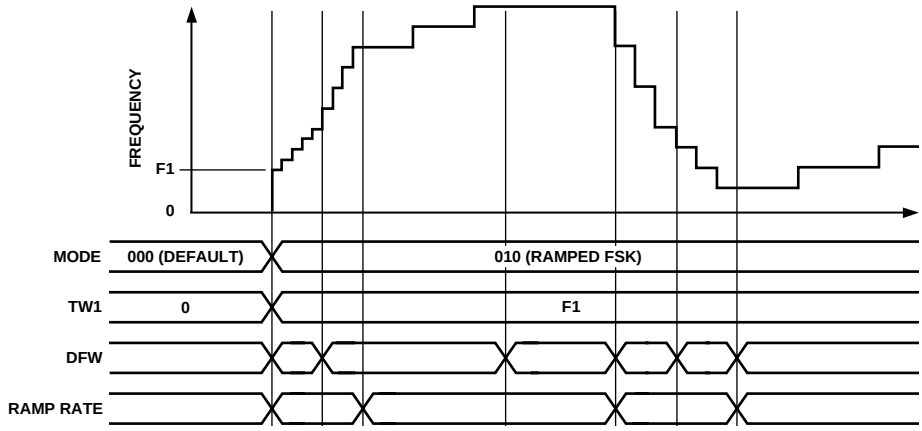



*Figure 43. Example of a Nonlinear Chirp*

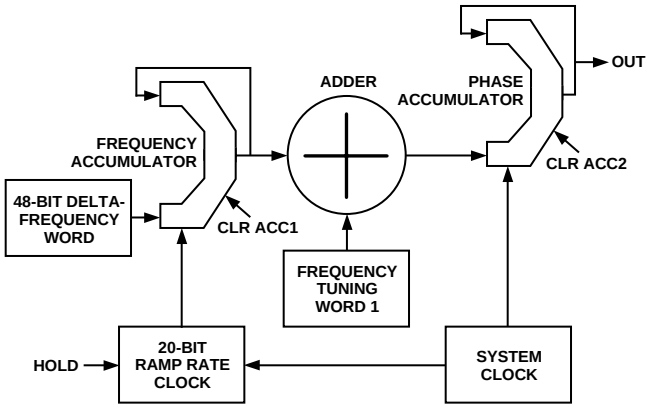



*Figure 44. FM Chirp Components*

**Basic FM Chirp Programming Steps**

1. Program a start frequency into Frequency Tuning Word 1 (parallel register addresses 4–9 hex) hereafter called FTW1.
2. Program the frequency step resolution into the 48-bit, *twos complement,* Delta Frequency Word (parallel register addresses 10–15 hex).
3. Program the rate of change (time at each frequency) into the 20-bit Ramp Rate Clock (parallel register addresses 1A–C).
4. When programming is complete, an I/O update pulse at Pin 20 will engage the program commands.

The necessity for a twos complement Delta Frequency Word is to define the direction in which the FM chirp will move. If the 48-bit delta frequency word is negative (MSB is high), the incremental frequency changes will be in a negative direction from FTW1. If the 48-bit word is positive (MSB is low), the incremental frequency changes will be in a positive direction.

It is important to note that the FTW1 is only a starting point for FM chirp. There is no built-in restraint requiring a return to FTW1. Once the FM chirp has left FTW1 it is free to move (under program control) within the Nyquist bandwidth (dc to 1/2 system clock). *Instant* return to FTW1 is easily achieved, though, and this option is explained in the next few paragraphs.

Two control bits are available in the FM Chirp mode that will allow practically instantaneous return to the beginning frequency, FTW1, or to 0 Hz. First, CLR ACC1 bit, register address 1F hex will, if set high, clear the 48-bit *frequency accumulator* (ACC1) *output* with a retriggerable one-shot pulse of one system clock duration. The 48-bit Delta Frequency Word input to the accumulator is unaffected by CLR ACC1 bit. If the CLR ACC1 bit is left high, a one-shot pulse will be delivered to the Frequency Accumulator (ACC1) on every rising edge of the I/O Update Clock. The effect is to interrupt the current chirp, reset the frequency back to FTW1, and continue the chirp at the previously programmed rate and direction. Clearing the Frequency Accumulator in the chirp mode is illustrated in Figure 45. Not shown in the diagram is the I/O update signal, which is either user-supplied or internally generated. A discussion of I/O Update is presented elsewhere in this data sheet.

Next, CLR ACC2 control bit (register address 1F hex) is available to clear both the *frequency accumulator* (ACC1) and the *phase accumulator* (ACC2). When this bit is set high, the output of the phase accumulator will result in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators will be cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low. This bit is useful in generating pulsed FM.

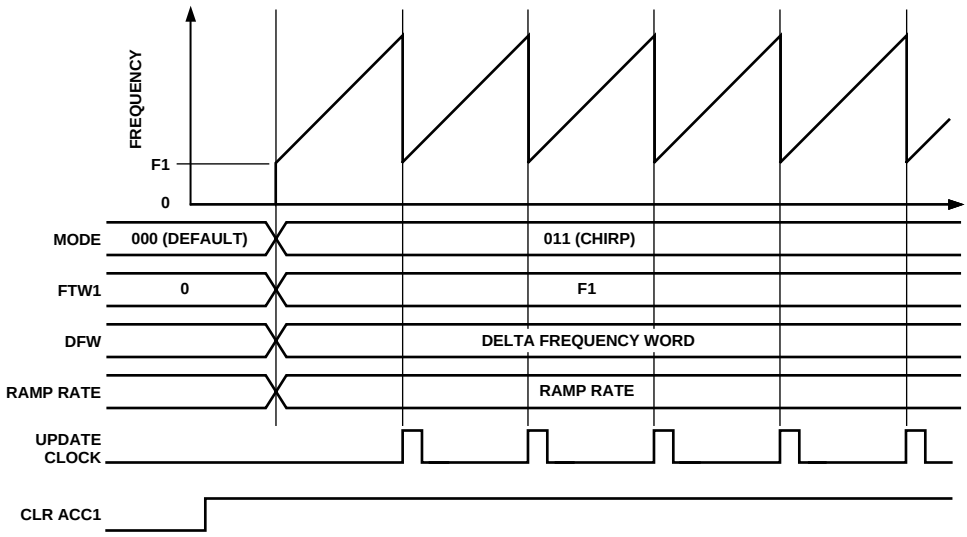



*Figure 45. Effect of CLR ACC1 in FM Chirp Mode*

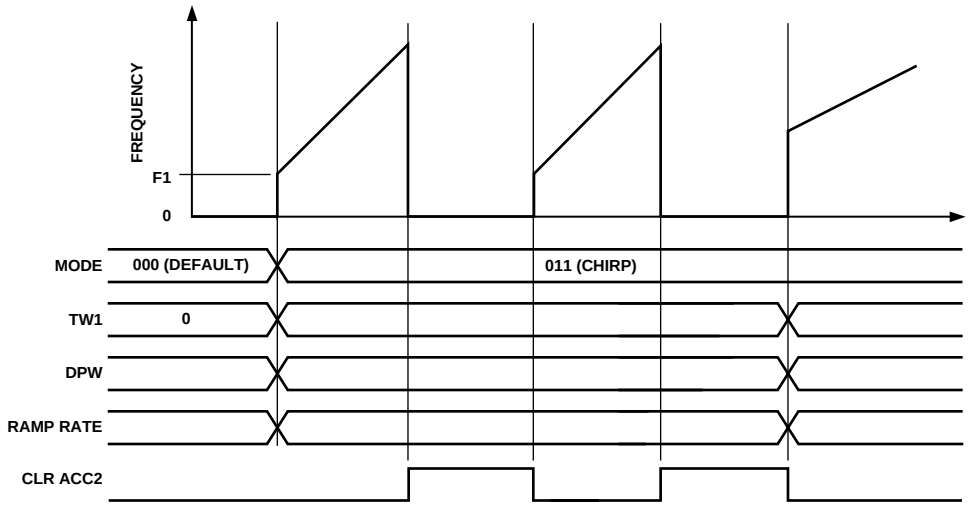



*Figure 46. Effect of CLR ACC2 in FM Chirp Mode*

**FM Chirp**

Figure 46 graphically illustrates the effect of CLR ACC2 bit upon the DDS output frequency. Note that reprogramming the registers while the CLR ACC2 bit is high allows a new FTW1 frequency and slope to be loaded.

Another function available only in the chirp mode is the HOLD pin, Pin 29. This function will stop the clocking signal to the ramp rate counter that will, in turn, halt any further clocking pulses to the frequency accumulator, ACC1. The effect is to halt the chirp and hold the output frequency in a static condition at the frequency existing just before HOLD was pulled high. When the HOLD pin is returned low, the clocks are resumed and chirp continues. During a hold condition, user may change the programming registers; however, the ramp rate counter must resume operation at its previous rate until a count of zero is obtained before a new ramp rate count can be loaded. Figure 47 illustrates the effect of the hold function on the DDS output frequency.

Users may utilize the 32-bit automatic I/O Update counter when constructing complex chirp or ramped FSK sequences. Since this internal counter is synchronized with the AD9852 System Clock, it allows precisely timed program changes to be invoked. In this manner, user is only required to reprogram the desired registers before the automatic I/O Update pulse is generated. A complete discussion of this function is presented elsewhere in this data sheet.

In the chirp mode, the destination frequency is not directly specified. If the user fails to control the chirp, the DDS will control itself by naturally confining its output between dc and Nyquist; however, unless terminated by the user, the chirp will continue until power is removed.

It is the user's choice as to what occurs when the chirp destination frequency is reached. Here are a few of the choices:

1. Stop and hold at the destination frequency using the HOLD pin, or by loading all zeros into the Delta Frequency Word registers of the frequency accumulator (ACC1).
2. Stop using the hold pin function, then ramp-down the output amplitude using the digital multiplier stages and the Shaped Keying pin, Pin 30, or via program register control (addresses 21–24 hex).
3. Stop and abruptly terminate the transmission using the CLR ACC2 bit.

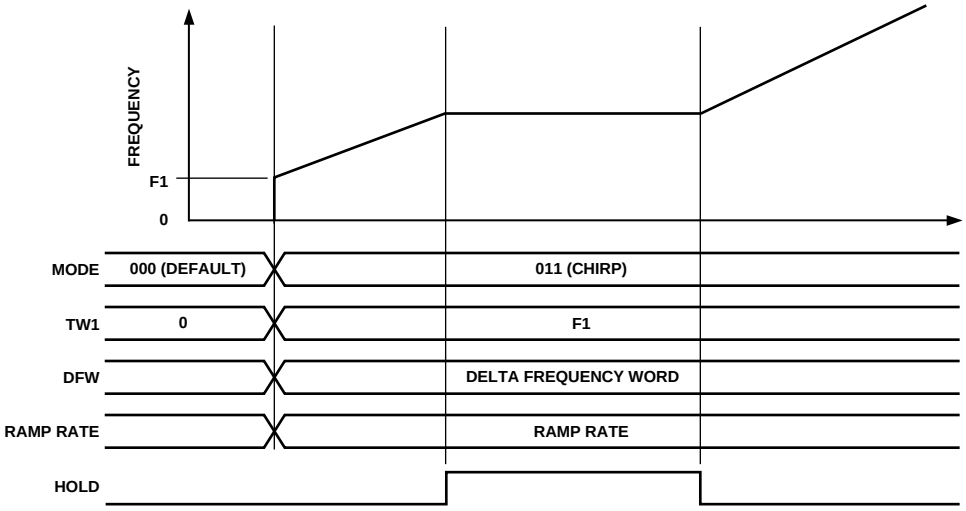



*Figure 47. Illustration of HOLD Function*

4. Continue chirp by reversing direction and returning to the previous, or another, destination frequency in a linear or user-directed manner. If this involves going down in frequency, a negative 48-bit Delta Frequency Word (the MSB is set to "1") must be loaded into registers 10–15 hex. Any decreasing frequency step of the Delta Frequency Word requires the MSB to be set to logic high.
5. Continue chirp by immediately returning to the F1 beginning frequency in a sawtooth fashion and repeat the previous chirp process again. This is where CLR ACC1 control bit is used. An automatic, repeating chirp can be setup using the 32-bit Update Clock to issue CLR ACC1 commands at precise time intervals. Adjusting the timing intervals or changing the Delta Frequency Word will change the chirp range. It is incumbent upon the user to balance the chirp duration and frequency resolution to achieve the proper frequency range.

**BPSK (Mode 100)**

Binary, biphase, or bipolar phase shift keying is a means to rapidly select between two preprogramming 14-bit output phase offsets that will identically affect both the I and Q outputs of the AD9852. The logic-state of Pin 29, BPSK pin, controls the selection of Phase Adjust register number 1 or 2. When low, Pin 29 selects Phase Adjust register 1; when high, Phase Adjust register 2 is selected. Figure 48 illustrates phase changes made to four cycles of an output carrier.

Basic BPSK programming steps:

1. Program a carrier frequency into Frequency Tuning Word 1.
2. Program appropriate 14-bit phase words in Phase Adjust registers 1 and 2.
3. Attach BPSK data source to Pin 29.
4. Activate I/O Update pulse when ready.

If phase shift keying is not the objective, but rather a broader range of phase offsets is needed, the user should select the Single-Tone mode and program Phase Adjust register 1 using the serial or high-speed parallel programming bus.

***I/O Port Buffers***—100 MHz, 8-bit parallel or 10 MHz serial loading, SPI-compatible. The programming mode is selected externally via the serial/parallel (S/P Select) pin. I/O Buffers can be written to, or read from, according to the signals supplied to the Read (RDB) and Write pins (WRB) and the 6-bit address (A0–A5) in the parallel mode or to CSB, SCLK and SDIO pins in the Serial mode.

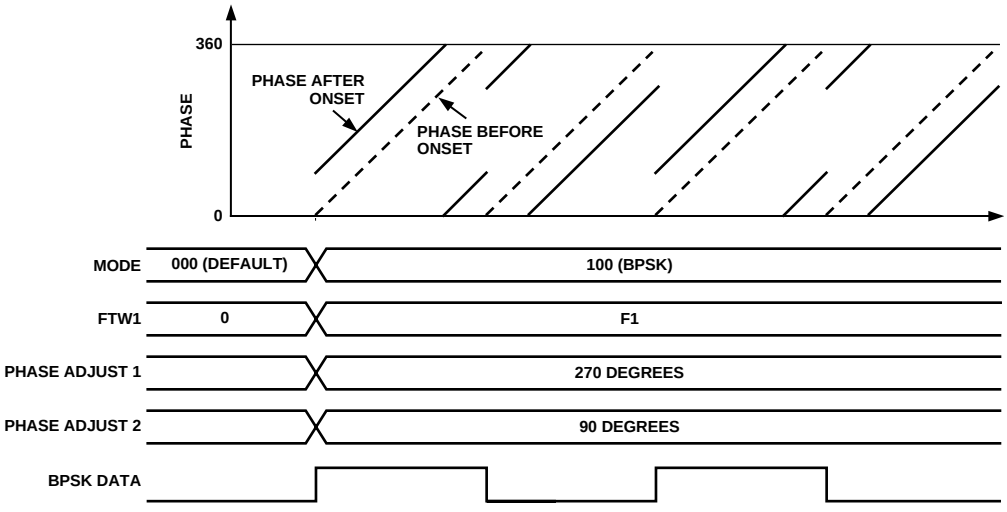



*Figure 48. BPSK Mode*

Data in the I/O Port Buffers is stored until overwritten by changes in program instructions supplied by the user or until power is removed. An I/O Update clocks-in the data from the I/O Buffers to the DDS Programming Registers where it is executed.

***AM***—amplitude modulation of the sine DACs is possible using the I/O port to control 12-bit digital multiplier stages that precede the DACs. The multipliers can also be used to set the DAC outputs between zero- and full-scale for static amplitude adjustment. See the "Shaped On/Off Keying" description for more information. Shaped keying function does not apply to the Control DAC.

***High-Speed Comparator***—optimized for high speed, >300 MHz toggle rate, low jitter, sensitive input, built-in hysteresis and an output level of 1 V p-p minimum into 50 Ω or CMOS logic levels into high impedance loads. The comparator can be separately powered down to conserve power. This comparator is used in "clock generator" applications to square up a bandpass or low-pass filtered sine wave.

***Eight-Bit Ramp Rate Clock***—when Shaped On/Off Keying is engaged, this down-counter takes the system clock (300 MHz maximum), and divides it by an 8-bit binary value (programmed by the user) to produce a user-defined clock. The clock outputs one pulse every time the counter counts down to zero. This clock is used to set the rate-of-change of the 12-bit digital multipliers of the I and Q DACs to perform an output shaping function.

***Twenty-Bit Ramp Rate Clock***—when selected, this down-counter takes the system clock (300 MHz maximum) and divides it by a 20-bit binary value (programmed by the user) to produce a user-defined clock. The clock outputs one pulse every time the counter counts down to zero. This clock is used to set the rate-of-frequency-change of the ramped FSK or FM Chirp modes.

***Forty-Eight-Bit Delta Frequency Register***—is used only in the Chirp and ramped-FSK modes. This register is loaded with a 48-bit word that represents the frequency increment value of Frequency Accumulator (ACCU 1) whose output will be added to a frequency that is set in either F1 or F2 frequency registers. This register is periodically incremented at a rate set by the 20-bit ramp rate clock (150 MHz maximum).

***Forty-Eight-Bit Delta Frequency Register***—is programmed with a 48-bit Frequency Tuning Word that is input to the 48-bit Phase Accumulator (ACCU 2) and determines the output frequency of the DDS in the single-tone mode. When ramped-FSK or Chirp are selected, this register is sent to a digital adder where it is summed with the output of ACCU 1 before being input to ACCU 2. Therefore, the signal sent to ACCU 2 may be either static or changing at a rate of up to 150 million 48-bit frequency tuning words per second.

***Power-Down***—Several individual stages, when not needed, can be powered down to reduce power consumption via the programming registers while still maintaining functionality of desired stages. These stages are identified in the Register Layout table, address 1D hex. Power-down is achieved by setting the specified bits to logic high. A logic low indicates that the stages are powered up.

Furthermore, and perhaps most significantly, two intensely digital stages, the Inverse Sinc filters and the Digital Multiplier stages, can be bypassed to achieve significant power reduction through programming of the control registers in address 20 hex. Again, logic high will cause the stage to be bypassed. Of particular importance is the Inverse Sinc filter as this stage consumes a significant amount of power.

A full power-down occurs when all four $\overline{\text{PD}}$ Bits in control register 1D hex are set to logic high. This reduces power consumption to approximately 10 mW (3 mA).

***Master RESET***—logic high active, must be held high for a minimum of 10 system clock cycles. This causes the communications bus to be initialized and loads default values listed in the Table V.

**Table V. Register Layout. Shaded Sections Comprise the Control Register**

| Parallel Address | Serial Address | AD9852 Register Layout | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Hex | Hex | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default Value |
| 00<br>01 | 0 | Phase Adjust Register #1 <13:8> (Bits 15, 14 don't care)<br>Phase Adjust Register #1 <7:0> | | | | | Phase 1 | | | 00h<br>00h |
| 02<br>03 | 1 | Phase Adjust Register #2 <13:8:> (Bits 15, 14 don't care)<br>Phase Adjust Register #2 <7:0> | | | | | Phase 2 | | | 00h<br>00h |
| 04<br>05<br>06<br>07<br>08<br>09 | 2 | Frequency Tuning Word 1 <47:0><br>Frequency Tuning Word 1 <39:32><br>Frequency Tuning Word 1 <31:24><br>Frequency Tuning Word 1 <23:16><br>Frequency Tuning Word 1 <15:8><br>Frequency Tuning Word 1 <7:0> | | | | | Frequency 1 | | | | 00h<br>00h<br>00h<br>00h<br>00h<br>00h |
| 0A<br>0B<br>0C<br>0D<br>0E<br>0F | 3 | Frequency Tuning Word 2 <47:40><br>Frequency Tuning Word 2 <39:32><br>Frequency Tuning Word 2 <31:24><br>Frequency Tuning Word 2 <23:16><br>Frequency Tuning Word 2 <15:8><br>Frequency Tuning Word 2 <7:0> | | | | | Frequency 2 | | | 00h<br>00h<br>00h<br>00h<br>00h<br>00h |
| 10<br>11<br>12<br>13<br>14<br>15 | 4 | Delta Frequency Word <47:40><br>Delta Frequency Word <39:32><br>Delta Frequency Word <31:24><br>Delta Frequency Word <23:16><br>Delta Frequency Word <15:8><br>Delta Frequency Word <7:0> | | | | | | | | 00h<br>00h<br>00h<br>00h<br>00h<br>00h |
| 16<br>17<br>18<br>19 | 5 | Update Clock <31:24><br>Update Clock <23:16><br>Update Clock <15:8><br>Update Clock <7:0> | | | | | | | | 00h<br>00h<br>00h<br>40h |
| 1A<br>1B<br>1C | 6 | Ramp Rate Clock <19:16> (Bits 23, 22, 21, 20 don't care)<br>Ramp Rate Clock <15:8><br>Ramp Rate Clock <7:0> | | | | | | | | 00h<br>00h<br>00h |
| 1D<br><br>1E | 7 | Don't Care | Don't Care | Don't Care | Comp PD | Reserved, Always Low | Control DAC PD | DAC PD | DIG PD | 00h |
| 1F | | Don't Care | PLL Range | Bypass PLL | Ref Mult 4 | Ref Mult 3 | Ref Mult 2 | Ref Mult 1 | Ref Mult 0 | 64h |
| 20 | | CLR ACC 1 | CLR ACC 2 | Triangle | Don't Care | Mode 2 | Mode 1 | Mode 0 | Int Update Clk | 01h |
| | | Don't Care | Bypass Inv Sinc | OSK EN | OSK INT | Don't Care | Don't Care | LSB First | SDO Active | 20h |
| 21<br>22 | 8 | Output Shape Key I Mult <11:8> (Bits 15, 14, 13, 12 don't care)<br>Output Shape Key I Mult <7:0> | | | | | | | | 00h<br>00h |
| 23<br>24 | 9 | Output Shape Key Q Mult <11:8> (Bits 15, 14, 13, 12 don't care)<br>Output Shape Key Q Mult <7:0> | | | | | | | | 00h<br>00h |
| 25 | A | Output Shape Key Ramp Rate <7:0> | | | | | | | | 80h |
| 26<br>27 | B | QDAC <11:8> (Bits 15, 14, 13, 12 don't care)<br>QDAC <7:0> (Data is required to be in twos-complement format) | | | | | | | | 00h<br>00h |

**Interfacing and Programming the AD9852**

The AD9852 Register Layout, shown in Table V, contains the information that programs the chip for the desired functionality. While many applications will require very little programming to configure the AD9852, some will make use of all twelve accessible register banks. The AD9852 supports an 8-bit byte parallel I/O operation or an SPI-compatible serial I/O operation. All accessible registers can be written and read back in either I/O operating mode.

An external pin, S/P SELECT, is used to configure the I/O mode. Systems that use the parallel I/O mode must connect the S/P SELECT pin to $V_{DD}$. Systems that operate in the serial I/O mode must tie the S/P SELECT pin to GND.

Regardless of mode, the I/O port data is written to a buffer memory that does NOT affect operation of the part until the contents of the buffer memory are transferred to the register banks. This transfer of information occurs, synchronously, to the system clock and occurs in one of two ways:

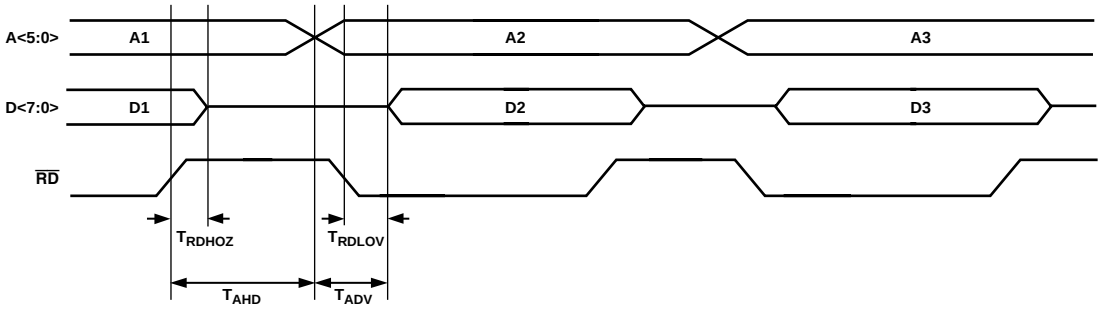
1. Internally, controlled at a rate programmable by the user or,
2. Externally, controlled by the user. I/O operations can occur in the absence of REFCLK but the data cannot be moved from the buffer memory to the register bank without REFCLK. See the Update Clock Operation section of this document for details.

**Parallel I/O Operation**

With the S/P SELECT pin tied high, the parallel I/O mode is active. The I/O port is compatible with industry standard DSPs and microcontrollers. Six address bits, eight bidirectional data bits and separate write/read control inputs make up the I/O port pins.

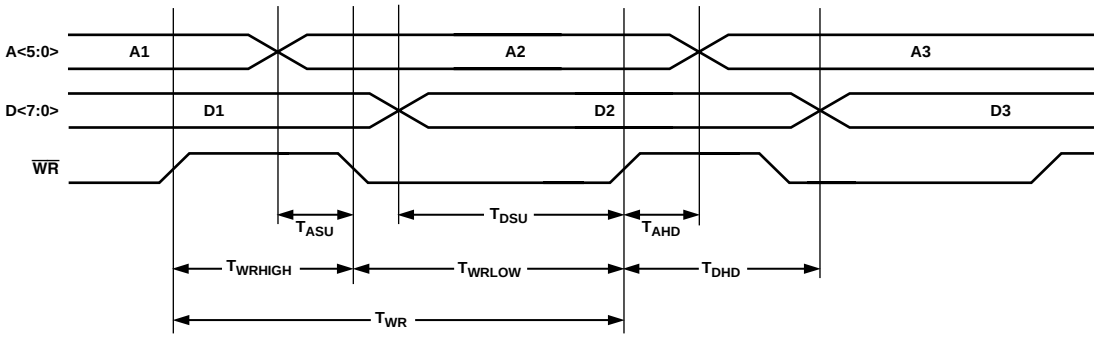
Parallel I/O operation allows write access to each byte of any register in a single I/O operation at 100 MHz. Readback capability for each register is included to ease designing with the AD9852. Reads are not guaranteed at 100 MHz as they are intended for software debug only.

Parallel I/O operation timing diagrams are shown in the Figures 49 and 50.




| SPECIFICATION | VALUE | DESCRIPTION |
|---|---|---|
| $T_{ADV}$ | 15 | ADDRESS TO DATA VALID TIME (MAXIMUM) |
| $T_{AHD}$ | 5 | ADDRESS HOLD TIME TO RD SIGNAL INACTIVE (MINIMUM) |
| $T_{RDLOV}$ | 15 | $\overline{RD}$ LOW TO OUTPUT VALID (MAXIMUM) |
| $T_{RDHOZ}$ | 10 | $\overline{RD}$ HIGH TO DATA THREE-STATE (MAXIMUM) |

*Figure 49. Parallel Port Read Timing Diagram*




| SPECIFICATION | VALUE | DESCRIPTION |
|---|---|---|
| $T_{ASU}$ | 4ns | ADDRESS SETUP TIME TO $\overline{WR}$ SIGNAL ACTIVE |
| $T_{DSU}$ | 2ns | DATA SETUP TIME TO $\overline{WR}$ SIGNAL INACTIVE |
| $T_{ADH}$ | 5ns | ADDRESS HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE |
| $T_{DHD}$ | 0ns | DATA HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE |
| $T_{WRLOW}$ | 3ns | $\overline{WR}$ SIGNAL MINIMUM LOW TIME |
| $T_{WRHIGH}$ | 7ns | $\overline{WR}$ SIGNAL MINIMUM HIGH TIME |
| $T_{WR}$ | 3ns | $\overline{WR}$ SIGNAL MINIMUM PERIOD |

*Figure 50. Parallel Port Write Timing Diagram*

**Serial Port I/O Operation**

With the S/P SELECT pin tied low, the serial I/O mode is active. The AD9852 serial port is a flexible, synchronous, serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols. The interface allows read/write access to all twelve registers that configure the AD9852 and can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO). Data transfers are supported in most significant bit (MSB) first format or least significant bit (LSB) first format at up to 10 MHz.

When configured for serial I/O operation, most pins from the AD9852 parallel port are inactive; some are used for the serial I/O. Table VI describes pin requirements for serial I/O.

**Table VI. Serial I/O Pin Requirements**

| Pin Number | Pin Name | Serial I/O Description |
|---|---|---|
| 1, 2, 3, 4, 5, 6, 7, 8 | D[7:0] | The parallel data pins are not active, tie to VDD or GND. |
| 14, 15, 16 | A[5:3] | The parallel address Pins A5, A4, A3 are not active, tie to VDD or GND. |
| 17 | A2 | IORESET |
| 18 | A1 | SDO |
| 19 | A0 | SDIO |
| 20 | I/O UD | Update Clock. Same functionality for Serial Mode as Parallel Mode. |
| 21 | WRB | SCLK |
| 22 | RDB | CSB—Chip Select |

**GENERAL OPERATION OF THE SERIAL INTERFACE**

There are two phases to a communication cycle with the AD9852. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9852, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9852 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, and the register address in which to transfer data to/from.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9852. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9852 and the system controller. The number of data bytes transferred in Phase 2 of the communication cycle is a function of the register address. The AD9852 internal serial I/O controller expects every byte of the register being accessed to be transferred. Table VII describes how many bytes must be transferred.

**Table VII. Register Address vs. Data Bytes Transferred**

| Serial Register Address | Register Name | Number of Bytes Transferred |
|---|---|---|
| 0 | Phase Offset Tuning Word Register #1 | 2 Bytes |
| 1 | Phase Offset Tuning Word Register #2 | 2 Bytes |
| 2 | Frequency Tuning Word #1 | 6 Bytes |
| 3 | Frequency Tuning Word #2 | 6 Bytes |
| 4 | Delta Frequency Register | 6 Bytes |
| 5 | Update Clock Rate Register | 4 Bytes |
| 6 | Ramp Rate Clock Register | 3 Bytes |
| 7 | Control Register | 4 bytes |
| 8 | I Path Digital Multiplier Register | 2 Bytes |
| 9 | Q Path Digital Multiplier Register | 2 Bytes |
| A | Shaped On/Off Keying Ramp Rate Register | 2 Bytes |
| B | Q DAC Register | 2 Bytes |

At the completion of any communication cycle, the AD9852 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle. In addition, an active high input on the IORESET pin immediately terminates the current communication cycle. After IORESET returns low, the AD9852 serial port controller requires the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9852 is registered on the rising edge of SCLK. All data is driven out of the AD9852 on the falling edge of SCLK.

Figures 51 and 52 are useful in understanding the general operation of the AD9852 Serial Port.

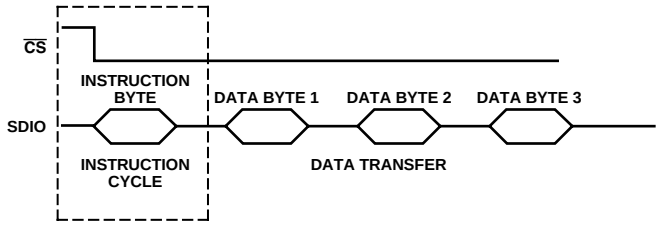



*Figure 51. Using SDIO as a Read/Write Transfer*

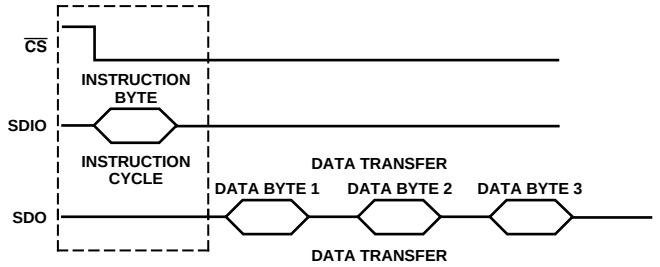



*Figure 52. Using SDIO as an Input, SDO as an Output*

**Instruction Byte**

The instruction byte contains the following information.

**Table VIII. Instruction Byte Information**

| MSB | D6 | D5 | D4 | D3 | D2 | D1 | LSB |
|---|---|---|---|---|---|---|---|
| R/$\overline{W}$ | X | X | X | A3 | A2 | A1 | A0 |

***R/$\overline{W}$***—Bit 7 of the instruction byte determines whether a read or write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic zero indicates a write operation.

Bits 6, 5, and 4 of the instruction byte are don't care.

A3, A2, A1, A0—Bits 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. See Table VIII for register address details.

## SERIAL INTERFACE PORT PIN DESCRIPTION

**SCLK**

Serial Clock (Pin 21). The serial clock pin is used to synchronize data to and from the AD9852 and to run the internal state machines. SCLK maximum frequency is 10 MHz.

**$\overline{CS}$**

Chip Select (Pin 22). Active low input that allows more than one device on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

**SDIO**

Serial Data I/O (Pin 19). Data is always written into the AD9852 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 0 of register address 20h. The default is logic zero, which configures the SDIO pin as bidirectional.

**SDO**

Serial Data Out (Pin 18). Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9852 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

**IO RESET**

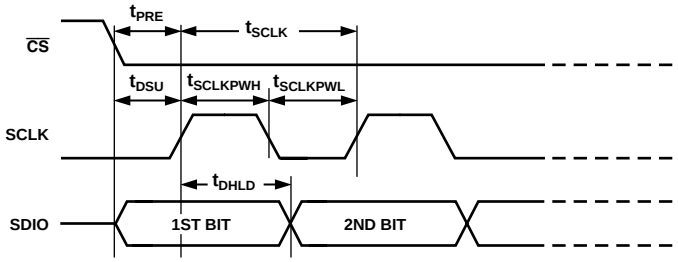
Synchronize I/O Port (Pin 17). Synchronizes the I/O port state machines without affecting the addressable registers contents. An active high input on IO RESET pin causes the current communication cycle to terminate. After IO RESET returns low (Logic 0) another communication cycle may begin, starting with the instruction byte write.

## NOTES ON SERIAL PORT OPERATION

The AD9852 serial port configuration bits reside in Bits 1 and 0 of register address 20h. It is important to note that the configuration changes *immediately* upon a valid I/O update. For multibyte transfers, writing this register may occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remainder of the current communication cycle.

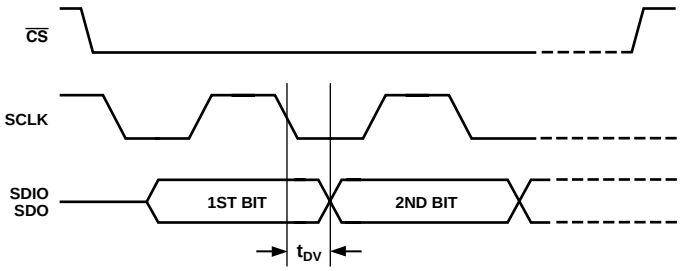
The system must maintain synchronization with the AD9852 or the internal control logic will not be able to recognize further instructions. For example, if the system sends the instruction to write a 2-byte register, then pulses the SCLK pin for a 3-byte register (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9852, but the next eight rising SCLK edges are interpreted as the next instruction byte, NOT the final byte of the previous communication cycle.

In the case where synchronization is lost between the system and the AD9852, the IO RESET pin provides a means to reestablish synchronization without reinitializing the entire chip. Asserting the IO RESET pin (active high) resets the AD9852 serial port state machine, terminating the current IO operation and putting the device into a state in which the next eight SCLK rising edges are understood to be an instruction byte. The SYNC IO pin must be deasserted (low) before the next instruction byte write can begin. Any information that had been written to the AD9852 registers during a valid communication cycle prior to loss of synchronization will remain intact.




| SYMBOL | MIN | DEFINITION |
|---|---|---|
| $T_{PRE}$ | 30ns | $\overline{CS}$ SETUP TIME |
| $T_{SCLK}$ | 100ns | PERIOD OF SERIAL DATA CLOCK |
| $T_{DSU}$ | 30ns | SERIAL DATA SETUP TIME |
| $T_{SCLKPWH}$ | 40ns | SERIAL DATA CLOCK PULSEWIDTH HIGH |
| $T_{SCLKPWL}$ | 40ns | SERIAL DATA CLOCK PULSEWIDTH LOW |
| $T_{DHLD}$ | 0ns | SERIAL DATA HOLD TIME |

*Figure 53. Timing Diagram for Data Write to AD9852*




| SYMBOL | MAX | DEFINITION |
|---|---|---|
| $T_{DV}$ | 30ns | DATA VALID TIME |

*Figure 54. Timing Diagram for Read from AD9852*

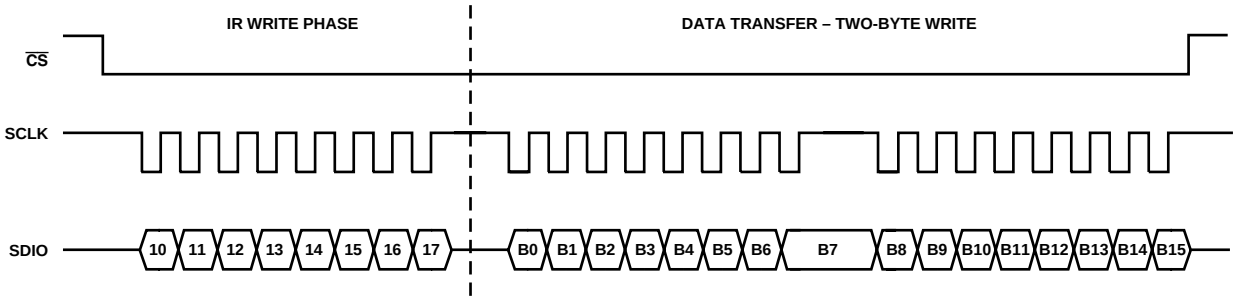



*Figure 55. Data Write Cycle, SCLK Idle High*

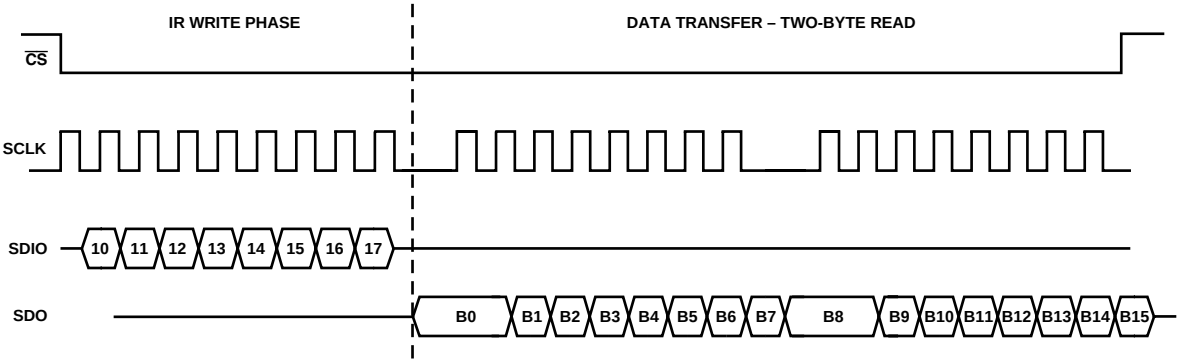



*Figure 56. Data Read Cycle, 3-Wire Configuration, SCLK Idle Low*

**MSB/LSB TRANSFERS**

The AD9852 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by Bit 1 of serial register bank 20h. When this bit is set active high, the AD9852 serial port is in LSB first format. This bit defaults low, to the MSB first format. The instruction byte must be written in the format indicated by Bit 1 of serial register bank 20h. That is, if the AD9852 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

**Update Clock Operation**

Programming the AD9852 is asynchronous to the system clock with all data being stored in a buffer memory that does not immediately affect the part operation. The buffer memory is transferred to the register bank synchronous to system clock. The register bank information affects part operation.

This transfer of data can occur automatically, with frequency of updates programmable by the user, or can occur completely under user control.

Complete user control, referred to as external update mode, allows the user to drive the I/O UD signal from their ASIC or DSP. The AD9852 I/O UD pin is configured as an input in external update mode. A rising edge on I/O UD indicates to the AD9852 that the contents of the buffer memory is to be transferred to the register bank. The design uses an edge detector to signal the AD9852 to transfer data which allows a very small minimum high pulse width requirement (two system clock periods). Its important to note that if the user keeps I/O UD high, the AD9852 will NOT continuously update the register bank.

Internal update mode, in which the AD9852 transfers data from the buffer memory to the register bank automatically, configures the AD9852 I/O UD pin as an output. The AD9852 generates a high pulse on I/O UD pin to signal the user that the buffer memory has just been transferred to the register bank. The minimum high pulsewidth is designed to be eight system clock cycles (min). The I/O UD signal can be used as an interrupt within the system. Its important to note that as an output I/O UD pin will not have anything approaching a 50/50 duty cycle for slower update rates.

Programming the Update Clock register for values less than five will cause the I/O UD pin to remain high. The update clock functionality still works, its just that the user cannot use the signal as an indication that data is transferring. This is an affect of the minimum high pulse time when I/O UD is an output.

For internal update clock operation, the rate which the updates occur is programmed into the update clock register. The update clock register is 32 bits and the value written into the register corresponds to HALF the number of clock cycles between updates. That is, if a value of 00_00_00_0A (hex), is written into the update clock register the rising edge of the I/O UD pin will occur every 20 cycles (0A hex equals 10 decimal).

**CONTROL REGISTER**

The Control Register is located in the shaded portion of the Table V at address 1D through 20 hex. It is composed of 32 bits. Bit 31 is located at the top left position and Bit 0 is located in the lower right position of the shaded table portion. The register has been subdivided below to make it easier to locate the text associated with specific control categories.

**Power-Down Functions**
Four bits are available to power down the AD9852. Each bit is active high, that is, they default low and a Logic 1 causes the power-down function to be working, The four bits all reside in the same control byte such that one IO write cycle can complete a full power-down by writing all four bits true simultaneously. The four bits are located in Control Register [28, 26:24] and are described below. The default state for these bits is Logic 0, inactive.

CR[31:29] are open.

CR[28] is the comparator power-down bit. When set (Logic 1), this signal indicates to the comparator that a power-down mode is active.

CR[27] must always be written to logic zero. Writing this bit to Logic 1 causes the AD9852 to stop working until a master reset is applied.

CR[26] is the Control DAC power-down bit. When set (Logic 1), this signal indicates to the Control DAC that a power-down mode is active.

CR[25] is the full DAC power-down bit. When set (Logic 1), this signal indicates to both the cosine and Control DACs, as well as the reference, that a power-down mode is active.

CR[24] is the digital power-down bit. When set (Logic 1), this signal indicates to the digital section that a power-down mode is active. Within the digital section, the clocks will be forced to dc, effectively powering down the digital section. The REFCLK input will still be seen by the PLL and the PLL will continue to output the higher frequency.

**REFCLK Multiplier PLL Functions**
Seven control register bits, located in the Control Register [22:16] positions, relate to the PLL.

CR[23] is reserved, write to zero.

CR[22] is the PLL range bit. The PLL range bit controls the VCO gain. The power-up state of the PLL range bit is Logic 1, higher gain for frequencies above 200 MHz.

CR[21] is the bypass PLL bit, active high. When active, the PLL is powered down and the REFCLK input is used to drive the system clock signal. The power-up state of the bypass PLL bit is Logic 1, PLL bypassed.

CR[20:16] bits are the PLL multiplier factor. These bits are the REFCLK multiplication factor unless the bypass PLL bit is set. The PLL multiplier valid range is from 4 to 20, inclusive.

**Other Operational Functions**
CR[15] is the clear accumulator 1 bit. This bit has a one-shot type function. When written active, Logic 1, a clear accumulator 1 signal is sent to the DDS logic, resetting the accumulator value to zero. The bit is then automatically reset, but the buffer memory is not reset. This bit allows the user to easily create a sawtooth frequency sweep pattern with very little (or no) user input required. This bit is intended for chirp mode only, but there is no logic to suppress its functionality in other modes.

CR[14] is the clear accumulator bit. This bit, active high, holds both the accumulator 1 and accumulator 2 values at zero for as long as the bit is active. This allows the DDS phase to be initialized via the I/O port.

CR[13] is the triangle bit. When this bit is set, the AD9852 will automatically perform a continuous frequency sweep from the Frequency 1 to Frequency 2 and back. The effect is a triangular frequency sweep. When this bit is set, the operating mode must be set to ramped FSK.

CR[11:9] are the three bits that describe the five operating modes of the AD9852:

0h = Single-Tone Mode
1h = FSK Mode
2h = Ramped FSK mode
3h = Chirp Mode
4h = PSK Mode

CR[8] is the internal update active bit. When this bit is set to Logic 1, the I/O UD pin is an output and the AD9852 generates the I/O UD signal. When Logic 0, external I/O UD functionality is performed, the I/O UD pin is configured as an input.

CR[7] reserved, write to zero.

CR[6] is the bypass of the inverse sinc filter bit. When set, the data from the DDS block goes directly to the shaped keying logic and the clock to the inverse sinc filter is stopped. Default is clear, filter enabled.

CR[5] is the shaped keying enable bit. When set the output ramping function is enabled and is performed in accordance with the CR[4] bit requirements.

CR[4] is the internal/external shaped keying control bit. When set Logic 1, the shaped keying factor will be internally generated and applied to the I path. When clear, the shaped keying function is externally controlled by the user and the shaped keying factor is the I output shaped keying register values. The two registers that are the ramp factors also default low such that the output is off at power-up and until the device is programmed by the user.

CR[3:2] reserved, write to zero.

CR[1] is the serial port MSB/LSB first bit. Defaults low, MSB first.

CR[0] is the serial port SDO active bit. Defaults low, inactive.

## POWER DISSIPATION AND THERMAL CONSIDERATIONS

The AD9852 is a multifunctional, very high-speed device that targets a wide variety of synthesizer and agile clock applications. The set of numerous innovative features contained in the device each consume incremental power, the sum of which, if enabled in combination, may exceed the safe thermal operating conditions of the device. Careful analysis and consideration of power dissipation and thermal management is a critical element in the successful application of the AD9852 device.

The AD9852 device is specified to operate within the industrial temperature range of –40°C to +85°C. This specification is conditional, however, such that the absolute maximum junction temperature of 150°C is not exceeded. At high operating temperatures, extreme care must be taken in the operation of the device to avoid exceeding the junction temperature which results in a potentially damaging thermal condition.

Many variables contribute to the operating junction temperature within the device, including:

1. Package Style
2. Selected Mode of Operation
3. Internal System Clock Speed
4. Supply Voltage
5. Ambient Temperature.

The combination of these variables determines the junction temperature within the AD9852 device for a given set of operating conditions.

The AD9852 device is available in two package styles: a thermally-enhanced surface-mount package with an exposed heat sink, and a nonthermally-enhanced surface-mount package. The thermal impedance of these packages are 16°C/W and 38°C/W respectively, measured under still air conditions.

## THERMAL IMPEDANCE

The thermal impedance of a package can be thought of as a thermal resistor that exists between the semiconductor surface and the ambient air. The thermal impedance of a package is determined by package material and its physical dimensions. The dissipation of the heat from the package is directly dependent upon the ambient air conditions and the physical connection made between the IC package and the PCB. Adequate dissipation of power from the AD9852 relies upon all power and ground pins of the device being soldered directly to a copper plane on a PCB. In addition, the thermally-enhanced package of the AD9852ASQ contains a heat sink on the bottom of the package that must be soldered to a ground pad on the PCB surface. This pad must be connected to a large copper plane which, for convenience, may be ground plane. Sockets for either package style of the AD9852 device are not recommended.

## JUNCTION TEMPERATURE CONSIDERATIONS

The power dissipation ($P_{DISS}$) of the AD9852 device in a given application is determined by many operating conditions. Some of the conditions have a direct relationship with $P_{DISS}$, such as supply voltage and clock speed, but others are less deterministic. The total power dissipation within the device, and its effect on the junction temperature, must be considered when using the device. The junction temperature of the device is given by:

$$\textit{Junction Temperature} = (\textit{Thermal Impedance} \times \textit{Power Consumption}) + \textit{Ambient Temperature}$$

Given that the junction temperature should never exceed 150°C for the AD9852, and that the ambient temperature can be 85°C, the maximum power consumption for the AD9852AST is 1.7 W and the AD9852ASQ (thermally-enhanced package) is 4.1 W. Factors affecting the power dissipation are:

***Supply Voltage***—this obviously affects power dissipation and junction temperature since $P_{DISS}$ equals V × I. Users should design for 3.3 V nominal, however the device is guaranteed to meet specifications over the full temperature range and over the supply voltage range of 3.135 V to 3.465 V.

***Clock Speed***—this directly and linearly influences the total power dissipation of the device and, therefore, junction temperature. As a rule, to minimize power dissipation, the user should always select the lowest internal clock speed possible to support a given application. Normally the usable frequency output bandwidth from a DDS is limited to 40% of the clock rate to keep reasonable requirements on the output low-pass filter. For the typical DDS application, the system clock frequency should be 2.5 times the highest desired output frequency.

***Mode of Operation***—the selected mode of operation for the AD9852 has a great influence on total power consumption. The AD9852 offers many features and modes, each of which imposes an additional power requirement. The collection of features contained in the AD9852 target a wide variety of applications and the device was designed under the assumption that only a few would be enabled for any given application. In fact, the user must understand that enabling multiple features at higher clock speeds may cause the junction temperature of the die to be exceeded. This can severely limit the long-term reliability of the device. Figure 57 provides a summary of the power requirements associated with the individual features of the AD9852. This table should be used as a guide in determining the optimum application of the AD9852 for reliable operation.

As can be seen in the Figure 57, the Inverse Sinc filter function requires a significant amount of power, and much forethought and scrutiny should be given to its use. As an alternate approach to maintaining flatness across the output bandwidth, the Digital Multiplier function may be used to adjust the output signal level, at a dramatic savings in power consumption. Careful planning and management in the use of the feature set will minimize power dissipation and avoid exceeding junction temperature requirements within the IC.

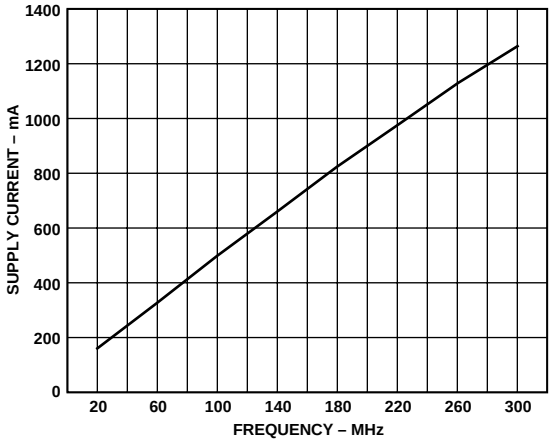



*Figure 57a. Power Consumption vs. Clock Frequency Showing Supply Current Consumption When All Optional Circuitry Is Enabled*

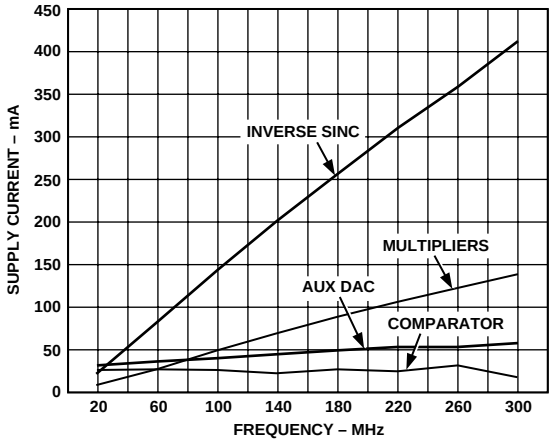



*Figure 57b. Decrease in Current Consumption When Various Circuitry Is Disabled*

**EVALUATION OF OPERATING CONDITIONS**

The first step in applying the AD9852 is to select the internal clock frequency. Clock frequency selections above 200 MHz will require the thermally-enhanced package (AD9852ASQ); clock frequency selections of 200 MHz and below may allow the user to use the standard plastic surface-mount package, but more information will be needed to make that determination.

The second step is to determine the maximum required operating temperature for the AD9852 in the given application. Subtract this value from 150°C, which is the maximum junction temperature allowed for the AD9852. For the extended industrial temperature range of 85°C, the result will be 65°C. This is the maximum rise in temperature that the junction may experience due to power dissipation.

The third step is to divide this maximum rise number by the thermal impedance, to arrive at the maximum power dissipation allowed for the application. For the example, so far, 65°C divided by both versions of the AD9852 package's thermal impedances of 38°C/W and 16°C/W, yields a total power dissipation limit of 1.7 W and 4.1 W (respectively). This means that for a 3.3 V nominal power supply voltage, the current consumed by the device under full operating conditions must not exceed 515 mA in the standard plastic package and 1242 mA in the thermally-enhanced package. The total set of enabled functions and operating conditions of the AD9852 application must support these current consumption limits.

Figure 57a and 57b may be used to determine the suitability of a given AD9852 application vs. power dissipation requirements. These graphs assume that the AD9852 device will be soldered to a multilayer PCB per the recommended best manufacturing practices and procedures for the given package type. This ensures that the specified thermal impedance specifications will be achieved.

**THERMALLY ENHANCED PACKAGE MOUNTING GUIDELINES**

The following are general recommendations for mounting the thermally enhanced exposed heat sink package (AD9852ASQ) to printed circuit boards. The exceptional thermal characteristics of this package depend entirely upon proper mechanical attachment.

Figure 58 depicts the package from the bottom and shows the dimensions of the exposed heat sink. A solid conduit of solder needs to be established between this pad and the surface of the PCB.

Figure 59 depicts a general PCB land pattern for such an exposed heat sink device. Note that this pattern is for a 64-lead device not an 80-lead, but the relative shapes and dimensions still apply. In this land pattern, a solid copper plane exists inside of the individual lands for device leads. Note also that the solder mask opening is conservatively dimensioned to avoid any assembly problems.

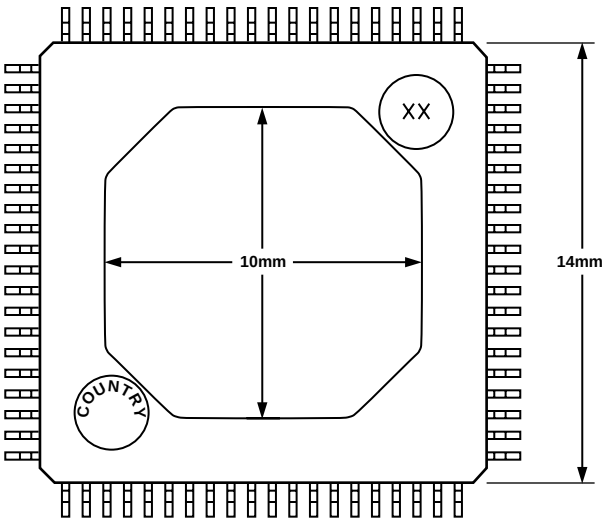



*Figure 58.*

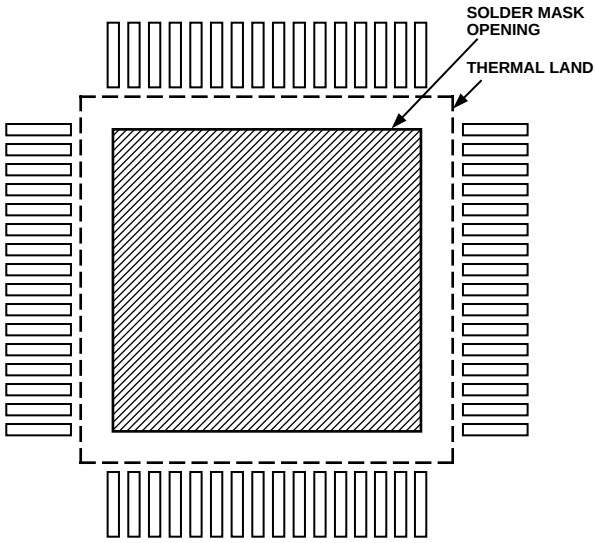



*Figure 59.*

The thermal land itself must be able to distribute heat to an even larger copper plane such as an internal ground plane. Vias must be uniformly provided over the entire thermal pad to connect to this internal plane. A proposed via pattern is shown in Figure 60. Via holes should be small (12 mils, 0.3 mm) such that they can be plated and plugged. These will provide the mechanical conduit for heat transfer.

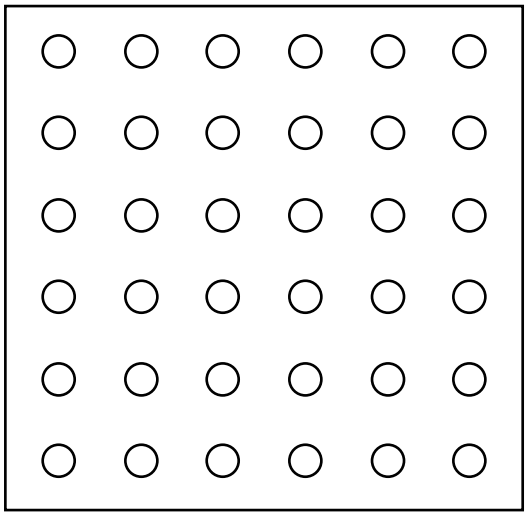


*Figure 60.*

Finally, a proposed stencil design is depicted for screen solder placement. Note that if vias are not plugged, wicking will occur which will displace solder away from the exposed heat sink and the necessary mechanical bond will not be established.

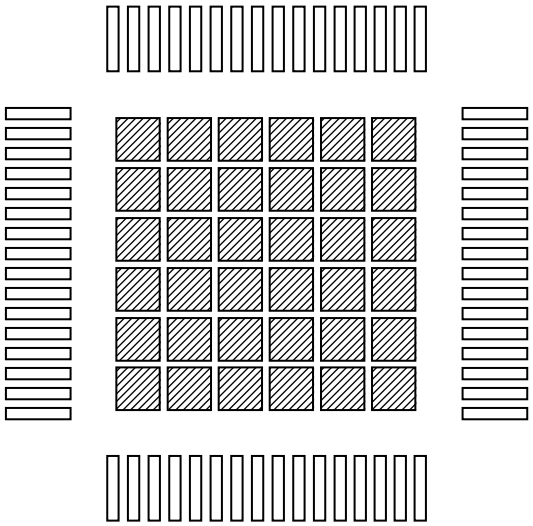


*Figure 61.*

**EVALUATION BOARD**

An evaluation board is available that supports the AD9852 DDS devices. This evaluation board consists of a PCB, software, and documentation to facilitate bench analysis of the performance of the AD9852 device. It is recommended that users of the AD9852 familiarize themselves with the operation and performance capabilities of the device with the evaluation board. The evaluation board should also be used as a PCB reference design to ensure optimum dynamic performance from the device.

**OPERATING INSTRUCTIONS**

To assist in proper placement of the pin-header shorting-jumpers, the instructions will refer to direction (left, right, top, bottom) as well as header pins to be shorted. Pin #1 for each three pin-header has been marked on the PCB corresponding with the schematic diagram. When following these instructions, position the PCB so that the text can be read from left to right. The board is shipped with the pin-headers configuring the board as follows:

1. REFCLK for the AD9852 is configured as differential. The differential clock signals are provided by the 100LVEL16 differential receiver.
2. Input clock for the 100LVEL16 is single-ended via J5. This signal may be 3.3 V CMOS or a 2 V p-p sine wave capable of driving 50 Ω (R8).
3. Both DAC outputs from the AD9852 are routed through the two 120 MHz elliptical LP filters and their outputs connected to J3 (Q) and J4 (I).
4. The board is set up for software control via the printer port connector.
5. Configured for AD9852 operation.

*Load the software* from the CD onto the host PC's hard disk. Only Windows 9X/NT operating system is supported. Connect a printer cable from the PC to the AD9852 Evaluation Board printer port connector labeled "J11."

*Attach power* wires to connector labeled "TB1" using the screw-down terminals. This is a plastic connector that press-fits over a 4-pin header soldered to the board. Table IX below shows connections to each pin. DUT = "device under test."

**Table IX. Power Requirements for DUT Pins**

| | | | |
|---|---|---|---|
| AVDD 3.3 V for All DUT Analog Pins | DVDD 3.3 V for All DUT Digital Pins | VCC 3.3 V for All Other Devices | Ground —for All Devices |

**Attach REFCLK**

There are three possibilities to choose from:

1. On-Board (But Optional) Crystal Clock Oscillator, Y1. Insert an appropriate 3.3 V CMOS clock oscillator. See that the shorting jumper at W5 is located on Pins 1 and 2 (the left two pins). This routes the single-ended oscillator output to a very high speed "Differential Receiver" (the MC100LVEL16), where the signal is transformed to a *differential PECL output.* To route the differential output signals to AD9852, two more switches must be configured. W9 must have a shorting jumper on Pins 2 and 3 (the right two pins). To engage the differential clocking mode of the AD9852 W3, Pins 2 and 3 (the right two pins) must be connected with a shorting jumper.
2. External Differential Clock Input, J5. This is actually just another single-ended input that will be routed to the MC100LVEL16 for conversion to differential PECL output. This is accomplished by attaching a 2 V p-p clock or sine wave source to J5. Note that this is a 50 Ω impedance point set by R8. The input signal will be ac-coupled and then biased to the center switching threshold of the MC100LVEL16. Position the shorting jumper of W5 to Pins 2 and 3 (the right two pins) to route the signal at J5 to the differential receiver IC. To route the differential output signals to AD9852, two more switches must be configured. W9 must have a shorting jumper on Pins 2 and 3 (the right two pins). To engage the differential clocking mode of the AD9852 W3, Pins 2 and 3 (the right two pins) must be connected with a shorting jumper.
3. External Single-Ended Clock Input, J7**.** This mode bypasses the MC100LVEL16 and directly drives the AD9852 with your reference clock. Attach a 50 Ω, 2 V p-p sine source that is dc offset to 1.65 V, or a 50 Ω CMOS-level clock source to J7. Remove the shorting jumper from W5 altogether to make certain that the device (U3) is not Toggling or Self-Oscillating. Set the shorting jumper at W9 on Pins 1 and 2 (the left two pins) to route the REFCLK signal from J7 to Pin 69 of the AD9852. Finally, set the shorting jumper at W3 to Pins 1 and 2 (the left two pins) to place the AD9852 in the single-ended clock mode.

Regardless of the origination, the signals arriving at the AD9852 are called the Reference Clock. If you choose to engage the on-chip REFCLK Multiplier, this signal is the reference clock for the REFCLK Multiplier and the REFCLK Multiplier output becomes the SYSTEM CLOCK. If you choose to bypass the REFCLK Multiplier, the reference clock that you have supplied is directly operating the AD9852 and is, therefore, the system clock.

Three-state control or switch headers W11, W12, W14, and W15 must be shorted to allow the provided software to control the AD9852 evaluation board via the printer port connector J11. If programming of the AD9852 is not to be provided by the host PC via the ADI software, then headers W11, W12, W14, and W15 should be opened (shorting jumpers removed). This effectively detaches the PC interface and allows the 40-pin header, J10, to assume control without bus contention. Input signals on J10 going to the AD9852 should be 3.3 V CMOS logic levels.

**Low-Pass Filter Testing**

The purpose of 2-pin headers W7 and W10 (associated with J1 and J2) are to allow the two 50 Ω, 120 MHz filters to be tested during PCB assembly without interference from other circuitry attached to the filter inputs. *Normally, a shorting jumper will be attached to each header to allow the DAC signals to be routed to the filters.* If the user wishes to test the filters, the shorting jumpers at W7 and W10 should be removed and 50 Ω test signals applied at J1 and J2 inputs to the 50 Ω elliptic filters. User should refer to Figure 62 and the following sections to properly position the remaining shorting jumpers.

**Observing the Unfiltered IOUT1 and the Unfiltered IOUT2 DAC Signals**

This allows the viewer to observe the unfiltered DAC outputs at J2 (the "I" signal) and J1 (the "Q" signal). The procedure below simply routes the two 50 Ω terminated analog DAC outputs to the BNC connectors and disconnects any other circuitry. The "raw" DAC outputs will be a series of quantized (stepped) output levels. The default 10 mA output current will develop a 0.5 V p-p signal across the on-board 50 Ω termination. When connected to an external 50 Ω input, the DAC will therefore develop 0.25 V p-p due to the double termination.

1. Install shorting jumpers at W7 and W10.
2. Remove shorting jumper at W16.
3. Remove shorting jumper from 3-pin header W1.
4. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W4.

**Observing the Filtered IOUT1 and the Filtered IOUT2**

This allows viewer to observe the filtered sine DAC and control DAC outputs at J4 (the sine signal) and J3 (the control DAC signal). This places the 50 Ω (input and output Z) low-pass filters in the I and Q DAC pathways to remove images and aliased harmonics and other spurious signals above the dc to approximately 120 MHz bandpass. These filters are designed with the assumption that the system clock speed is at or near maximum (300 MHz). If the system clock utilized is much less than 300 MHz, for example, 200 MHz, unwanted DAC products other than the fundamental signal will be passed by the low-pass filters.

1. Install shorting jumpers at W7 and W10.
2. Install shorting jumper at W16.
3. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W1.
4. Install shorting jumper on Pins 1 and 2 (bottom two pins) of 3-pin header W4.
5. Install shorting jumper on Pins 1 and 2 (top two pins) of 3-pin header W2 and W8.

**Observing the Filtered $I_{OUT}$ and the Filtered $I_{OUT}B$**

This allows viewer to observe only the filtered sine DAC outputs at J4 (the "true" signal) and J3 (the "complementary" signal). This places the 120 MHz low-pass filters in the true

and complementary output paths of the sine DAC to remove images and aliased harmonics and other spurious signals above approximately 120 MHz. These signals will appear as nearly pure sine waves and exactly 180 degrees out-of-phase with each other. Again, if the system clock utilized is much less than 300 MHz, for example, 200 MHz, unwanted DAC products other than the fundamental signal will be passed by the low-pass filters.

1. Install shorting jumpers at W7 and W10.
2. Install shorting jumper at W16.
3. Install shorting jumper on Pins 2 and 3 (top two pins) of 3-pin header W1.
4. Install shorting jumper on Pins 2 and 3 (top two pins) of 3-pin header W4.
5. Install shorting jumper on Pins 1 and 2 (top two pins) of 3-pin header W2 and W8.

**Connecting the High-Speed Comparator in a Single-Ended Configuration**

This will allow duty cycle or pulsewidth control and requires that a dc threshold voltage be present at one of the comparator inputs. You may supply this voltage using the control DAC. A 12-bit, twos-complement value is written to the control DAC register that will set the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum) with all 0s being midscale. The $I_{OUT}1$ channel will continue to output a filtered sine wave programmed by the user. These two signals are routed to the comparator inputs using W2 and W8 3-pin header switches. The configuration described above entitled "Observing the Filtered IOUT1 and the Filtered IOUT2" must be used. Follow steps 1 through 4 above and then the following Step 5.

5. Install shorting jumper on Pins 2 and 3 (bottom two pins) of 3-pin header W2 and W8

User should elect to change the $R_{SET}$ resistor from 3900 Ω to 1950 Ω to obtain a more robust signal at the comparator inputs. This will decrease jitter and extend comparator operating range. User can accomplish this by soldering a second 3.9 kΩ chip resistor in parallel with the provided R2.

**USING THE CONTROL SOFTWARE**

The control software for the AD9852/PCB evaluation board is provided on a CD. This brief set of instructions should be used in conjunction with the AD9852/PCB evaluation board schematic. Several numerical entries, such as frequency and phase information, require that the ENTER key by pressed to register that information.

1. Select the proper printer port. Click the "Parallel Port" selection in the menu bar. Select the port that matches your PC. If unknown, experiment by performing the following on the selected port. With the part powered up, properly clocked and connected to the PC, select a port and go to the "Mode and Frequency" menu and click the "Reset DUT and Initialize Registers" button. Then go to the "Clock and Amplitude" menu. Once there, click the box next to "Bypass Inverse Sinc Filter" . . . a check mark will appear in the box . . . next click the button "Send Control Info to DUT." If the proper port has been selected, the supply current going to the AD9852/PCB evaluation board should drop by approximately 1/3 when the inverse sinc filters are bypassed. Conversely, the supply current will increase approximately 1/3 when the inverse sinc filters are engaged.
2. Normal operation of the AD9852/PCB evaluation board begins with a master reset. Many of the default register values after reset are depicted in the software "control panel." The reset command sets the DDS output amplitude to minimum and 0 Hz, 0 phase-offset as well as other states listed in the AD9852 Register Layout table in the preliminary data sheet.
3. The next programming block should be the "Reference Clock and Multiplier" since this information is used to determine the proper 48-bit frequency tuning words that will be entered and calculated later.
4. The output amplitude defaults to the 12-bit straight binary multiplier values of the I and Q multiplier registers of 000hex and no output should be seen from the DACs. User should now set both multiplier amplitudes in the Output Amplitude window to a substantial value, such as FFFhex. You may bypass the digital multiplier by clicking the box "Output Amplitude is always Full-Scale" but experience has shown that doing so does not result in best SFDR It is interesting to note that best SFDR, as much as 11 dB better, is obtained by routing the signal through the digital multiplier and "backing off" on the multiplier amplitude. For instance, FC0 hex produces less spurious signal amplitude than FFF hex. Its a repeatable phenomenon that should be investigated exploited for maximum SFDR (spurious-free dynamic range).
5. Refer to this data sheet and evaluation board schematic to understand all the functions of the AD9852 available to the user and to gain an understanding of what the software is doing in response to programming commands.

Applications assistance is available for the AD9852, the AD9852/PCB evaluation board, and all other Analog Devices products. Please call 1/800-ANALOGD.

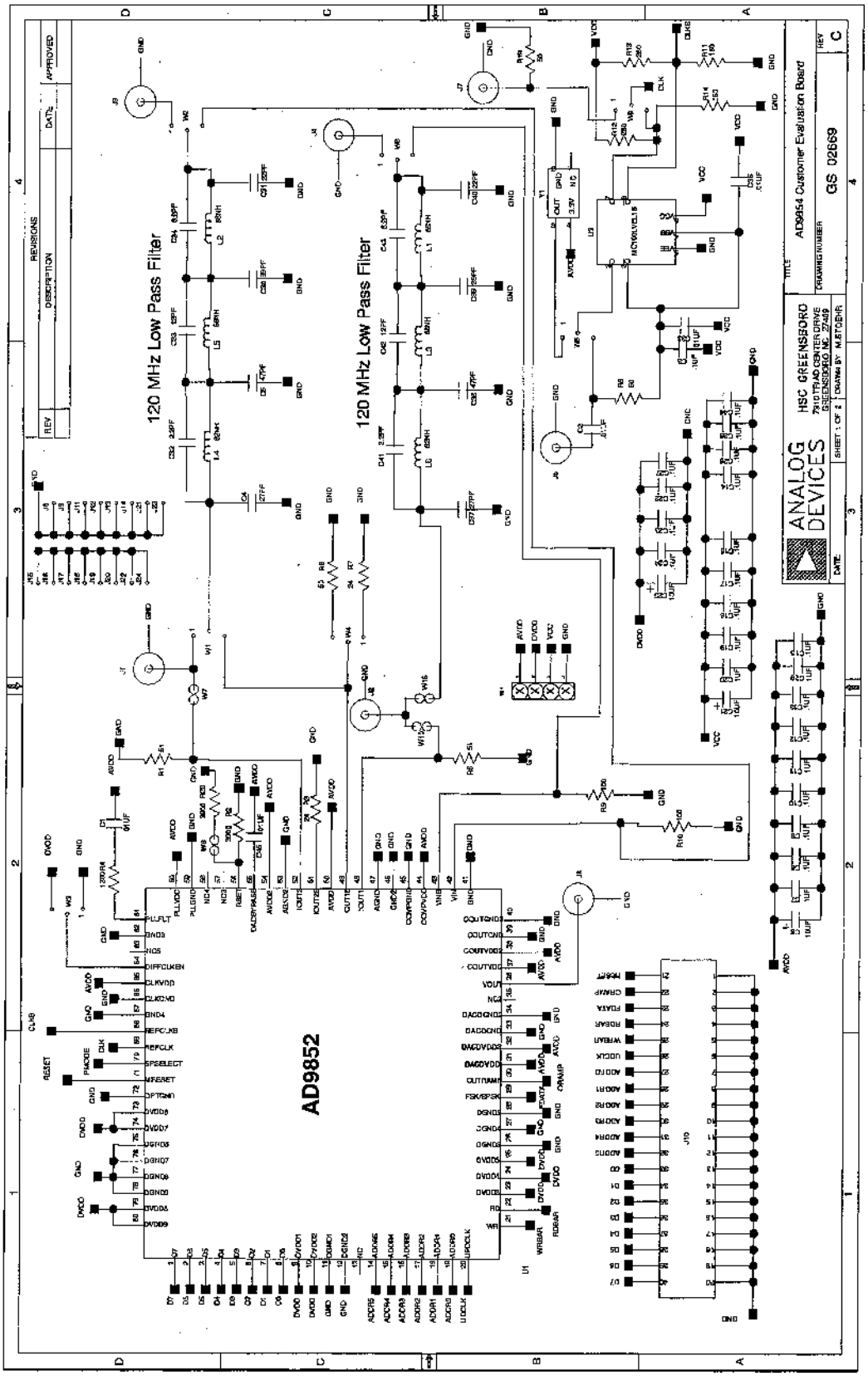



*Figure 62a. Evaluation Board Schematic*

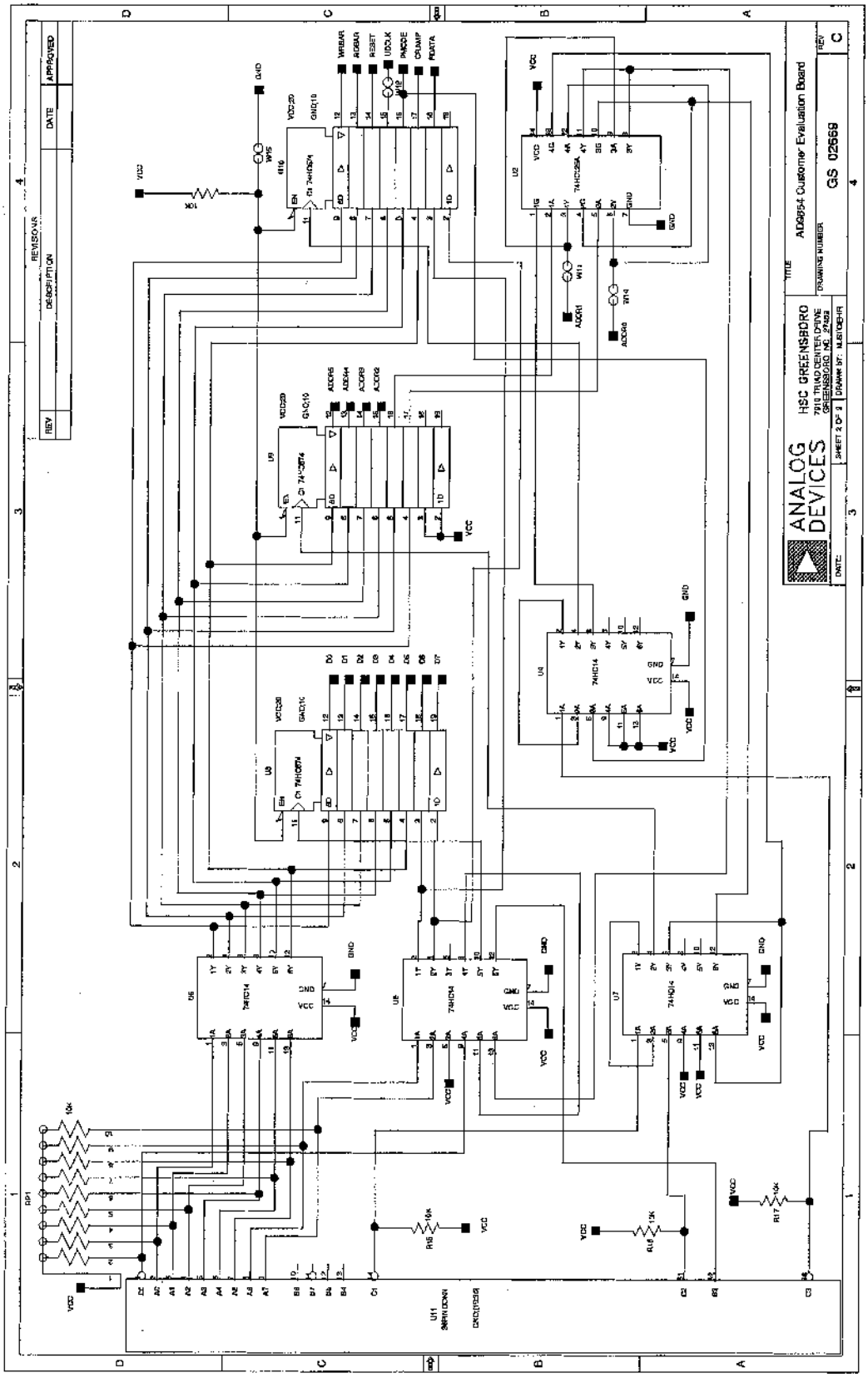



*Figure 62b. Evaluation Board Schematic*

**Customer Evaluation Board REV C, Bill of Material**

| # | Quantity | REFDES | Device | Package | Value |
|---|---|---|---|---|---|
| 1 | 5 | C1, C2, C35, C36, C45 | Chip Cap | 0805 | |
| 2 | 23 | C3, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C22, C23, C24, C26, C27, C28, C29, C44 | Chip Cap | 0805 | 0.1 µF |
| 3 | 2 | C4, C37 | 0805 | 0805 | 27 pF |
| 4 | 2 | C5, C38 | 0805 | 0805 | 47 pF |
| 5 | 3 | C6, C21, C25 | BCAPTAJD | TAJD | 10 µF |
| 6 | 2 | C30, C39 | 0805 | 0805 | 39 pF |
| | 2 | C31, C40 | 0805 | 0805 | 22 pF |
| 8 | 2 | C32, C41 | 0805 | 0805 | 2.2 pF |
| 9 | 2 | C33, C42 | 0805 | 0805 | 12 pF |
| 10 | 2 | C34, C43 | 0805 | 0805 | 8.2 pF |
| 11 | 7 | J1, J2, J3, J4, J5, J6, J7 | Conn | BNC | |
| 12 | 1 | | PCB | GS02669REVC | |
| 13 | 1 | J10 | 40CONN | SAM5-40 | |
| 14 | 4 | L1, L2, L3, L5 | Chip Ind | 1206 | 68NH |
| 15 | 2 | L4, L6 | Chip Ind | 1206 | 82NH |
| 16 | 2 | R1, R5 | RES_SM | 1206 | 51 |
| 17 | 2 | R2, R20 | RES_SM | 1206 | 3900 |
| 18 | 2 | R3, R7 | RES_SM | 1206 | 24 |
| 19 | 1 | R4 | RES_SM | 1206 | 1300 |
| 20 | 3 | R6, R8, R19 | RES_SM | 1206 | 50 |
| 21 | 2 | R9, R10 | RES_SM | 1206 | 100 |
| 22 | 2 | R11, R14 | RES_SM | 1206 | 160 |
| 23 | 2 | R12, R13 | RES_SM | 1206 | 260 |
| 24 | 4 | R15, R16, R17, R18 | RES_SM | 1206 | 10K |
| 25 | 1 | RP1 | RP1 | SIP-10P | 10K |
| 26 | 1 | TB | TB4 | TB4 | |
| 27 | 1 | U1 | AD9852 | 80LQFP | |
| 28 | 1 | U2 | 74HC125A | SO14 | |
| 29 | 1 | U3 | MC100LVEL1 | SO8NB | |
| 30 | 4 | U4, U5, U6, U7 | 74HC14 | SO14 | |
| 31 | 3 | U8, U9, U10 | 74HC574 | SO20WB | |
| 32 | 1 | U11 | 36PINCONN | CONN | |
| 33 | 7 | W1, W2, W3, W4, W5, W8, W9 | JUMP3PIN | SIP-3P | |
| 34 | 8 | W6, W7, W10, W11, W12, W14, W15, W16 | 2PINJUMP | 2PINJUMP | |
| 35 | 1 | Y1 | XTAL | COSC | |
| 36 | 4 | | PIN SOCK | Amp 5-330808-6 | |

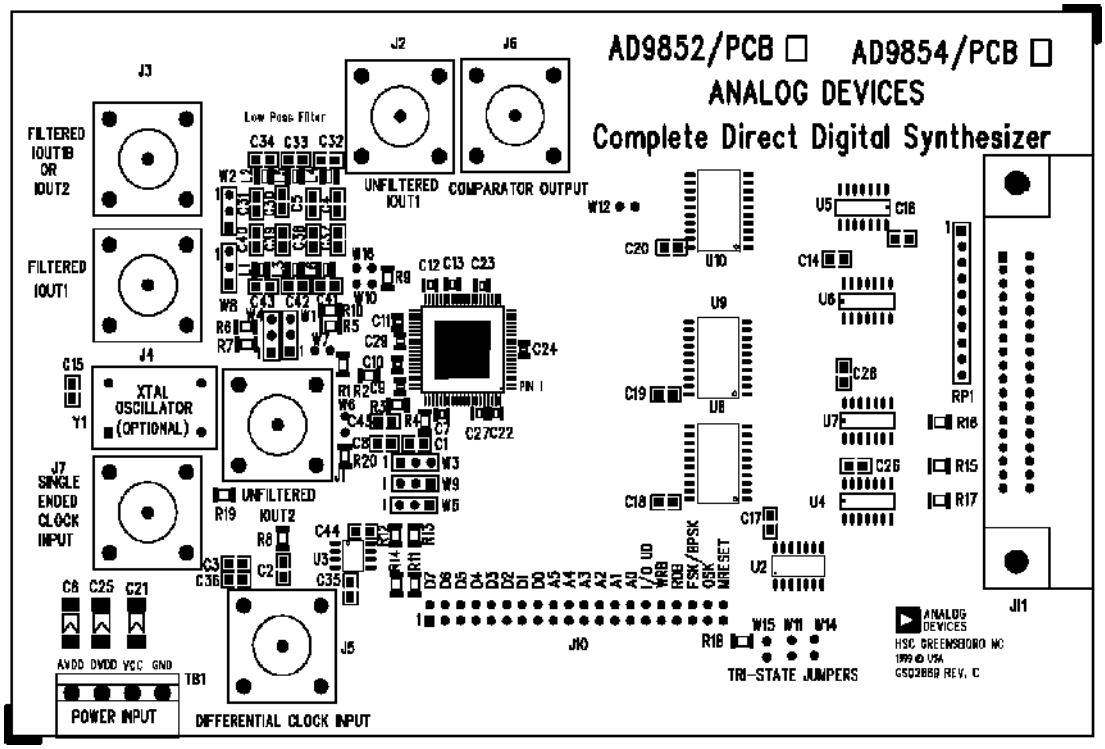



*Figure 63. Assembly Drawing*

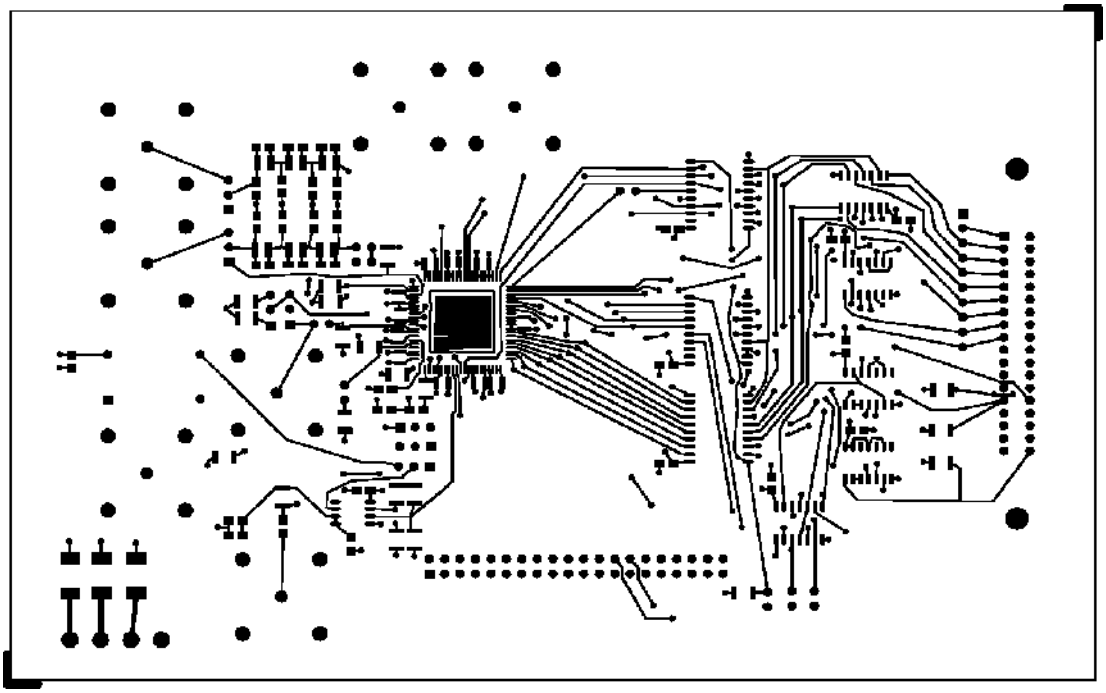


*Figure 64. Top Routing Layer, Layer 1*

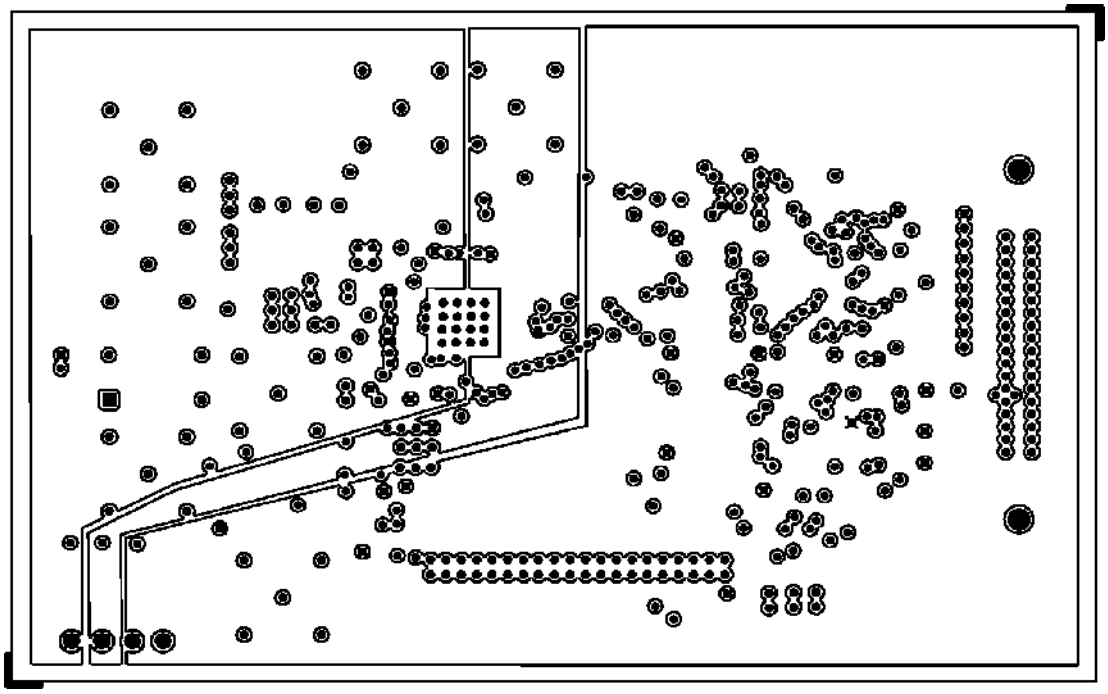


*Figure 65. Power Plane Layer, Layer 2*

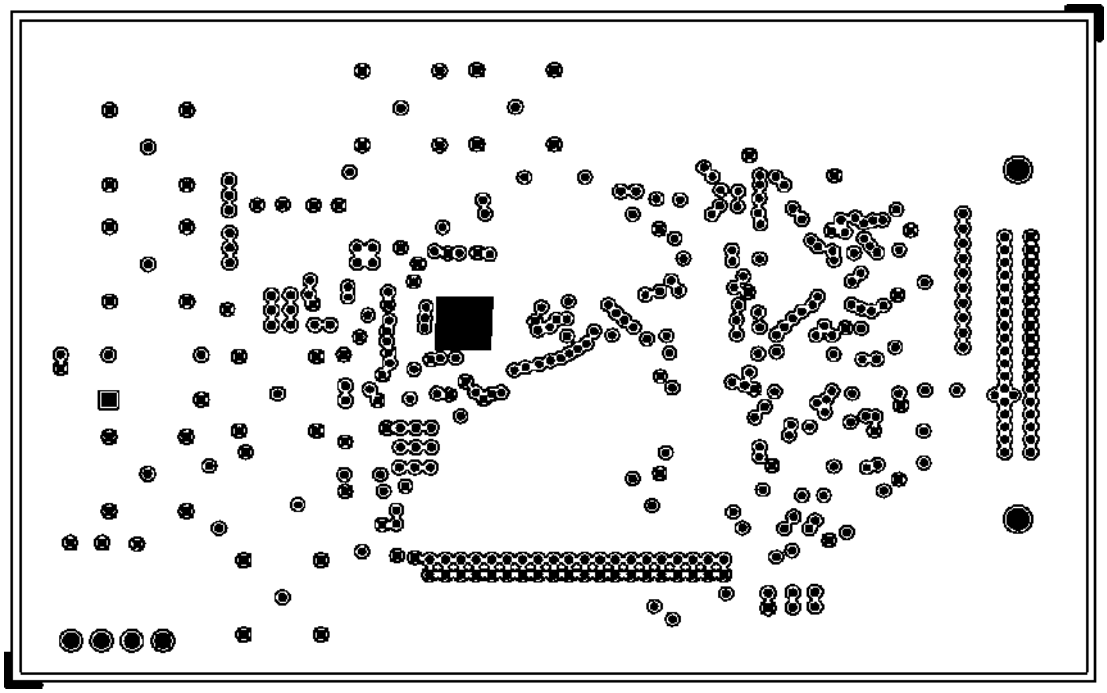


*Figure 66. Ground Plane Layer, Layer 3*

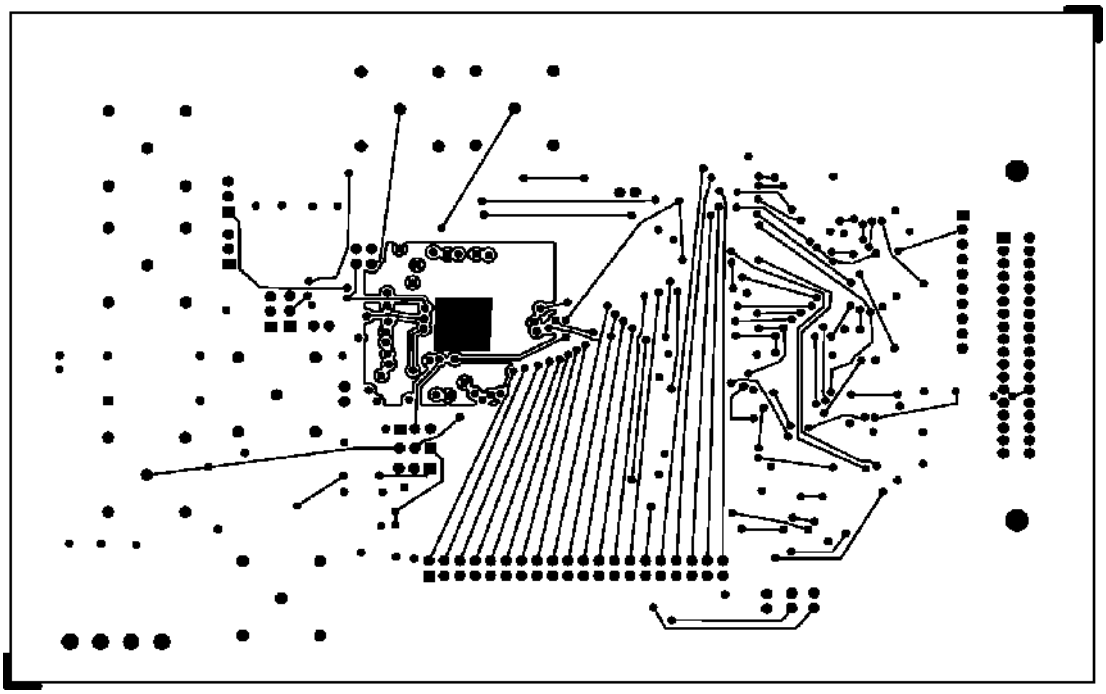
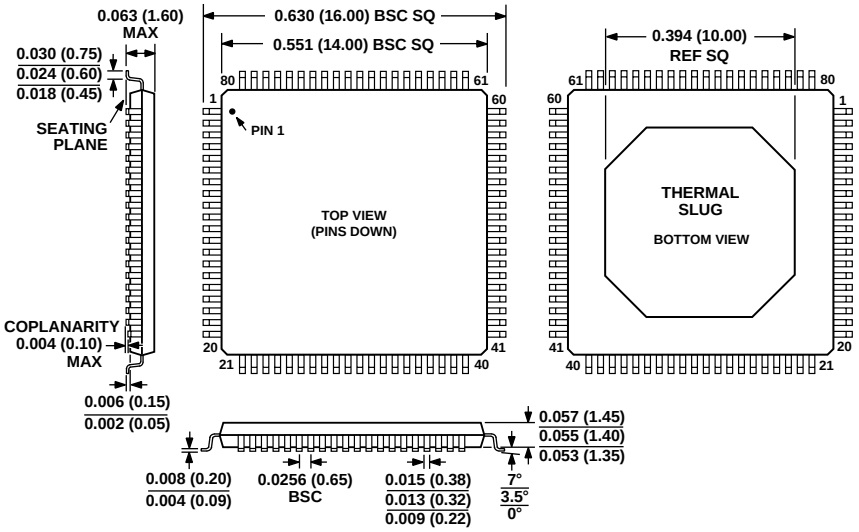


*Figure 67. Bottom Routing, Layer 4*

## OUTLINE DIMENSIONS

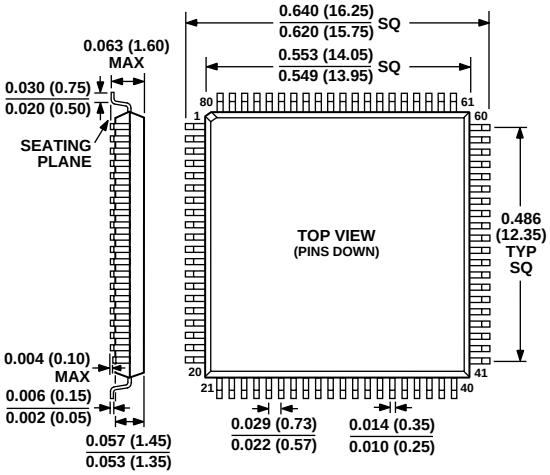
Dimensions shown in inches and (mm).

### 80-Lead LQFP_ED
### (SQ-80)




CONTROLLING DIMENSIONS IN MILLIMETERS.
CENTER FIGURES ARE NOMINAL UNLESS OTHERWISE NOTED.

### 80-Lead LQFP
### (ST-80)




C3727–8–10/99

PRINTED IN U.S.A.