

## 74VHC4316

### Quad Analog Switch with Level Translator

#### General Description

These devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the 4316 to implement a level translator which enables this circuit to operate with 0V–6V logic levels and up to  $\pm 6V$  analog switch levels. The 4316 also has a common enable input in addition to each switch's control which when HIGH will disable all switches to their off state. All analog inputs and outputs and digital

inputs are protected from electrostatic damage by diodes to  $V_{CC}$  and ground.

#### Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range:  $\pm 6V$
- Low "on" resistance: 50 typ. ( $V_{CC}-V_{EE} = 4.5V$ )  
30 typ. ( $V_{CC}-V_{EE} = 9V$ )
- Low quiescent current: 80  $\mu A$  maximum (74VHC)
- Matched switch characteristics
- Individual switch controls plus a common enable
- Pin functional compatible with 74HC4316

#### Ordering Code:

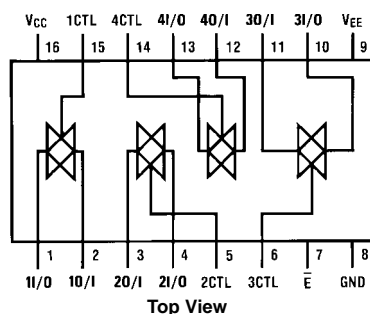
Order Number	Package Number	Package Description
74VHC4316M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74VHC4316WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74VHC4316MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC4316N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

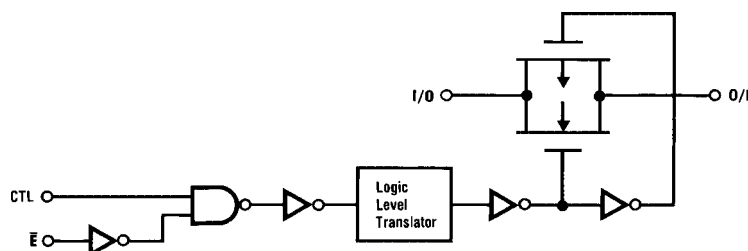
#### Truth Table

Inputs		Switch
$\bar{E}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

#### Connection Diagram



#### Logic Diagram



**Absolute Maximum Ratings** (Note 1)

(Note 2)

Supply Voltage ( $V_{CC}$ )	−0.5 to +7.5V
Supply Voltage ( $V_{EE}$ )	+0.5 to −7.5V
DC Control Input Voltage ( $V_{IN}$ )	−1.5 to $V_{CC}+1.5V$
DC Switch I/O Voltage ( $V_{IO}$ )	$V_{EE}-0.5$ to $V_{CC}+0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	±20 mA
DC Output Current, per pin ( $I_{OUT}$ )	±25 mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±50 mA
Storage Temperature Range ( $T_{STG}$ )	−65°C to +150°C
Power Dissipation ( $P_D$ ) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Recommended Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
Supply Voltage ( $V_{EE}$ )	0	−6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	−40	+85	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns
$V_{CC} = 12.0V$		250	ns

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	V <sub>EE</sub>	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = −40°C to +85°C		Units						
					Typ	Guaranteed Limits									
V <sub>IH</sub>	Minimum HIGH Level Input Voltage			2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	V							
V <sub>IL</sub>	Maximum LOW Level Input Voltage			2.0V 4.5V 6.0V		0.5 1.35 1.8	0.5 1.35 1.8	V							
R <sub>ON</sub>	Minimum “ON” Resistance (Note 5)	V <sub>CTL</sub> = V <sub>IH</sub> , I <sub>S</sub> = 2.0 mA V <sub>IS</sub> = V <sub>CC</sub> to V <sub>EE</sub> (Figure 1)	GND −4.5V −6.0V	4.5V 4.5V 6.0V	100 40 30	170 85 70	200 105 85	Ω							
		V <sub>CTL</sub> = V <sub>IH</sub> , I <sub>S</sub> = 2.0 mA V <sub>IS</sub> = V <sub>CC</sub> or V <sub>EE</sub> (Figure 1)	GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	100 40 50 20	180 80 60 40	215 100 75 60								
		R <sub>ON</sub>	Maximum “ON” Resistance Matching	V <sub>CTL</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to V <sub>EE</sub>	GND −4.5V −6.0V	4.5V 4.5V 6.0V	10 5 5		15 15 10	20 15 15	Ω				
					I <sub>IN</sub>	Maximum Control Input Current	V <sub>IN</sub> = V <sub>CC</sub> or GND		GND	6.0V			±0.1	±1.0	μA
					I <sub>IZ</sub>	Maximum Switch “OFF” Leakage Current	V <sub>OS</sub> = V <sub>CC</sub> or V <sub>EE</sub> V <sub>IS</sub> = V <sub>EE</sub> or V <sub>CC</sub> V <sub>CTL</sub> = V <sub>IL</sub> (Figure 2)		GND −6.0V	6.0V 6.0V			±30 ±50	±300 ±500	nA
		I <sub>IZ</sub>	Maximum Switch “ON” Leakage Current	V <sub>IS</sub> = V <sub>CC</sub> to V <sub>EE</sub> V <sub>CTL</sub> = V <sub>IH</sub> , V <sub>OS</sub> = OPEN (Figure 3)	GND −6.0V	6.0V 6.0V			±20 ±30	±75 ±150	nA				
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	GND −6.0V	6.0V 6.0V		1.0 4.0	10 40	μA							

**Note 4:** For a power supply of 5V ±10% the worst case on resistances ( $R_{ON}$ ) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

**Note 5:** At supply voltages ( $V_{CC}-V_{EE}$ ) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

## AC Electrical Characteristics

$V_{CC} = 2.0V - 6.0V$ ,  $V_{EE} = 0V - 6V$ ,  $C_L = 50$  pF unless otherwise specified

Symbol	Parameter	Conditions	V <sub>EE</sub>	V <sub>CC</sub>	T <sub>A</sub> =+25°C		T <sub>A</sub> =−40°C to +85°C	Units
					Typ	Guaranteed Limits		
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay Switch In to Out		GND GND −4.5V −6.0V	3.3V 4.5V 4.5V 6.0V	15 5 4 3	30 10 8 7	37 13 12 11	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Switch Turn “ON” Delay (Control)	R <sub>L</sub> = 1 kΩ	GND GND −4.5V −6.0V	3.3V 4.5V 4.5V 6.0V	25 20 15 14	97 35 32 30	120 43 39 37	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Switch Turn “OFF” Delay (Control)	R <sub>L</sub> = 1 kΩ	GND GND −4.5V −6.0V	3.3V 4.5V 4.5V 6.0V	35 25 20 20	145 50 44 44	180 63 55 55	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Switch Turn “ON” Delay (Enable)		GND GND −4.5V −6.0V	3.3V 4.5V 4.5V 6.0V	27 20 19 18	120 41 38 36	150 52 48 45	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Switch Turn “OFF” Delay (Enable)		GND GND −4.5V −6.0V	3.3V 4.5V 4.5V 6.0V	42 28 23 21	155 53 47 47	190 67 59 59	ns
	Minimum Frequency Response (Figure 7) 20 log (V <sub>OS</sub> /V <sub>IS</sub> )= −3 dB	R <sub>L</sub> = 600Ω, V <sub>IS</sub> = 2V <sub>PP</sub> at (V <sub>CC</sub> −V <sub>EE</sub> /2) (Note 6)(Note 7)	0V −4.5V	4.5 4.5V	40 100			MHz
	Control to Switch Feedthrough Noise (Figure 8)	R <sub>L</sub> = 600Ω, f = 1 MHz C <sub>L</sub> = 50 pF (Note 7)(Note 8)	0V −4.5V	4.5V 4.5V	100 250			mV
	Crosstalk Between any Two Switches (Figure 9)	R <sub>L</sub> = 600Ω, f = 1 MHz	0V −4.5V	4.5V 4.5V	−52 −50			dB
	Switch OFF Signal Feedthrough Isolation (Figure 10)	R <sub>L</sub> = 600Ω, f = 1 MHz V <sub>CTL</sub> = V <sub>IL</sub> (Note 7)(Note 8)	0V −4.5V	4.5V 4.5V	−42 −44			dB
THD	Sinewave Harmonic Distortion (Figure 11)	R <sub>L</sub> = 10 KΩ, C <sub>L</sub> = 50 pF, f = 1 KHz  V <sub>IS</sub> = 4 V <sub>PP</sub> V <sub>IS</sub> = 8 V <sub>PP</sub>	0V −4.5V	4.5V 4.5V	0.013 0.008			%
C <sub>IN</sub>	Maximum Control Input Capacitance				5			pF
C <sub>IN</sub>	Maximum Switch Input Capacitance				35			pF
C <sub>IN</sub>	Maximum Feedthrough Capacitance	V <sub>CTL</sub> = GND			0.5			pF
C <sub>PD</sub>	Power Dissipation Capacitance				15			pF

**Note 6:** Adjust 0 dBm for  $f = 1$  kHz (Null  $R_L/R_{on}$  Attenuation).

**Note 7:**  $V_{IS}$  is centered at  $V_{CC} - V_{EE}/2$ .

**Note 8:** Adjust for 0 dBm.

## AC Test Circuits and Switching Time Waveforms

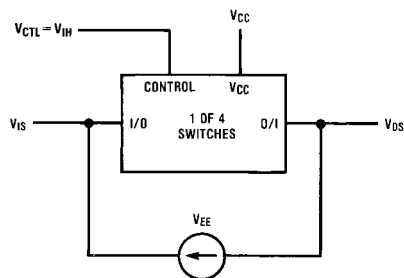


FIGURE 1. "ON" Resistance

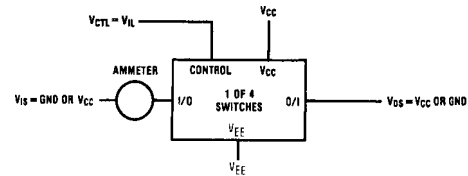


FIGURE 2. "OFF" Channel Leakage Current

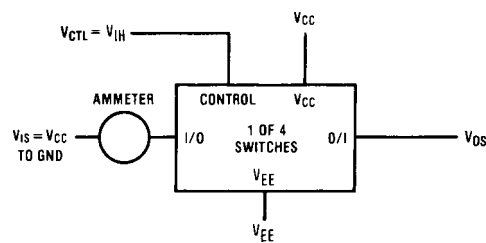
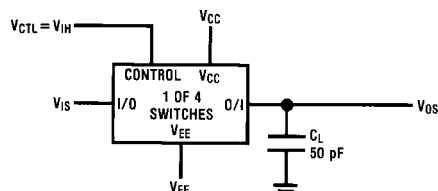
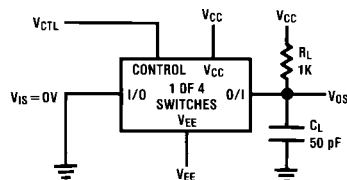
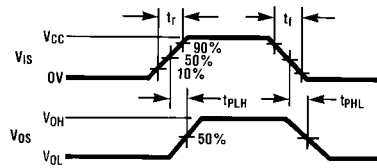
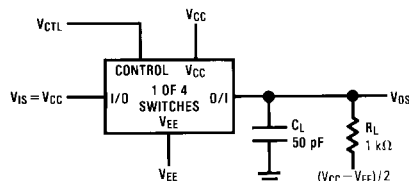
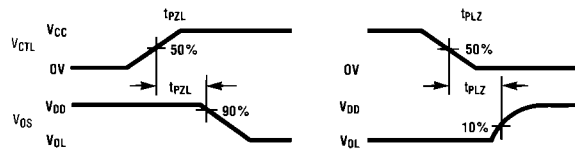
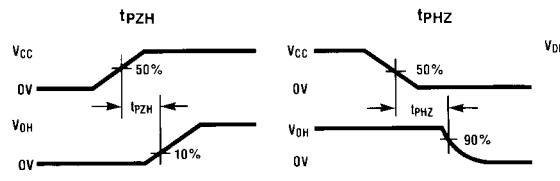


FIGURE 3. "ON" Channel Leakage Current

FIGURE 4.  $t_{PHL}$ ,  $t_{PLH}$  Propagation Delay Time Signal Input to Signal OutputFIGURE 5.  $t_{PZL}$ ,  $t_{PLZ}$  Propagation Delay Time Control to Signal OutputFIGURE 6.  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output

## AC Test Circuits and Switching Time Waveforms (Continued)

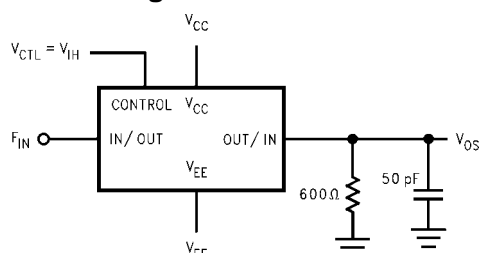


FIGURE 7. Frequency Response

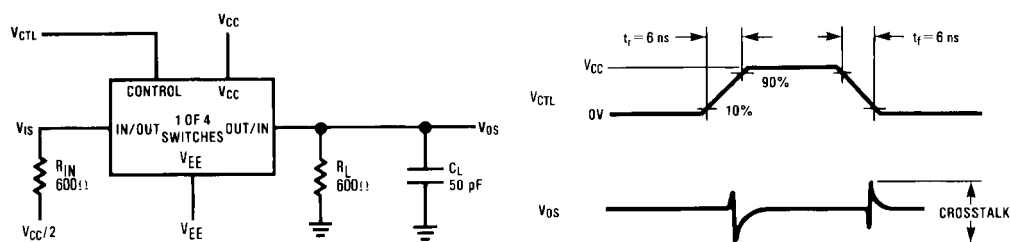


FIGURE 8. Crosstalk: Control Input to Signal Output

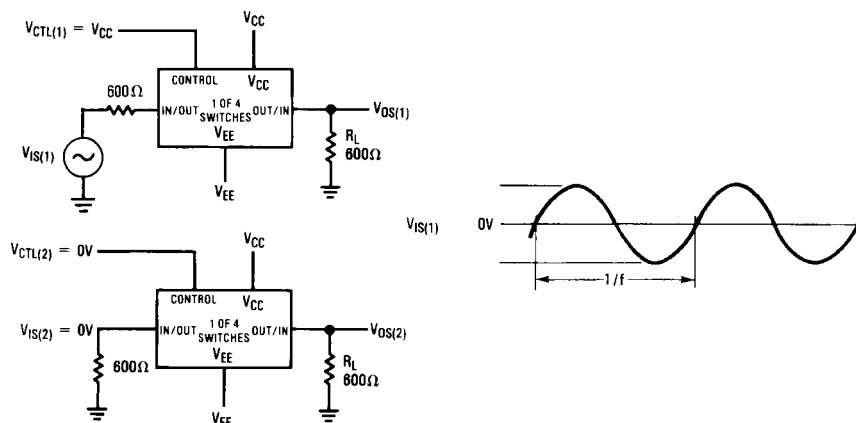


FIGURE 9. Crosstalk between Any Two Switches

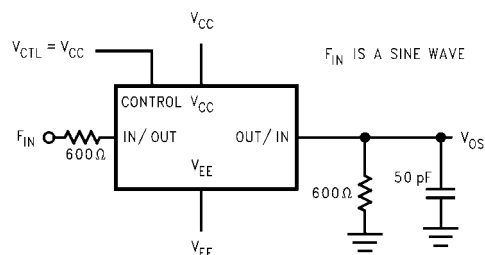


FIGURE 10. Switch OFF Signal Feedthrough Isolation

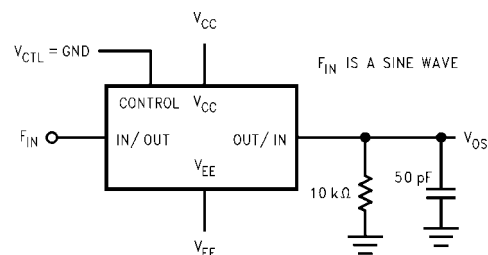
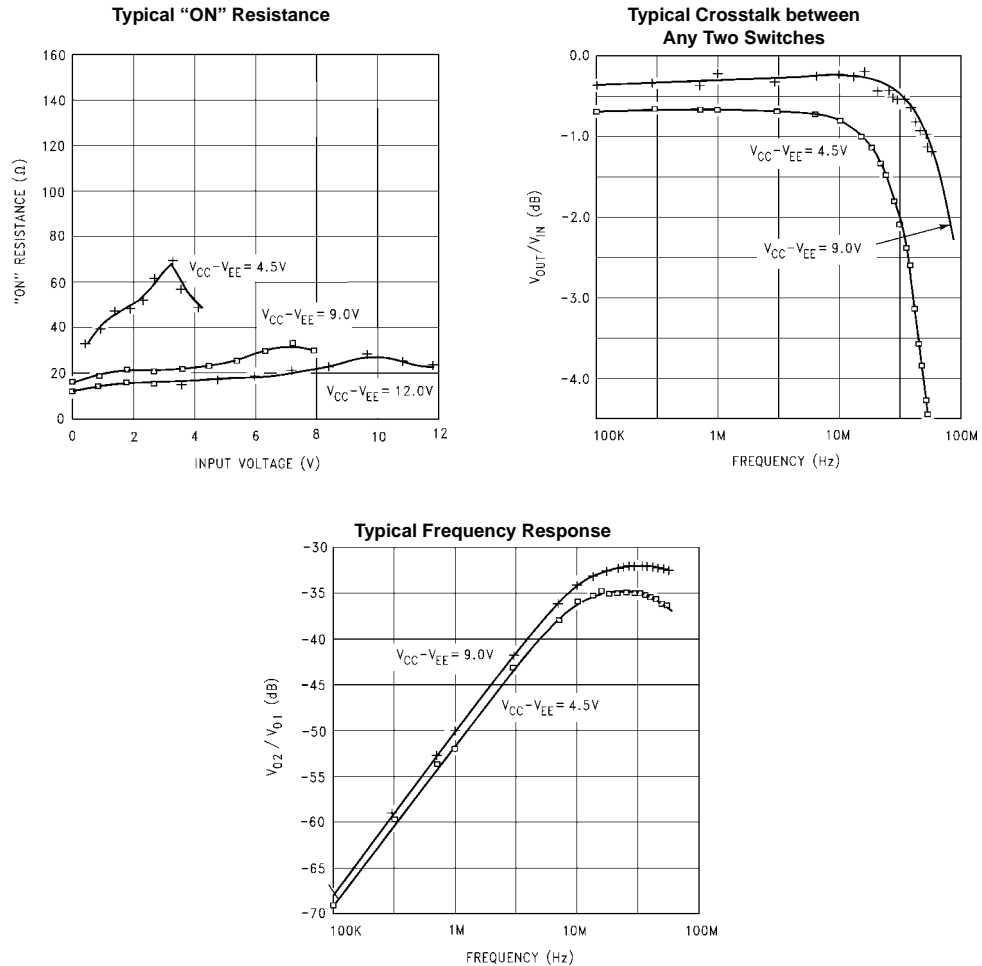


FIGURE 11. Sinewave Distortion

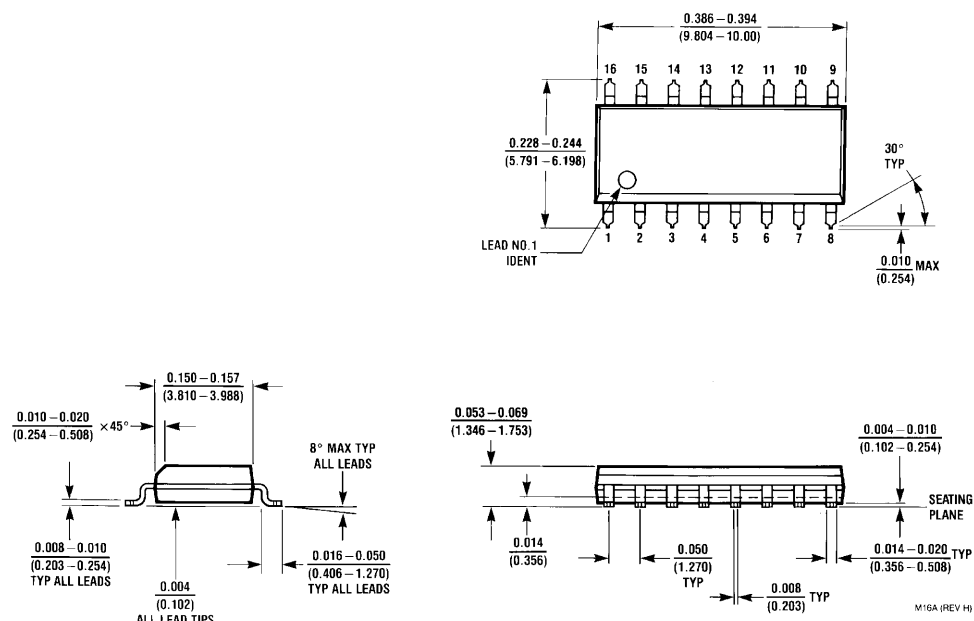
## Typical Performance Characteristics



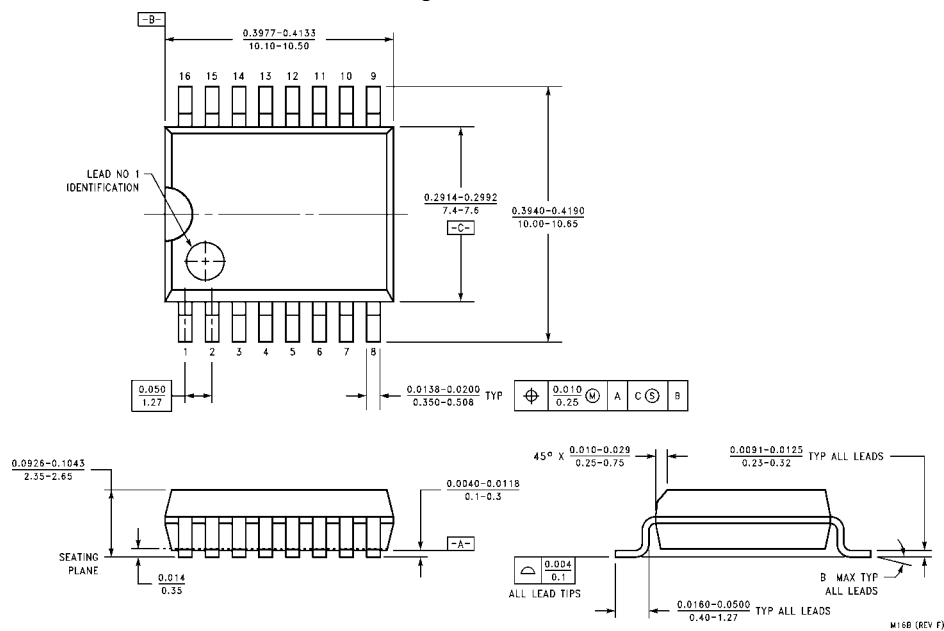
## Special Considerations

In certain applications the external load-resistor current may include both  $V_{CC}$  and signal line components. To avoid drawing  $V_{CC}$  current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

# Physical Dimensions inches (millimeters) unless otherwise noted

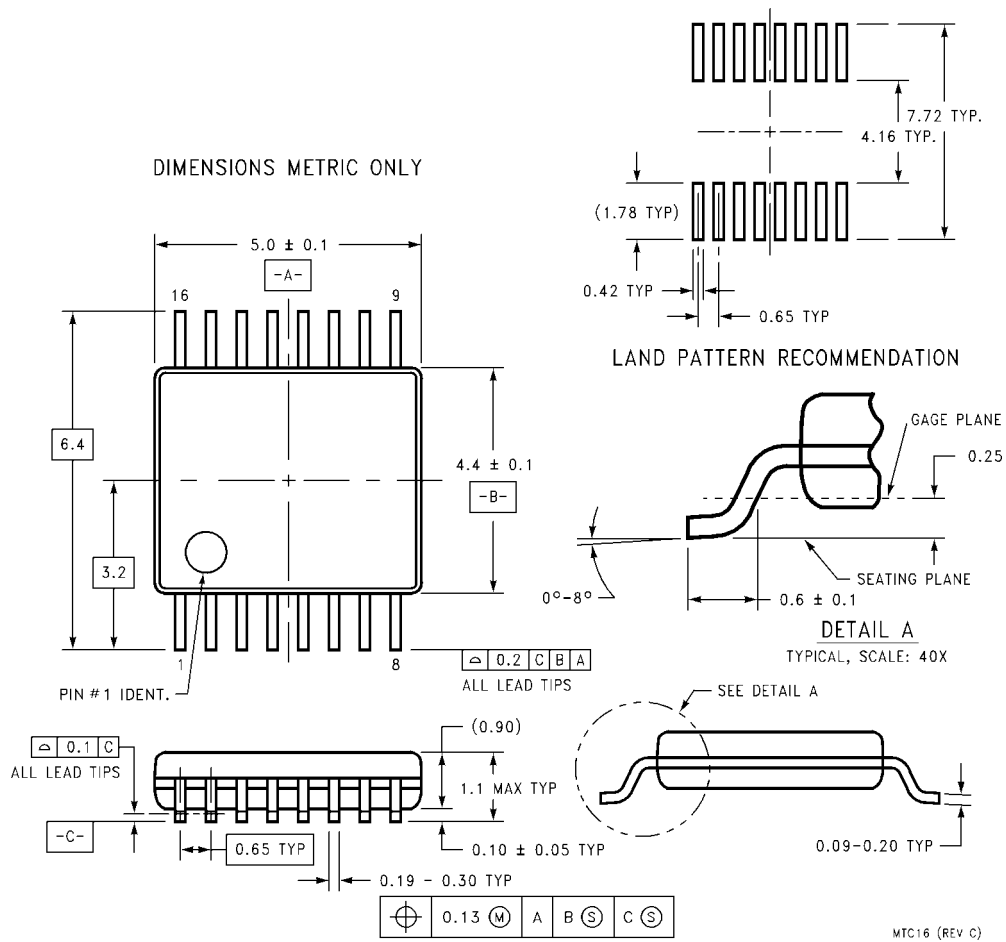


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**



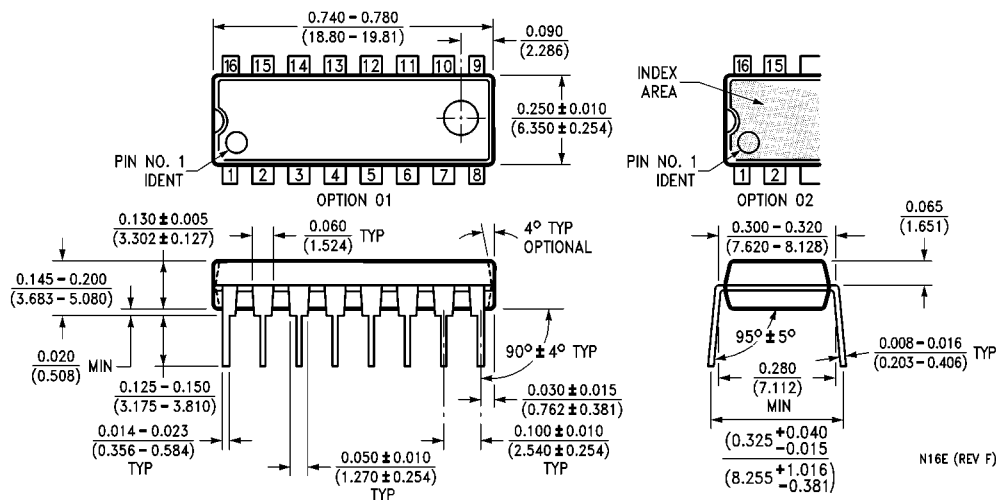
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M16B**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N16E**

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