

DATA SHEET

74LVC16244A; 74LVCH16244A
16-bit buffer/line driver; 5 V
input/output tolerant; 3-state

Product specification
Supersedes data of 2003 Jan 30

2003 Dec 08

16-bit buffer/line driver; 5 V input/output tolerant; 3-state

74LVC16244A; 74LVCH16244A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold (74LVCH16244A only).
- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC(H)16244A is a high-performance, low power, low voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 Volt. These features allow the use of these devices as a mixed 3.3 and 5 V environment.

The 74LVC(H)16244A is a 16-bit non-inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four Output Enables (1OE, 2OE, 3OE and 4OE), each controlling four of the 3-state outputs. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state.

The 74LVC(H)16244A is identical to the 74LVC16240A but has non-inverting outputs.

The 74LVCH16244A bushold data inputs eliminates the need for external pull-up resistors to hold unused inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f ≤ 2.5 ns.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|------------------------------------|--|---|---------|------|
| t _{PHL} /t _{PLH} | propagation delay nAn to nYn | C _L = 50 pF; V _{CC} = 3.3 V | 3.0 | ns |
| t _{PZH} /t _{PZL} | 3-state output enable time nOE to nYn | C _L = 50 pF; V _{CC} = 3.3 V | 3.5 | ns |
| t _{PHZ} /t _{PLZ} | 3-state output disable time nOE to nYn | C _L = 50 pF; V _{CC} = 3.3 V | 3.7 | ns |
| C _I | input capacitance | | 5.0 | pF |
| C _{PD} | power dissipation capacitance per gate | V _{CC} = 3.3 V; notes 1 and 2 | | |
| | | outputs enabled | 12 | pF |
| | | outputs disabled | 4.0 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

2. The condition is V_i = GND to V_{CC}.

16-bit buffer/line driver; 5 V input/output
tolerant; 3-state

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FUNCTION TABLE

See note 1.

| INPUT | | OUTPUT |
|-------------------------|-----|--------|
| $\overline{\text{nOE}}$ | nAn | nYn |
| L | L | L |
| L | H | H |
| H | X | Z |

Note

- H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | |
|-----------------|-------------------|------|---------|----------|----------|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE |
| 74LVC16244ADL | -40 to +125 °C | 48 | SSOP48 | plastic | SOT370-1 |
| 74LVCH16244ADL | -40 to +125 °C | 48 | SSOP48 | plastic | SOT370-1 |
| 74LVC16244ADGG | -40 to +125 °C | 48 | TSSOP48 | plastic | SOT362-1 |
| 74LVCH16244ADGG | -40 to +125 °C | 48 | TSSOP48 | plastic | SOT362-1 |
| 74LVC16244AEV | -40 to +125 °C | 56 | VFBGA56 | plastic | SOT702-1 |
| 74LVCH16244AEV | -40 to +125 °C | 56 | VFBGA56 | plastic | SOT702-1 |

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PINNING

| SYMBOL | PIN | BALL | DESCRIPTION |
|-------------------|-------------------------------|--------------------------------|----------------------------------|
| 1 \overline{OE} | 1 | A1 | output enable input (active LOW) |
| n.c. | – | A2, A3, A4, A5, K2, K3, K4, K5 | not connected |
| 1Y0 | 2 | B2 | data output |
| 1Y1 | 3 | B1 | data output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | B3, B4, D3, D4, G3, G4, J3, J4 | ground (0 V) |
| 1Y2 | 5 | C2 | data output |
| 1Y3 | 6 | C1 | data output |
| V _{CC} | 7, 18, 31, 42 | C3, H3, C4, H4 | supply voltage |
| 2Y0 | 8 | D2 | data output |
| 2Y1 | 9 | D1 | data output |
| 2Y2 | 11 | E2 | data output |
| 2Y3 | 12 | E1 | data output |
| 3Y0 | 13 | F1 | data output |
| 3Y1 | 14 | F2 | data output |
| 3Y2 | 16 | G1 | data output |
| 3Y3 | 17 | G2 | data output |
| 4Y0 | 19 | H1 | data output |
| 4Y1 | 20 | H2 | data output |
| 4Y2 | 22 | J1 | data output |
| 4Y3 | 23 | J2 | data output |
| 4 \overline{OE} | 24 | K1 | output enable input (active LOW) |
| 3 \overline{OE} | 25 | K6 | output enable input (active LOW) |
| 4A3 | 26 | J5 | data input |
| 4A2 | 27 | J6 | data input |
| 4A1 | 29 | H5 | data input |
| 4A0 | 30 | H6 | data input |
| 3A3 | 32 | G5 | data input |
| 3A2 | 33 | G6 | data input |
| 3A1 | 35 | F5 | data input |
| 3A0 | 36 | F6 | data input |
| 2A3 | 37 | E6 | data input |
| 2A2 | 38 | E5 | data input |
| 2A1 | 40 | D6 | data input |
| 2A0 | 41 | D5 | data input |
| 1A3 | 43 | C6 | data input |
| 1A2 | 44 | C5 | data input |
| 1A1 | 46 | B6 | data input |
| 1A0 | 47 | B5 | data input |
| 2 \overline{OE} | 48 | A6 | output enable input (active LOW) |

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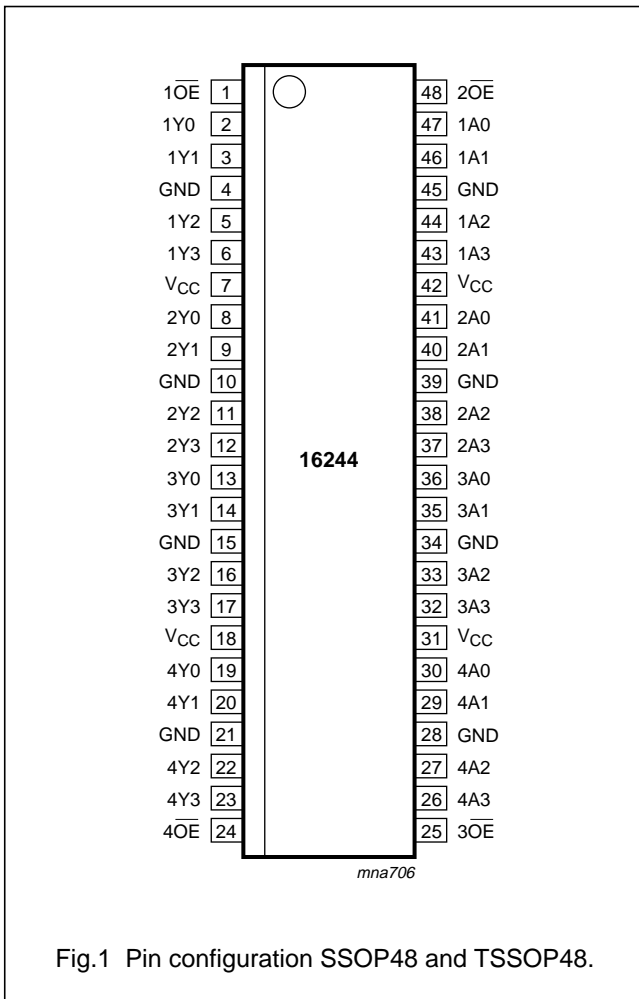


Fig.1 Pin configuration SSOP48 and TSSOP48.

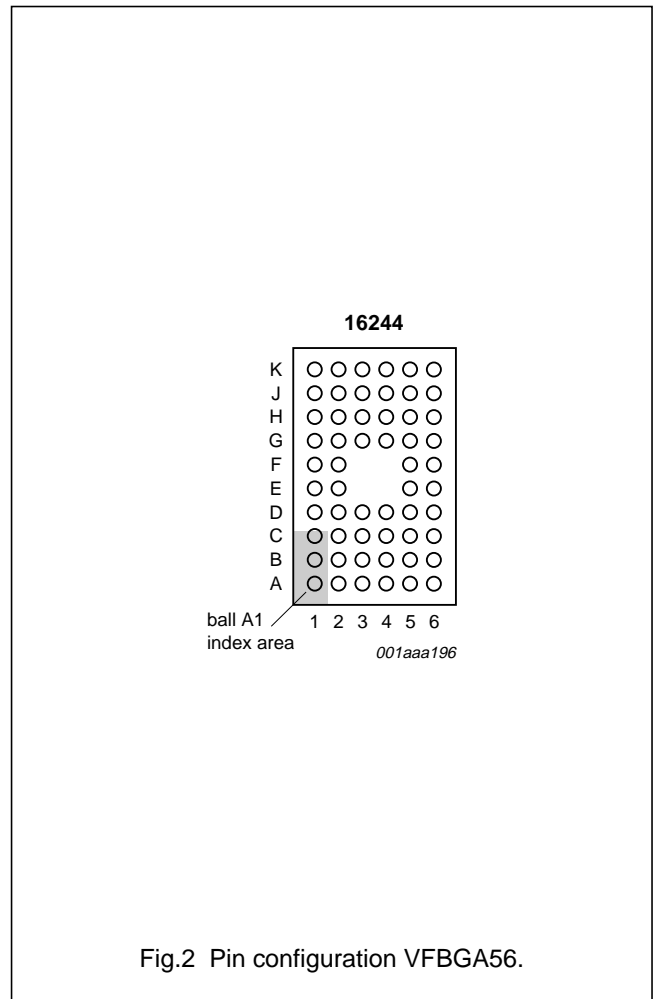
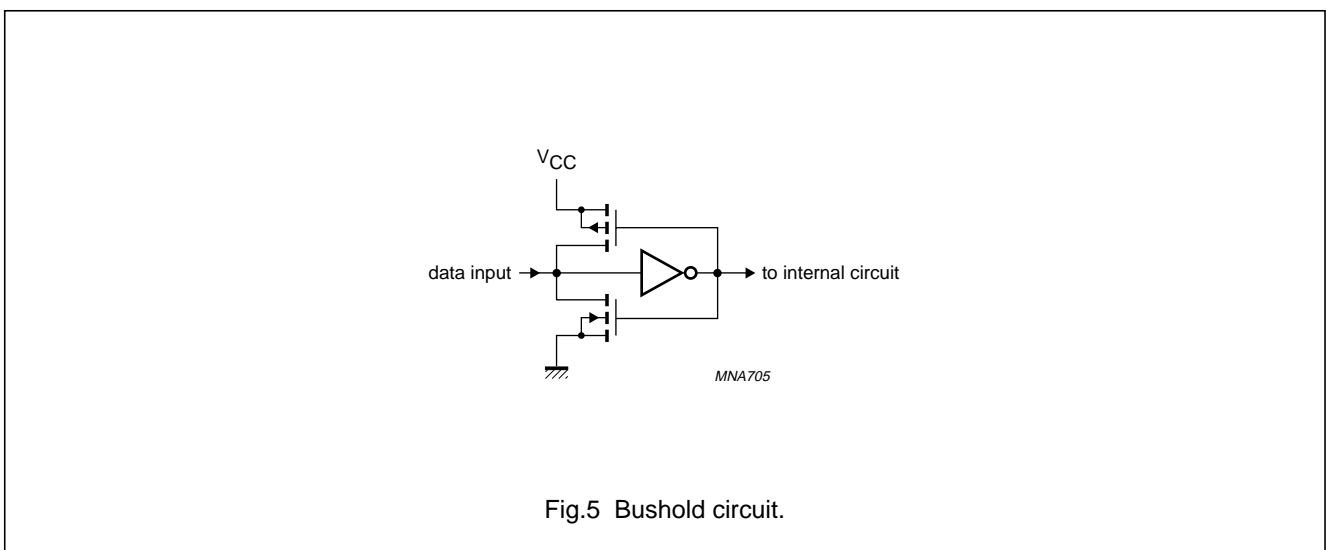
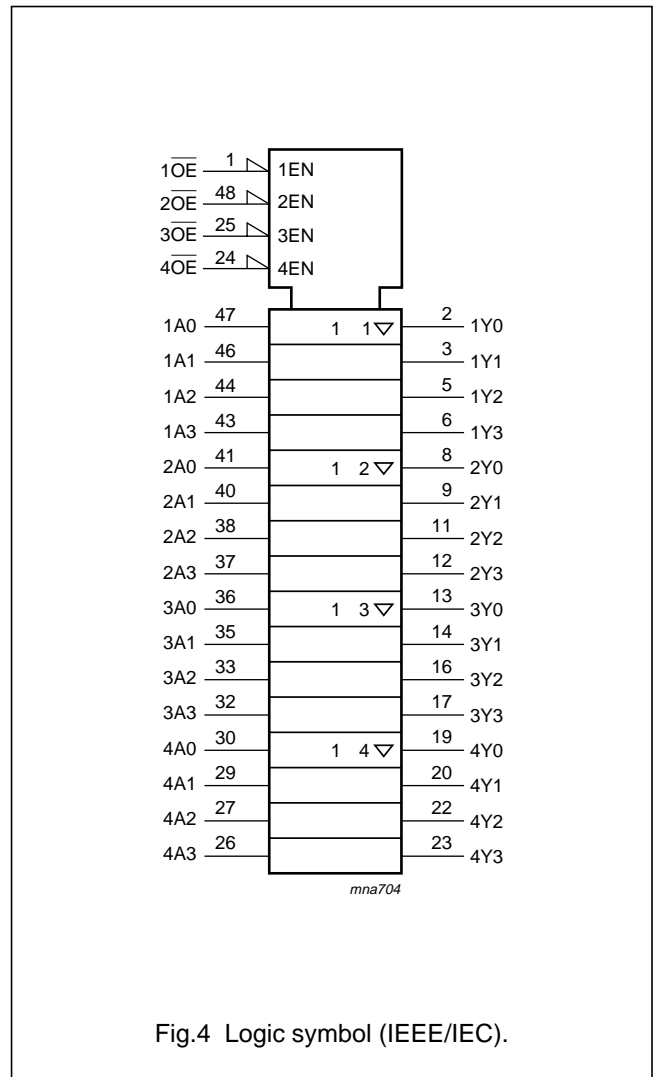
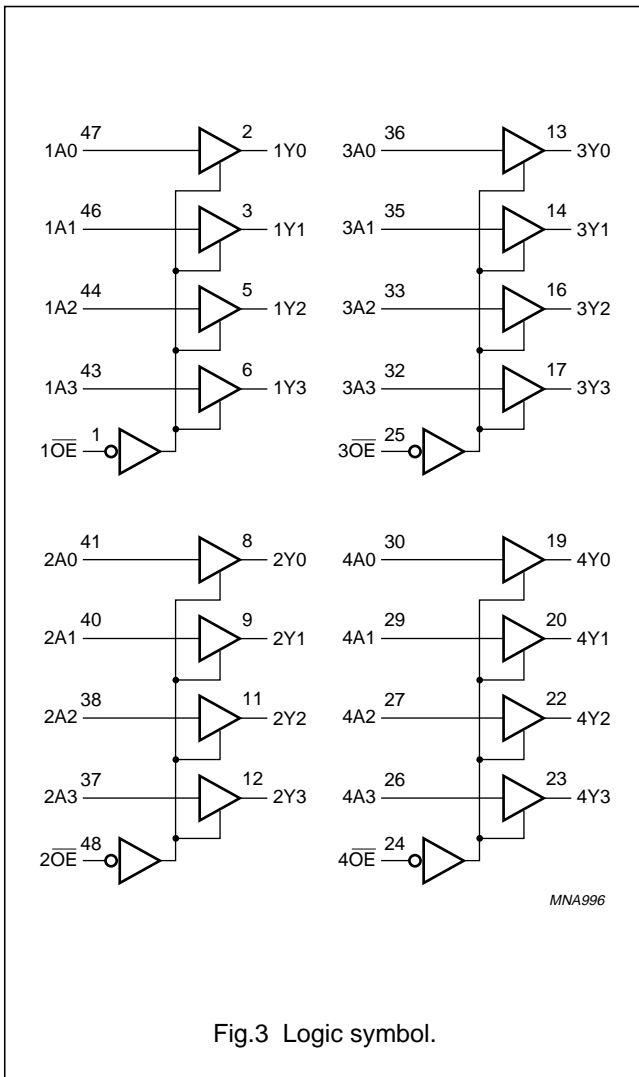


Fig.2 Pin configuration VFBGA56.

16-bit buffer/line driver; 5 V input/output tolerant; 3-state

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---------------------------------|-------------------------------|--------------------------------|------|-----------------|------|
| V _{CC} | supply voltage | for maximum speed performance | 2.7 | 3.6 | V |
| | | for low voltage applications | 1.2 | 3.6 | V |
| V _I | input voltage | | 0 | 5.5 | V |
| V _O | output voltage | output HIGH or LOW state | 0 | V _{CC} | V |
| | | output 3-state | 0 | 5.5 | V |
| T _{amb} | operating ambient temperature | in free air | -40 | +125 | °C |
| t _r , t _f | input rise and fall times | V _{CC} = 1.2 to 2.7 V | 0 | 20 | ns/V |
| | | V _{CC} = 2.7 to 3.6 V | 0 | 10 | ns/V |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------------------------|--|--|------|-----------------------|------|
| V _{CC} | supply voltage | | -0.5 | +6.5 | V |
| I _{IK} | input diode current | V _I < 0 | - | -50 | mA |
| V _I | input voltage | note 1 | -0.5 | +6.5 | V |
| I _{OK} | output diode current | V _O > V _{CC} or V _O < 0 | - | ±50 | mA |
| V _O | output voltage | output HIGH or LOW state; note 1 | -0.5 | V _{CC} + 0.5 | V |
| | | output 3-state; note 1 | -0.5 | +6.5 | V |
| I _O | output source or sink current | V _O = 0 to V _{CC} | - | ±50 | mA |
| I _{CC} , I _{GND} | V _{CC} or GND current | | - | ±100 | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | power dissipation SSOP and TSSOP package VFPGA package | T _{amb} = -40 to +125 °C; note 2 | - | 500 | mW |
| | | T _{amb} = -40 to +125 °C; note 3 | - | 1000 | mW |

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
3. Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

**16-bit buffer/line driver; 5 V input/output
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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|--|---|---|---------------------|-----------------------|-----------------|------|------|
| | | OTHER | V _{CC} (V) | | | | |
| T_{amb} = -40 to +85 °C; note 1 | | | | | | | |
| V _{IH} | HIGH-level input voltage | | 1.2 | V _{CC} | - | - | V |
| | | | 2.7 to 3.6 | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | | 1.2 | - | - | 0 | V |
| | | | 2.7 to 3.6 | - | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} I _O = -100 µA | 2.7 to 3.6 | V _{CC} - 0.2 | V _{CC} | - | V |
| | | I _O = -12 mA | 2.7 | V _{CC} - 0.5 | - | - | V |
| | | I _O = -18 mA | 3.0 | V _{CC} - 0.6 | - | - | V |
| | | I _O = -24 mA | 3.0 | V _{CC} - 0.8 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} I _O = 100 µA | 2.7 to 3.6 | - | 0 | 0.20 | V |
| | | I _O = 12 mA | 2.7 | - | - | 0.40 | V |
| | | I _O = 24 mA | 3.0 | - | - | 0.55 | V |
| I _{LI} | input leakage current | V _I = 5.5 V or GND; note 2 | 3.6 | - | ±0.1 | ±5 | µA |
| I _{OZ} | 3-state output OFF-state current | V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; note 2 | 3.6 | - | 0.1 | ±5 | µA |
| I _{off} | power-off leakage supply current | V _I or V _O = 5.5 V | 0.0 | - | 0.1 | ±10 | µA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 | 3.6 | - | 0.1 | 20 | µA |
| ΔI _{CC} | additional quiescent supply current per input pin | V _I = V _{CC} - 0.6 V; I _O = 0 | 2.7 to 3.6 | - | 5 | 500 | µA |
| I _{BH} | bushold LOW sustaining current | V _I = 0.8 V; notes 3 and 4 | 3.0 | 75 | - | - | µA |
| I _{BHH} | bushold HIGH sustaining current | V _I = 2.0 V; notes 3 and 4 | 3.0 | -75 | - | - | µA |
| I _{BHLO} | bushold LOW overdrive current | notes 3 and 5 | 3.6 | 500 | - | - | µA |
| I _{BHHO} | bushold HIGH overdrive current | notes 3 and 5 | 3.6 | -500 | - | - | µA |

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| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---------------------|------------------------|------|------|------|
| | | OTHER | V _{CC} (V) | | | | |
| T_{amb} = -40 to +125 °C | | | | | | | |
| V _{IH} | HIGH-level input voltage | | 1.2 | V _{CC} | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | V |
| V _{IL} | LOW-level input voltage | | 1.2 | – | – | 0 | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | 2.7 to 3.6 | V _{CC} – 0.3 | – | – | V |
| | | I _O = –100 μA | 2.7 | V _{CC} – 0.65 | – | – | V |
| | | I _O = –12 mA | 3.0 | V _{CC} – 0.75 | – | – | V |
| | | I _O = –18 mA | 3.0 | V _{CC} – 1 | – | – | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | 2.7 to 3.6 | – | – | 0.3 | V |
| | | I _O = 100 μA | 2.7 | – | – | 0.6 | V |
| | | I _O = 12 mA | 3.0 | – | – | 0.8 | V |
| | | I _O = 24 mA | | | | | |
| I _{LI} | input leakage current | V _I = 5.5 V or GND; note 2 | 3.6 | – | – | ±20 | μA |
| I _{OZ} | 3-state output OFF-state current | V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; note 2 | 3.6 | – | – | ±20 | μA |
| I _{off} | power-off leakage supply current | V _I or V _O = 5.5 V | 0.0 | – | – | ±20 | μA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 | 3.6 | – | – | 80 | μA |
| ΔI _{CC} | additional quiescent supply current per input pin | V _I = V _{CC} – 0.6 V; I _O = 0 | 2.7 to 3.6 | – | – | 5000 | μA |
| I _{BH} | bushold LOW sustaining current | V _I = 0.8 V; notes 3 and 4 | 3.0 | 60 | – | – | μA |
| I _{BHH} | bushold HIGH sustaining current | V _I = 2.0 V; notes 3 and 4 | 3.0 | –60 | – | – | μA |
| I _{BHLO} | bushold LOW overdrive current | notes 3 and 5 | 3.6 | 500 | – | – | μA |
| I _{BHHO} | bushold HIGH overdrive current | notes 3 and 5 | 3.6 | –500 | – | – | μA |

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For bushold parts, the bushold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input pin.
3. Valid for data inputs of bushold parts (74LVCH16244A) only. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data inputs holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.

16-bit buffer/line driver; 5 V input/output
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AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500 \Omega$.

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|--|------------------|---------------------|------|--------------------|------|------|
| | | WAVEFORMS | V _{CC} (V) | | | | |
| T_{amb} = -40 to +85 °C; note1 | | | | | | | |
| t _{PHL} /t _{PLH} | propagation delay nAn to nYn | see Figs 6 and 8 | 1.2 | – | 11.0 | – | ns |
| | | | 2.7 | 1.0 | – | 4.7 | ns |
| | | | 3.0 to 3.6 | 1.1 | 3.0 ⁽²⁾ | 4.1 | ns |
| t _{PZH} /t _{PZL} | 3-state output enable time n \overline{OE} to nYn | see Figs 7 and 8 | 1.2 | – | 15.0 | – | ns |
| | | | 2.7 | 1.0 | – | 5.8 | ns |
| | | | 3.0 to 3.6 | 1.0 | 3.5 ⁽²⁾ | 4.6 | ns |
| t _{PHZ} /t _{PLZ} | 3-state output disable time n \overline{OE} to nYn | see Figs 7 and 8 | 1.2 | – | 10.0 | – | ns |
| | | | 2.7 | 1.0 | – | 6.2 | ns |
| | | | 3.0 to 3.6 | 1.8 | 3.7 ⁽²⁾ | 5.2 | ns |
| T_{amb} = -40 to +125 °C | | | | | | | |
| t _{PHL} /t _{PLH} | propagation delay nAn to nYn | see Figs 6 and 8 | 1.2 | – | – | – | ns |
| | | | 2.7 | 1.0 | – | 6.0 | ns |
| | | | 3.0 to 3.6 | 1.1 | – | 5.5 | ns |
| t _{PZH} /t _{PZL} | 3-state output enable time n \overline{OE} to nYn | see Figs 7 and 8 | 1.2 | – | – | – | ns |
| | | | 2.7 | 1.0 | – | 7.5 | ns |
| | | | 3.0 to 3.6 | 1.0 | – | 6.0 | ns |
| t _{PHZ} /t _{PLZ} | 3-state output disable time n \overline{OE} to nYn | see Figs 7 and 8 | 1.2 | – | – | – | ns |
| | | | 2.7 | 1.0 | – | 8.0 | ns |
| | | | 3.0 to 3.6 | 1.8 | – | 6.5 | ns |

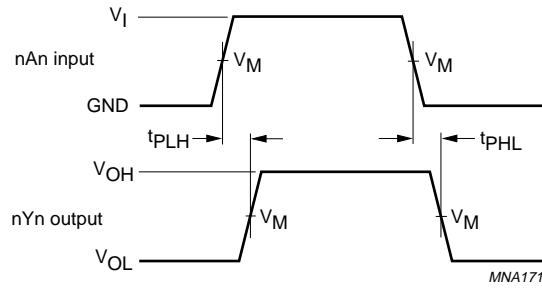
Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. These typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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AC WAVEFORMS



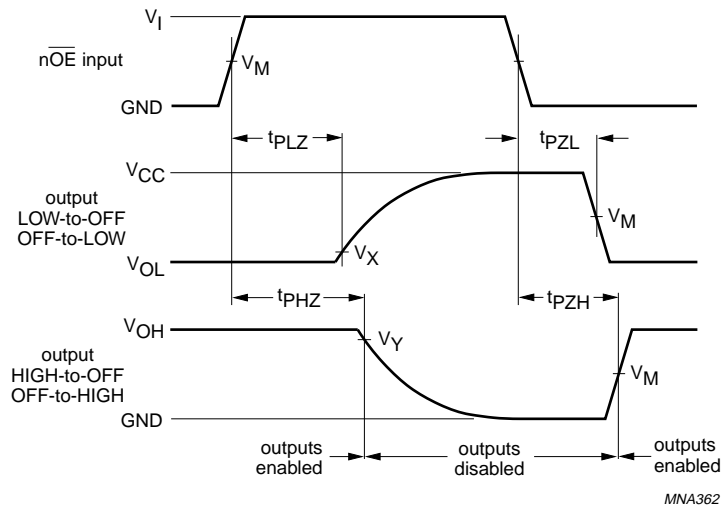
| V_{CC} | V_M | INPUT | |
|--------------|---------------------|----------|---------------|
| | | V_I | $t_r = t_f$ |
| 1.2 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.5 ns |
| 2.7 V | 1.5 V | 2.7 V | ≤ 2.5 ns |
| 3.0 to 3.6 V | 1.5 V | 2.7 V | ≤ 2.5 ns |

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 The input nAn to output nYn propagation delays.

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| V _{CC} | V _M | INPUT | |
|-----------------|-----------------------|-----------------|---------------------------------|
| | | V _I | t _r = t _f |
| 1.2 V | 0.5 × V _{CC} | V _{CC} | ≤ 2.5 ns |
| 2.7 V | 1.5 V | 2.7 V | ≤ 2.5 ns |
| 3.0 to 3.6 V | 1.5 V | 2.7 V | ≤ 2.5 ns |

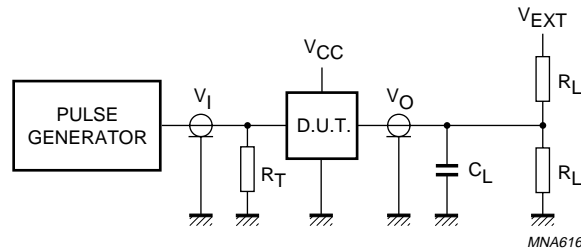
V_X = V_{OL} + 0.3 V at V_{CC} ≥ 2.7 V;
 V_X = V_{OL} + 0.1 V at V_{CC} < 2.7 V;
 V_Y = V_{OH} - 0.3 V at V_{CC} ≥ 2.7 V;
 V_Y = V_{OH} - 0.1 V at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.

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| V _{CC} | V _I | C _L | R _L | V _{EXT} | | |
|-----------------|-----------------|----------------|----------------------|------------------------------------|------------------------------------|------------------------------------|
| | | | | t _{PLH} /t _{PHL} | t _{PZH} /t _{PHZ} | t _{PZL} /t _{PLZ} |
| 1.2 V | V _{CC} | 50 pF | 500 Ω ⁽¹⁾ | open | GND | 2 × V _{CC} |
| 2.7 V | 2.7 V | 50 pF | 500 Ω | open | GND | 2 × V _{CC} |
| 3.0 to 3.6 V | 2.7 V | 50 pF | 500 Ω | open | GND | 2 × V _{CC} |

Note

1. The circuit performs better when R_L = 1000 Ω.

Definitions for test circuits:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

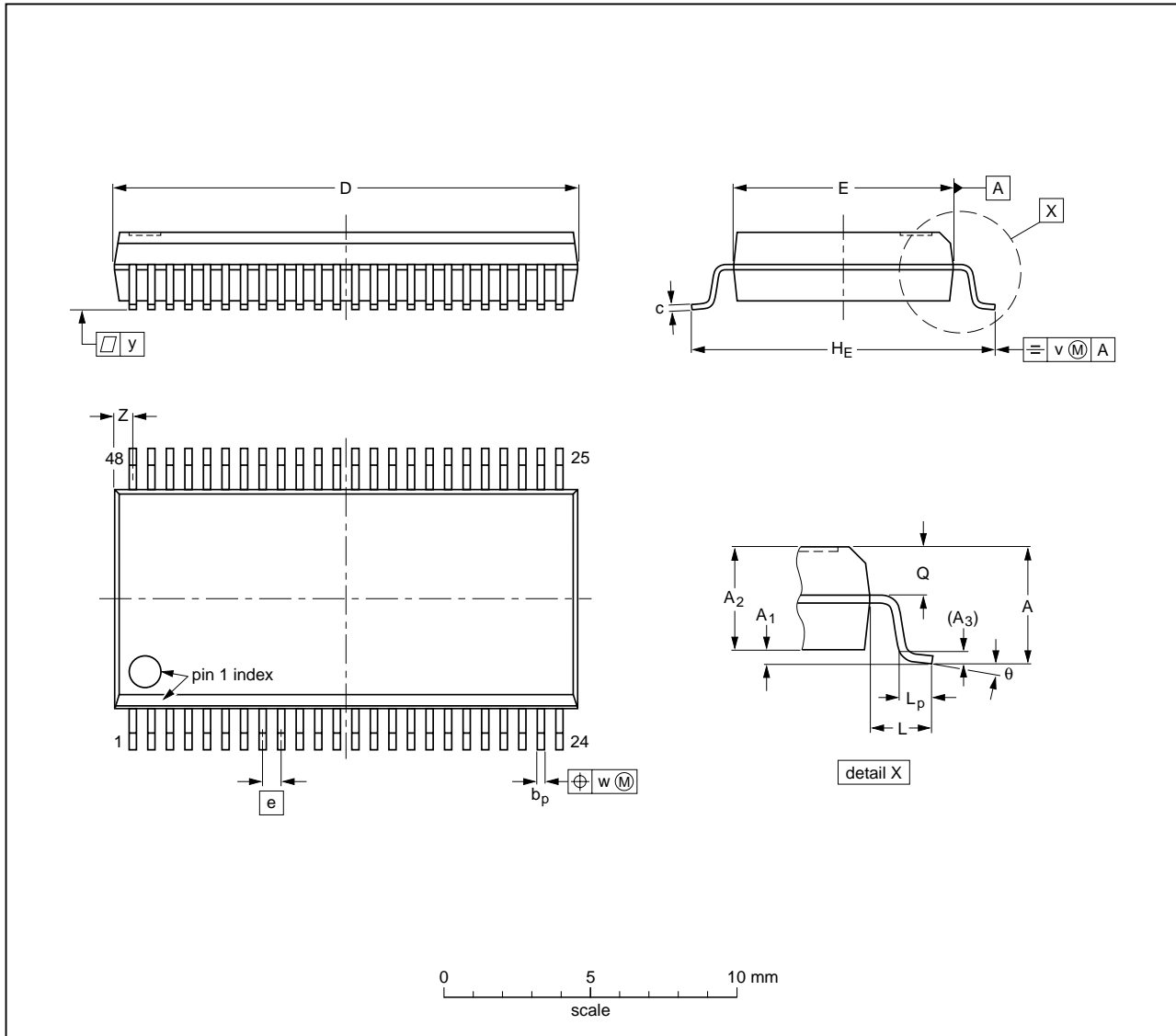
16-bit buffer/line driver; 5 V input/output tolerant; 3-state

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PACKAGE OUTLINES

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm | 2.8 | 0.4 0.2 | 2.35 2.20 | 0.25 | 0.3 0.2 | 0.22 0.13 | 16.00 15.75 | 7.6 7.4 | 0.635 | 10.4 10.1 | 1.4 | 1.0 0.6 | 1.2 1.0 | 0.25 | 0.18 | 0.1 | 0.85 0.40 | 8° 0° |

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

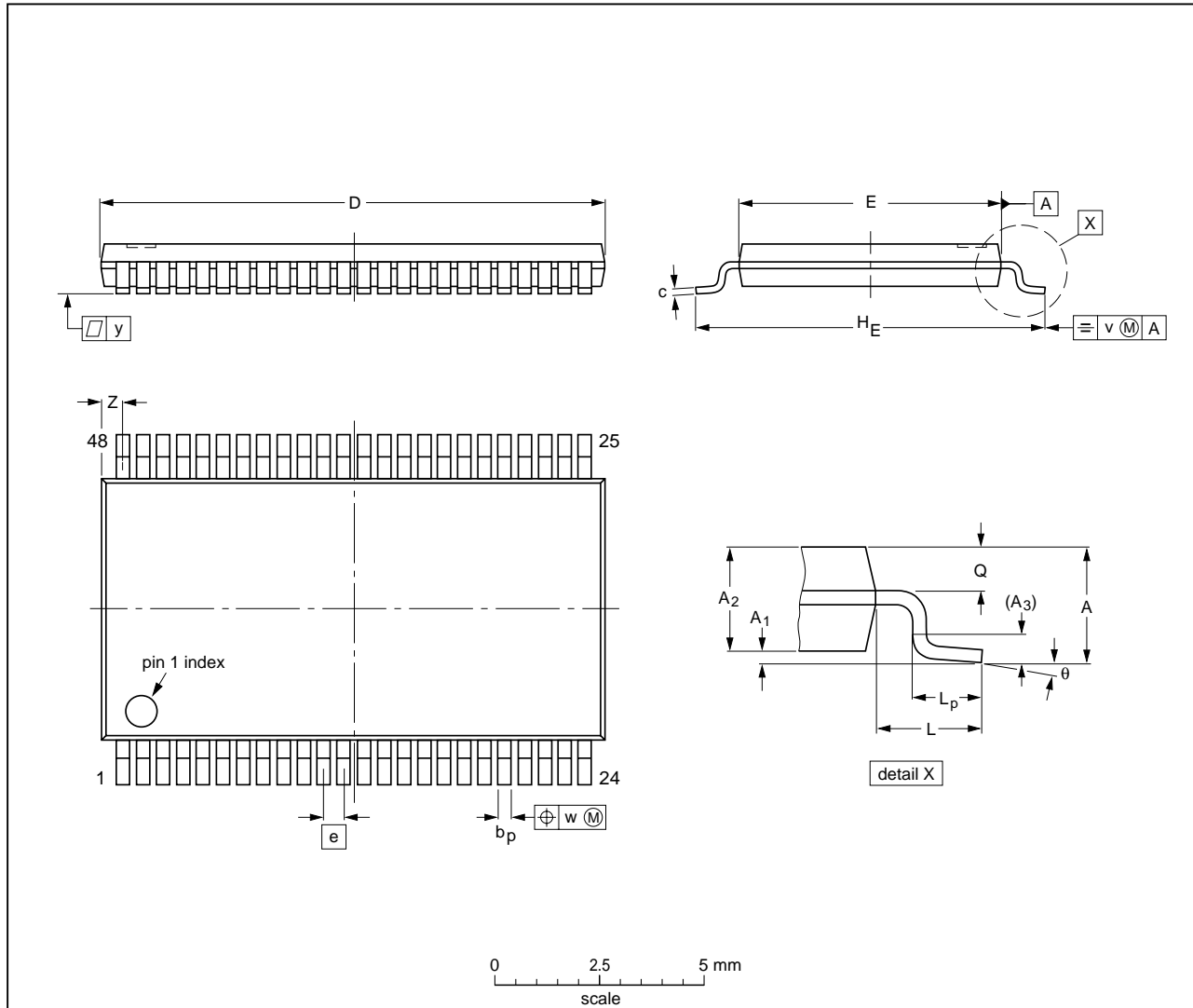
| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | |
| SOT370-1 | | MO-118 | | | 99-12-27 03-02-19 |

16-bit buffer/line driver; 5 V input/output tolerant; 3-state

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74LVCH16244A

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|-----|----------------|---|----------------|--------------|------|------|-----|------------|----------|
| mm | 1.2 | 0.15 0.05 | 1.05 0.85 | 0.25 | 0.28 0.17 | 0.2 0.1 | 12.6 12.4 | 6.2 6.0 | 0.5 | 8.3 7.9 | 1 | 0.8 0.4 | 0.50 0.35 | 0.25 | 0.08 | 0.1 | 0.8 0.4 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

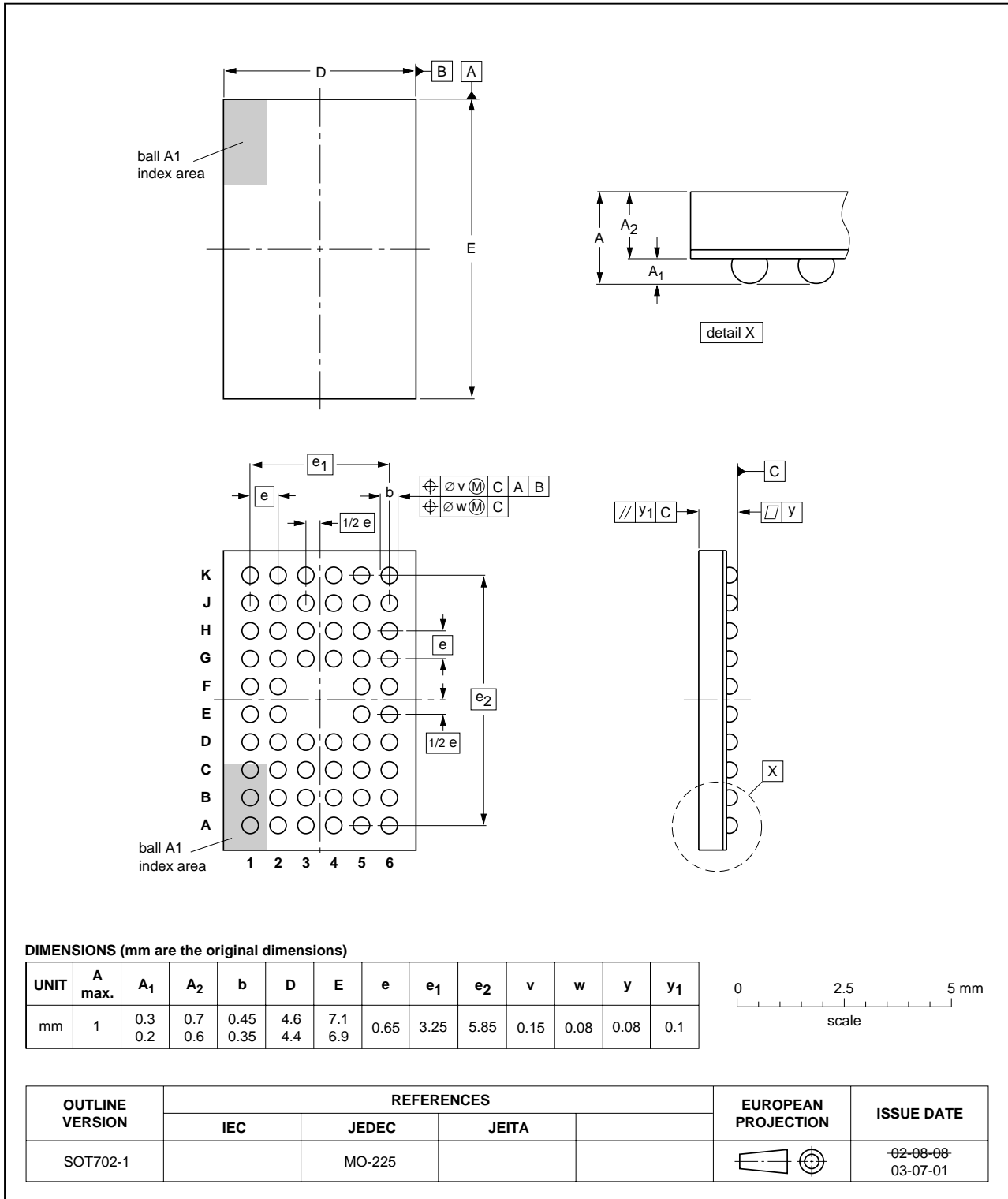
| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | |
| SOT362-1 | | MO-153 | | | 99-12-27 03-02-19 |

16-bit buffer/line driver; 5 V input/output tolerant; 3-state

74LVC16244A;
74LVCH16244A

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm

SOT702-1



16-bit buffer/line driver; 5 V input/output
tolerant; 3-state

74LVC16244A;
74LVCH16244A

DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾⁽³⁾ | DEFINITION |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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