DATA SHEET

MOS INTEGRATED CIRCUIT

μPD6325, μPD6326, μPD6335, μPD6336

QUAD/OCTAL 6BIT D/A CONVERTER
CMOS LSI

DESCRIPTION

μPD6325 Serise are 6 bit D/A Converter for control volumn, brightness, contrast, color or tone of TV set.
The data are transferring serially from micro-computer.

μPD6325 Serise Line-up	QUAD D/A	OCTAL D/A
D/A output is consist of Emitter follower buffer	μPD6325C, 6325G	μPD6326C
Non buffer output	μPD6335C, 6335G	μPD6336C

FEATURES

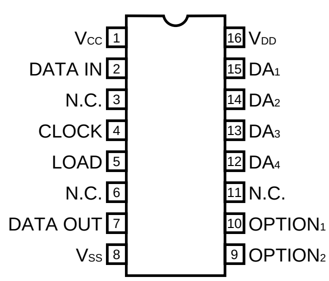
- R-2R ladder D/A
- Serial Data input (DATA IN, CLOCK, LOAD)
- Power supply voltage of interface is 5 V (V_{CC}) and D/A reference voltage is free (V_{CC} to 15 V).

ORDERING INFORMATION

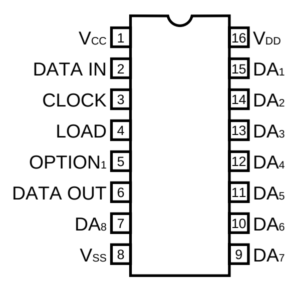
Part No.	Package
μPD6325C	16-pin plastic DIP (300 mil)
μPD6325G	16-pin plastic SOP (300 mil)
μPD6326C	16-pin plastic DIP (300 mil)
μPD6335C	16-pin plastic DIP (300 mil)
μPD6335G	16-pin plastic SOP (300 mil)
μPD6336C	16-pin plastic DIP (300 mil)

PIN CONNECTION DIAGRAM (Top View)

μPD6325, μPD6335

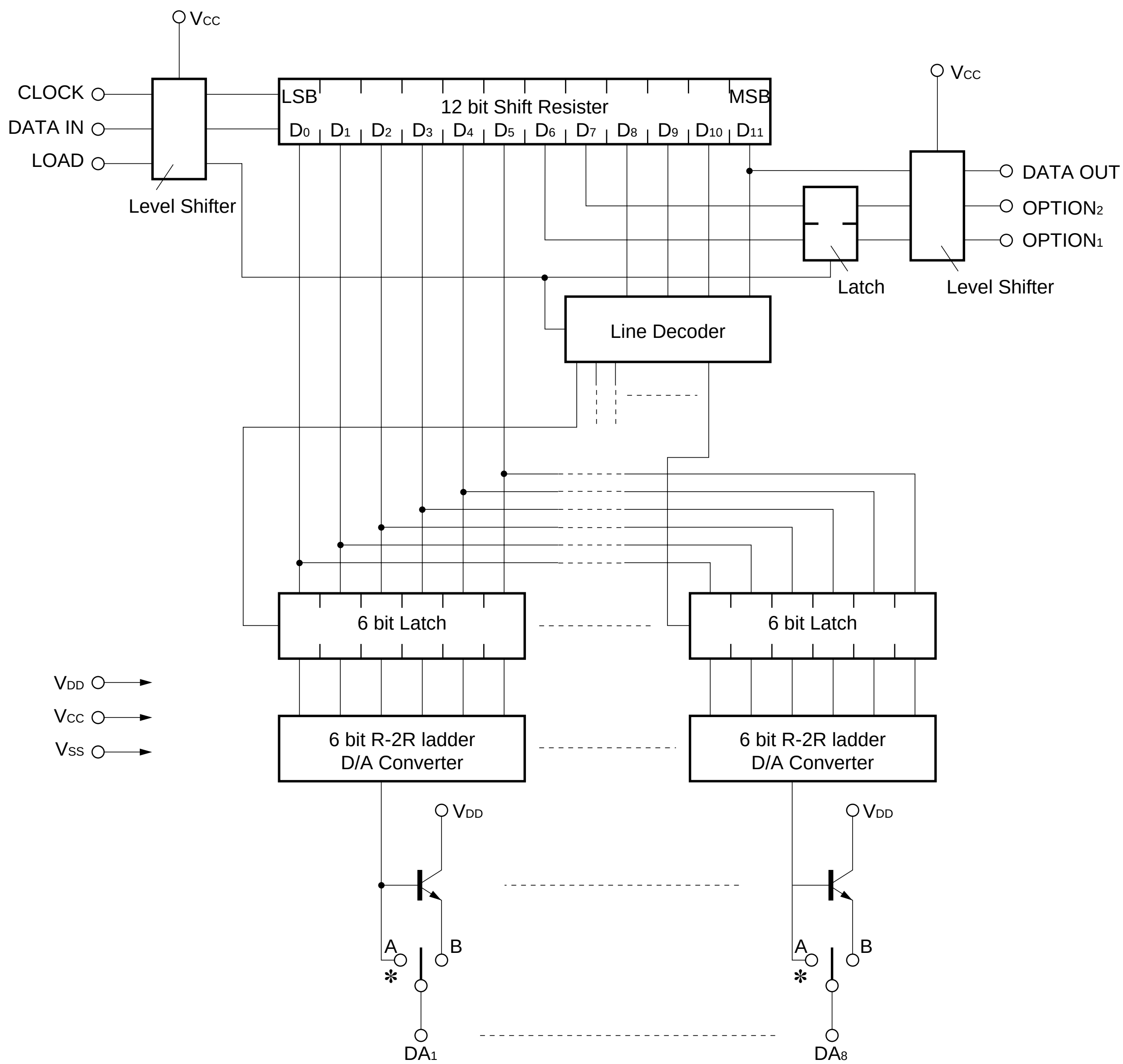


μPD6326, μPD6336



Document No. G10654EJ6V0DS00 (6th edition)
Date Published November 1997 N
Printed in Japan

BLOCK DIAGRAM



*A ------ μPD6335, μPD6336
B ------ μPD6325, μPD6326

μPD6325, μPD6326 have Quad D/As.

PIN CONFIGURATION

Pin No. μPD6325/6335	Pin No. μPD6326/6336	Symbol	Pin Name	Function
1	1	V_{CC}	Interface Power Supply	This pin is used to interface with the control IC (ex. micro processor). Supply the voltage high level of the control IC.
2	2	DATA IN	Serial Data Input	Control data input terminal. Data is read in synchronization with the clocks input to the CLOCK terminal.
4	3	CLOCK	Shift Clock Input	Data read clock input terminal. The Data input to the DATA IN terminal is read at the leading edge of the clock.
5	4	LOAD	Load Pulse Input	This terminal is used to input Load signals after inputting serial data. 12 bit data is read after leading edge of a pulse input to the LOAD terminal.
7	6	DATA OUT	Serial Data Output	Serial data output terminal. The final stage data of 12 bit shift register appeares on this terminal in synchronization with shift clock.
8	8	V_{SS}	Ground	System ground.
9	–	$OPTION_2$	Expantion Output Port	D_7 the data of the shift register appears on this terminal. (Only μPD6325 and μPD6335)
10	5	$OPTION_1$	Expanttion Output Port	D_6 the data of the shift register appears on this terminal.
–	7	DA_8	Analog Output Channel 8	Analog Output
–	9	DA_7	Analog Output Channel 7	Analog Output
–	10	DA_6	Analog Output Channel 6	Analog Output
–	11	DA_5	Analog Output Channel 5	Analog Output
12	12	DA_4	Analog Output Channel 4	Analog Output
13	13	DA_3	Analog Output Channel 3	Analog Output
14	14	DA_2	Analog Output Channel 2	Analog Output
15	15	DA_1	Analog Output Channel 1	Analog Output
16	16	V_{DD}	Power Supply	Reference Voltage for D/A converters. Analog output voltage range is GND to V_{DD}.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Supply Voltage	V_{DD},V_{CC}	–0.5 to +18, $V_{CC} \le V_{DD}$	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Input Current	I_{IN}	10	mA
Emitter Follower Current	I_{OE}	10	mA
Power Dissipation	P_D	500*/200**	mW
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C

*DIP

**SOP

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD}	V_{CC}		15	V	$V_{CC} \le V_{DD}$
Supply Voltage of Interface	V_{CC}	4.5	5.0	5.5	V	$V_{CC} \le V_{DD}$
Low Level Input Voltage	V_{IL}			0.8	V	V_{CC} = 5 V, V_{DD} = 5 to 15 V
High Level Input Voltage	V_{IH}	3.5			V	V_{CC} = 5 V, V_{DD} = 5 to 15 V
Only μPD6325 & μPD6326 Emitter Follower Power Dissipation 1	P_E/unit			5	mW	T_A = 85 °C
Emitter Follower Power Dissipation 2	P_E/unit			15	mW	T_A = 70 °C
Emitter Follower Power Dissipation 3	P_E total			25	mW	T_A = 85 °C
Emitter Follower Power Dissipation 4	P_E total			75	mW	T_A = 70 °C
TIMING CONDITIONS (T_A = –40 to +85 °C, V_{SS} = 0 V, V_{CC} = 5 V, V_{DD} = V_{CC} to 15 V)						
CLOCK High Level Width	t_{CH}	4.0			μs	
CLOCK Low Level Width	t_{CL}	10.0			μs	
CLOCK Rise Time	t_{cr}			1.0	μs	
CLOCK Fall Time	t_{cf}			1.0	μs	
DATA IN Setup Time	t_{Dsetup}	2			μs	
DATA IN Hold Time	t_{Dhold}	10			μs	
Pulse Width, LOAD High	$t_{W(LOAD)}$	4			μs	
LOAD Lead Time	t_{Llead}	10			μs	
LOAD Lag Time	t_{Llag}	10			μs	

ELECTRICAL CHARACTERISTICS

(T_A = –40 to +85°C, V_{SS} = 0 V, V_{CC} = 4.5 to 5.5 V, V_{DD} = V_{CC} to 15 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Current Consumption	I_{DD}			15	mA	No Load, for μPD6326, 6336
Current Consumption	I_{DD}			10	mA	No Load, for μPD6325, 6335
Current Consumption of Interface	I_{CC}			10	μA	No Load of DATA OUT, Static Consumption
Input Leak Current	I_{ILEAK}			±1	μA	V_{IN} = V_{CC} or V_{SS}
DATA OUT High Level Output Voltage	I_{OH}	–100			μA	V_{OH} = V_{DD} –0.5 V
DATA OUT Low Level Output Voltage	I_{OL}	100			μA	V_{OL} = 0.5 V
Emitter Follower Leak Current	I_{OLEAK}			20	μA	for μPD6325, 6326
Setling Time	$t_{DA\ set}$			10	μs	**Note**

Note μPD6325, 6326: R_L = 20 kΩ, C_L = 50 pF
μPD6335, 6336: No Load.

DATA CONFIGURATION

Data Length is 12 bit.

Last → First

LSB											MSB
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}

D/A output CONTROL BIT

D_{11}	D_{10}	D_9	D_8	Select D/A	Target device
0	0	0	0	Don't Care	μPD6325, 6326 μPD6335, 6336
0	0	0	1	DA_1	μPD6325, 6326 μPD6335, 6336
0	0	1	0	DA_2	μPD6325, 6326 μPD6335, 6336
0	0	1	1	DA_3	μPD6325, 6326 μPD6335, 6336
0	1	0	0	DA_4	μPD6325, 6326 μPD6335, 6336
0	1	0	1	DA_5	μPD6326 μPD6336
0	1	1	0	DA_6	μPD6326 μPD6336
0	1	1	1	DA_7	μPD6326 μPD6336
1	0	0	0	DA_8	μPD6326 μPD6336
1	×	×	×	Don't Care	μPD6325, 6326 μPD6335, 6336

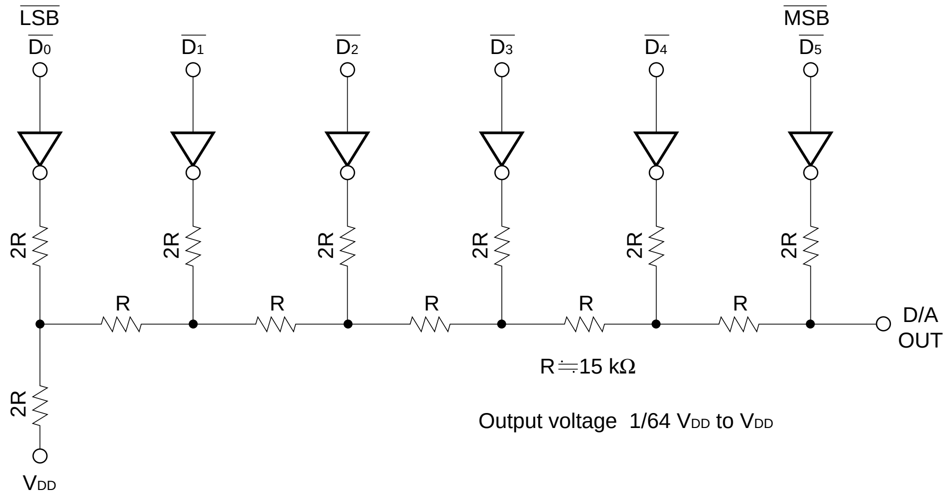
OPTION output CONTROL BIT

D_7	D_6	$OPTION_1$ out.	$OPTION_2$ out.	Note
0	0	L	L	OPTION2 is only μPD6325, 6326
0	1	H	L	OPTION2 is only μPD6325, 6326
1	0	L	H	OPTION2 is only μPD6325, 6326
1	1	H	H	OPTION2 is only μPD6325, 6326

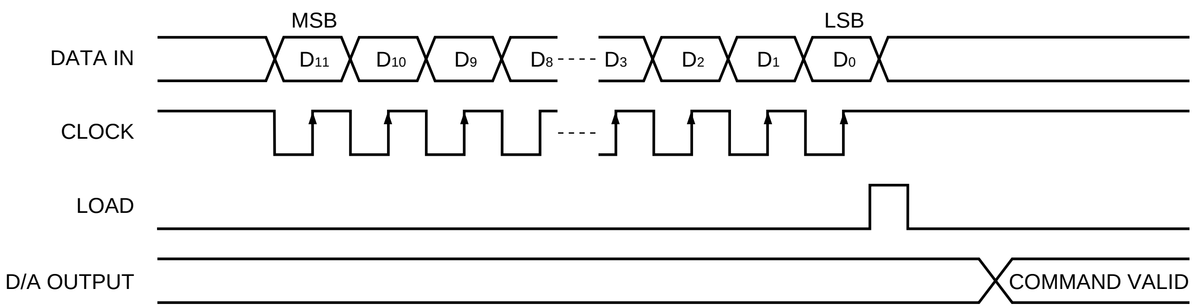
D/A Output Voltage CONTROL BIT

D_5	D_4	D_3	D_2	D_1	D_0	Output Voltage
0	0	0	0	0	0	≒ $V_{DD}/64$
0	0	0	0	0	1	≒ $2 \times V_{DD}/64$
0	0	0	0	1	0	≒ $3 \times V_{DD}/64$
0	0	0	0	1	1	≒ $4 \times V_{DD}/64$
⁝	⁝	⁝	⁝	⁝	⁝	⁝
1	1	1	1	1	0	≒ $63 \times V_{DD}/64$
1	1	1	1	1	1	≒ V_{DD}

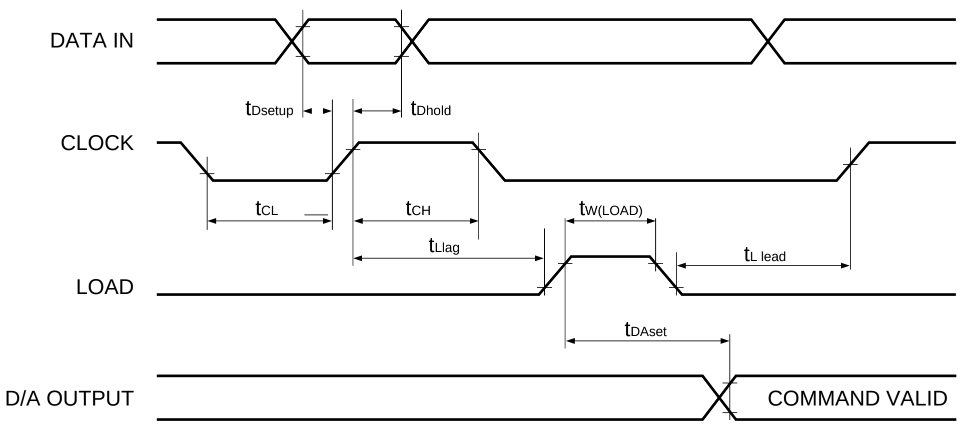
EQUIVALENT CIRCUIT OF 6 bit D/A



TIMING CHART

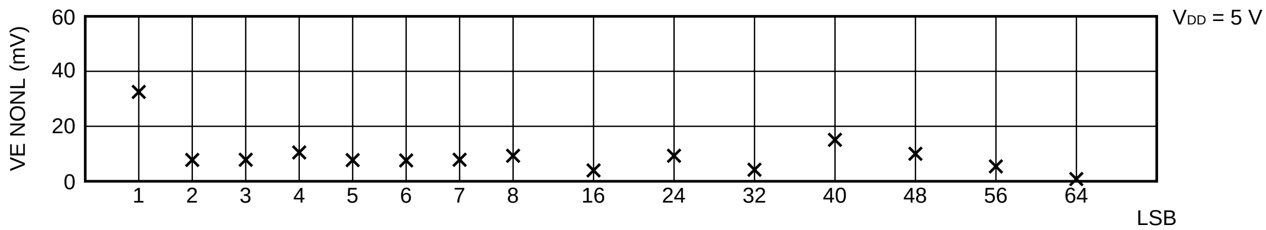


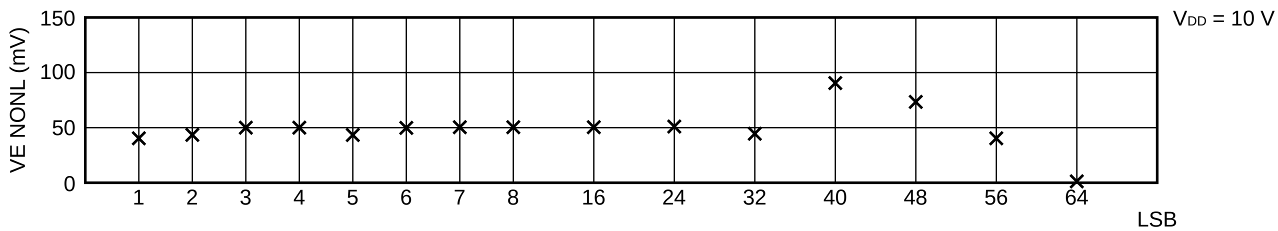
Data is loaded when LOAD is high level.

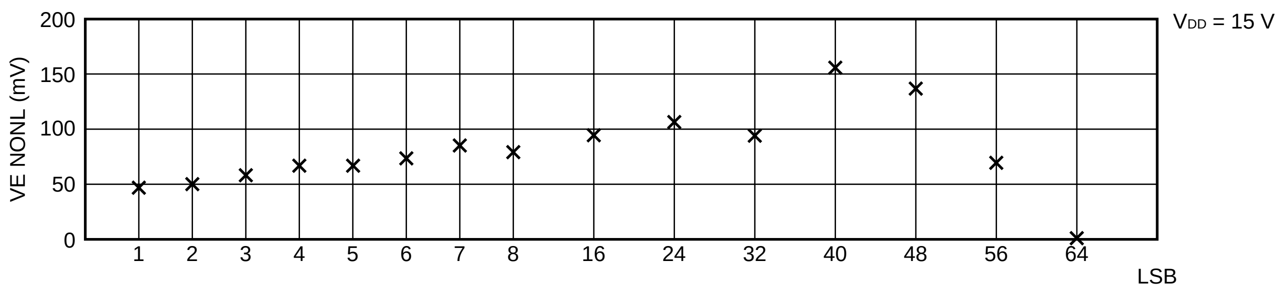


LINIARITY OF D/A OUTPUT (μPD6335, 6336) (TYP.)

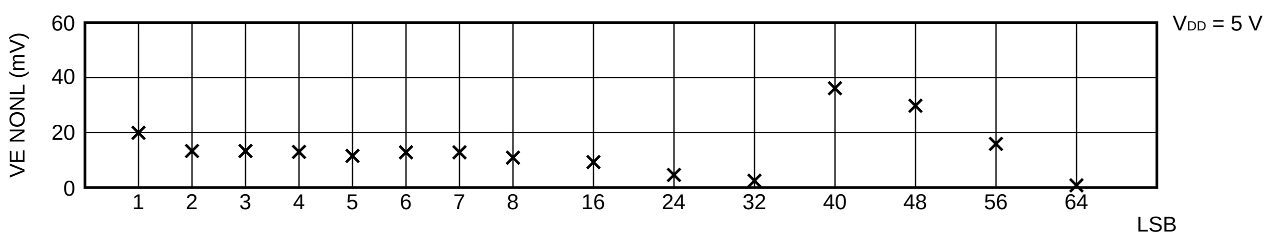
•T_A = –40 °C

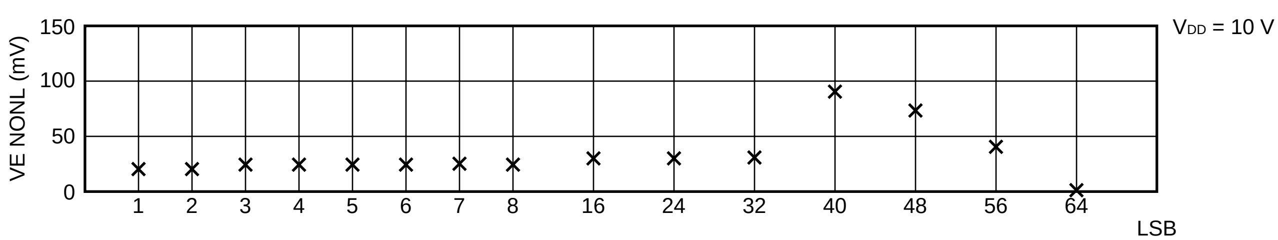


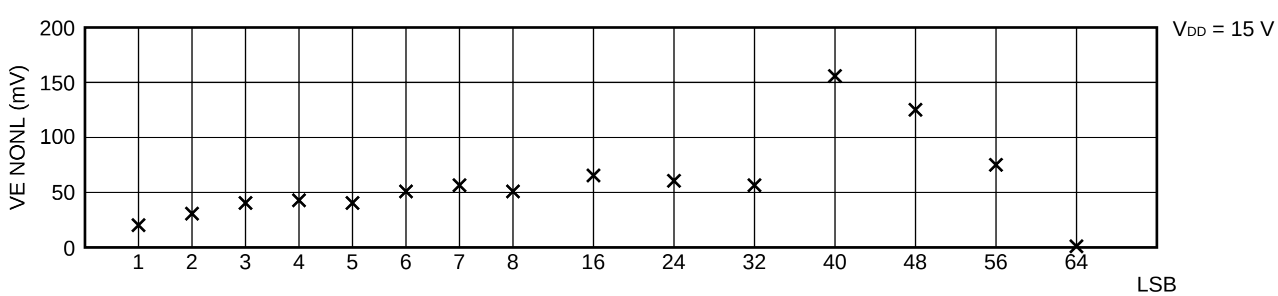




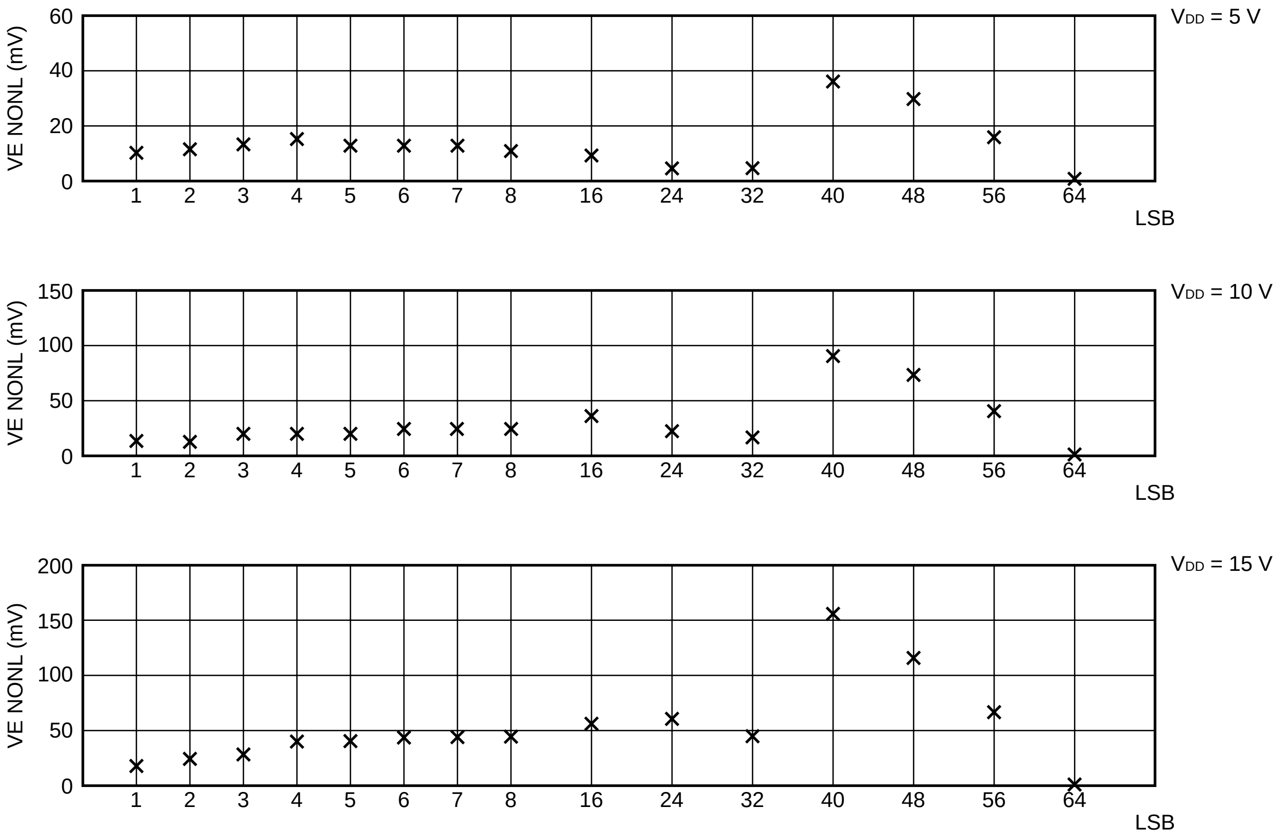
•T_A = 25 °C







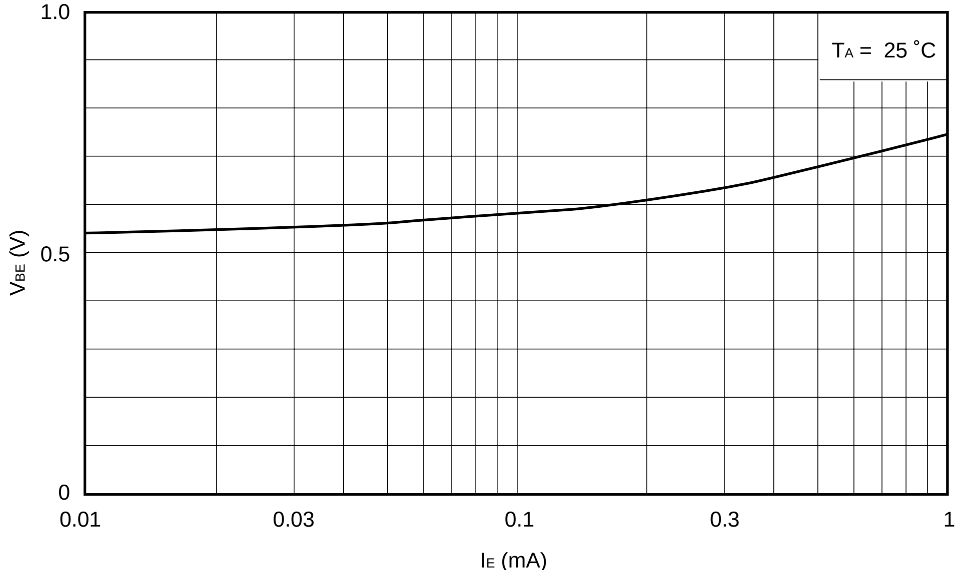
•T_A = 85 °C



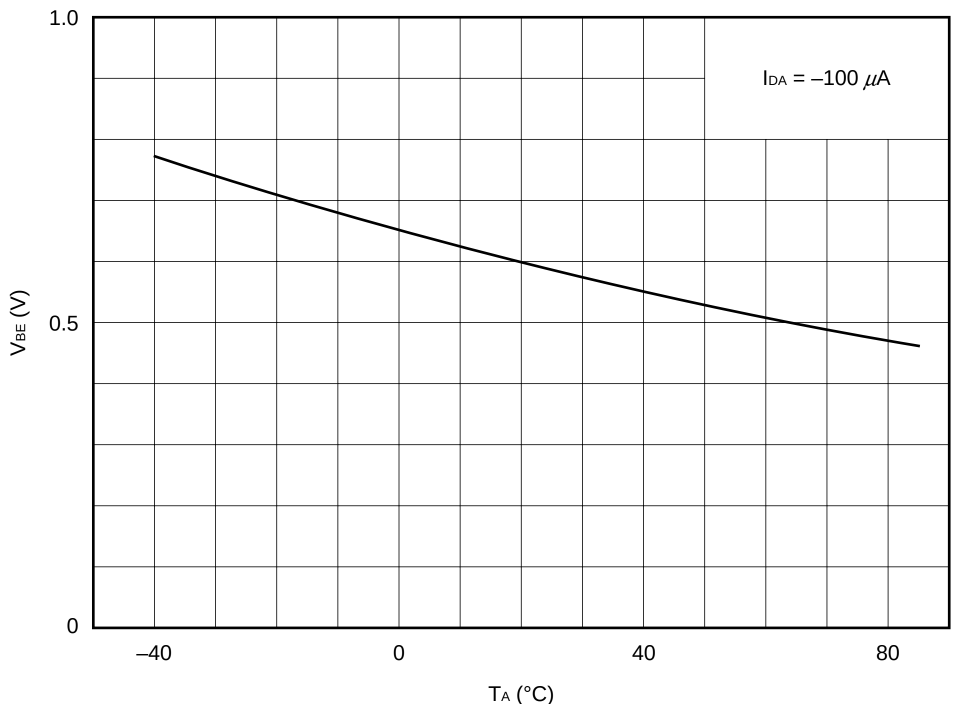
* VE NONL = (MEASUREMENT VALUE) – (IDEAL VALUE)

Characteristics of Emitter follower buffer (μPD6325, 6326)

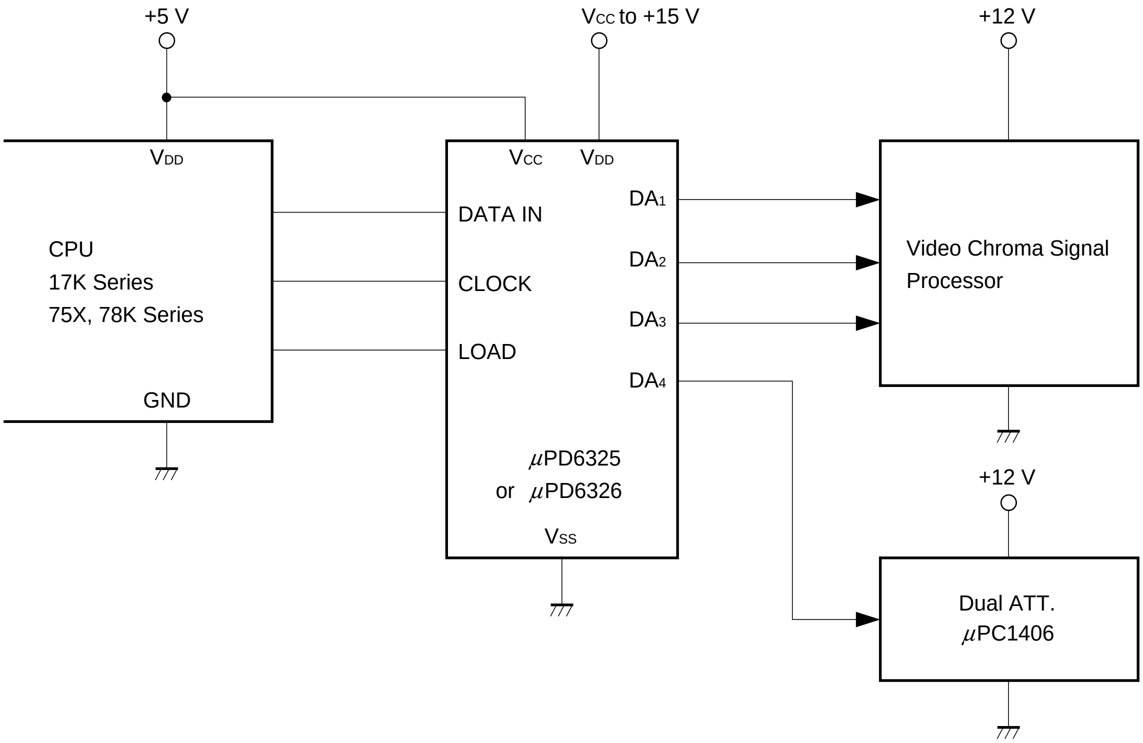
(1) V_{BE} - I_E (including R-2R's resister)



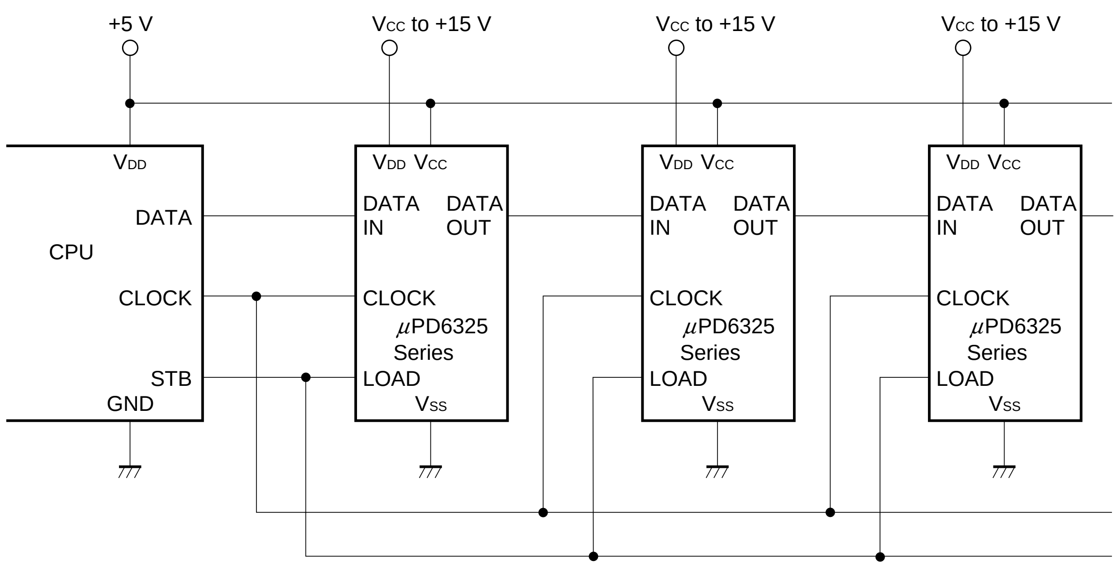
(2) V_{BE} - T_A



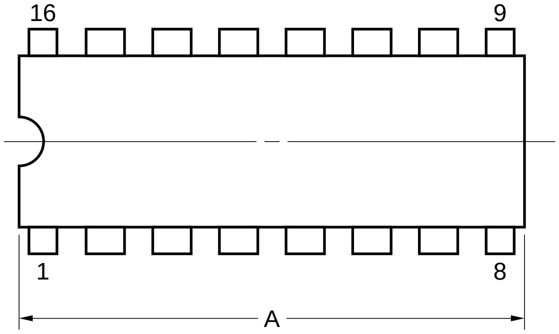
APPLICATION FOR TV SET

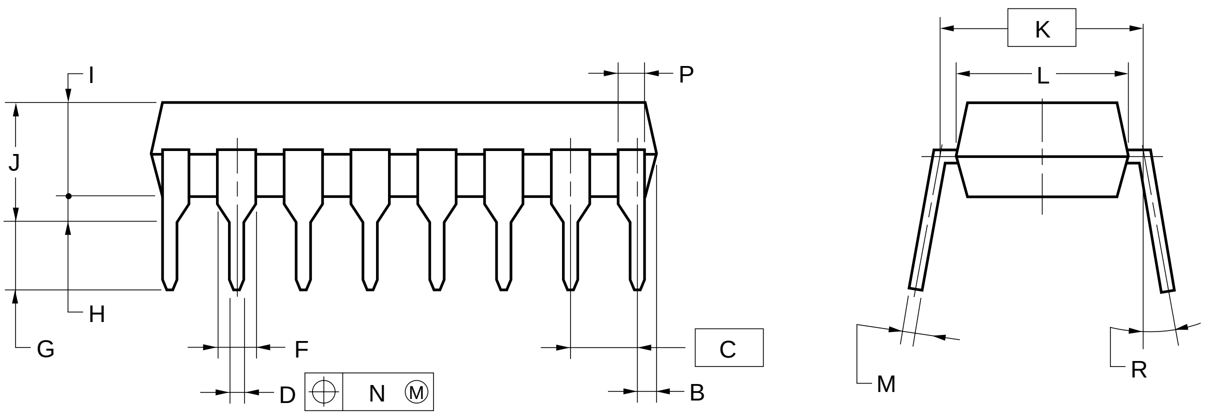


APPLICATION FOR CASCADE CONNECTING



16PIN PLASTIC DIP (300 mil)





NOTES

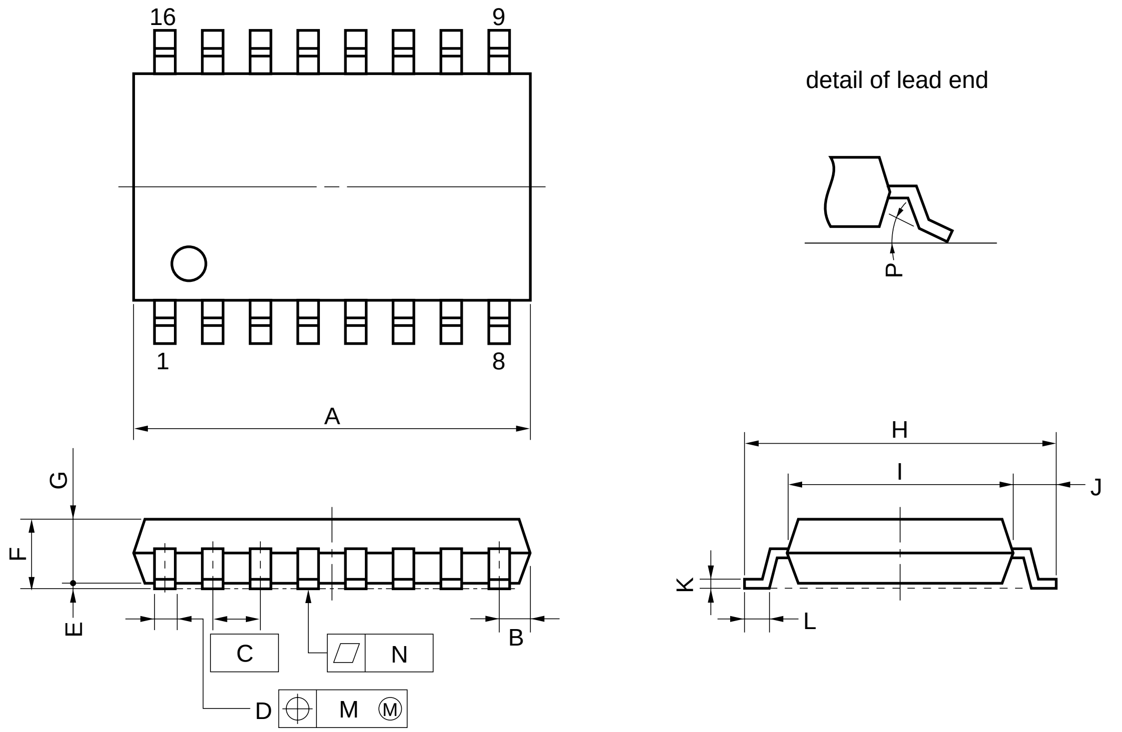
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.5±0.3	0.138±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.
R	0~15°	0~15°

P16C-100-300A,C-1

16 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P16GM-50-300B-4

REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	IEI-1212
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E

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