NEC

MOS INTEGRATED CIRCUIT

μPD3725A

5000-BIT × 3 CCD COLOR LINEAR IMAGE SENSOR

The μPD3725A is a high sensitivity 5000-bit × 3 CCD (Charge Coupled Device) color linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD3725A has 3 rows of 5000-bit photocell array and 6 rows of 2500-bit charge transferred register, so it is suitable for high resolution color image scanners and digital color copiers.

FEATURES

- Valid photocell : 5000-bit × 3
- Photocell's pitch : 14 μm
- Line distance : 112 μm (8 lines) R(red) bit-G(green) bit, Gbit-B(blue)bit
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7lx•Hour)
- Resolution : 16 dot/mm across the shorter side of a B4-size (257 × 364 mm) sheet
- Drive clock level : CMOS output under 5 V operation
- Data rate : 16 MHz MAX.
- High speed scan : 320 μs/line
- Power supply : +12 V

CHANGED POINTS from the μPD3725D-01

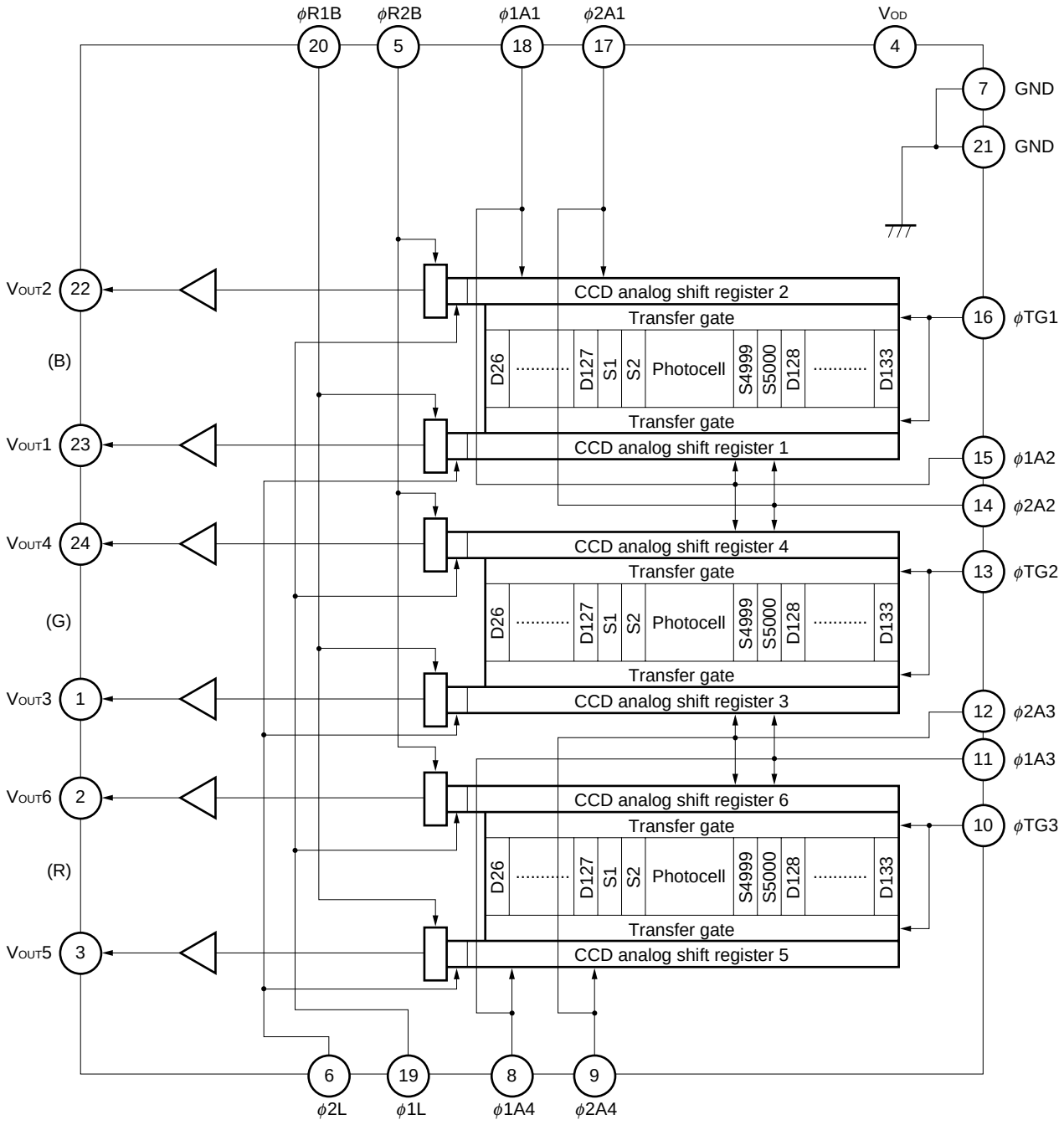
- Pins 18 and 15, 17 and 14, 11 and 8, 12 and 9 are each connected inside of the device (refer to **BLOCK DIAGRAM**).
- The specification of the total transfer efficiency (TTE) is improved from 92 % to 93.5 % (MIN.) (refer to **ELECTRICAL CHARACTERISTICS**).

ORDERING INFORMATION

Part Number	Package
μPD3725AD	CCD linear image sensor 24-pin ceramic DIP (600 mil)

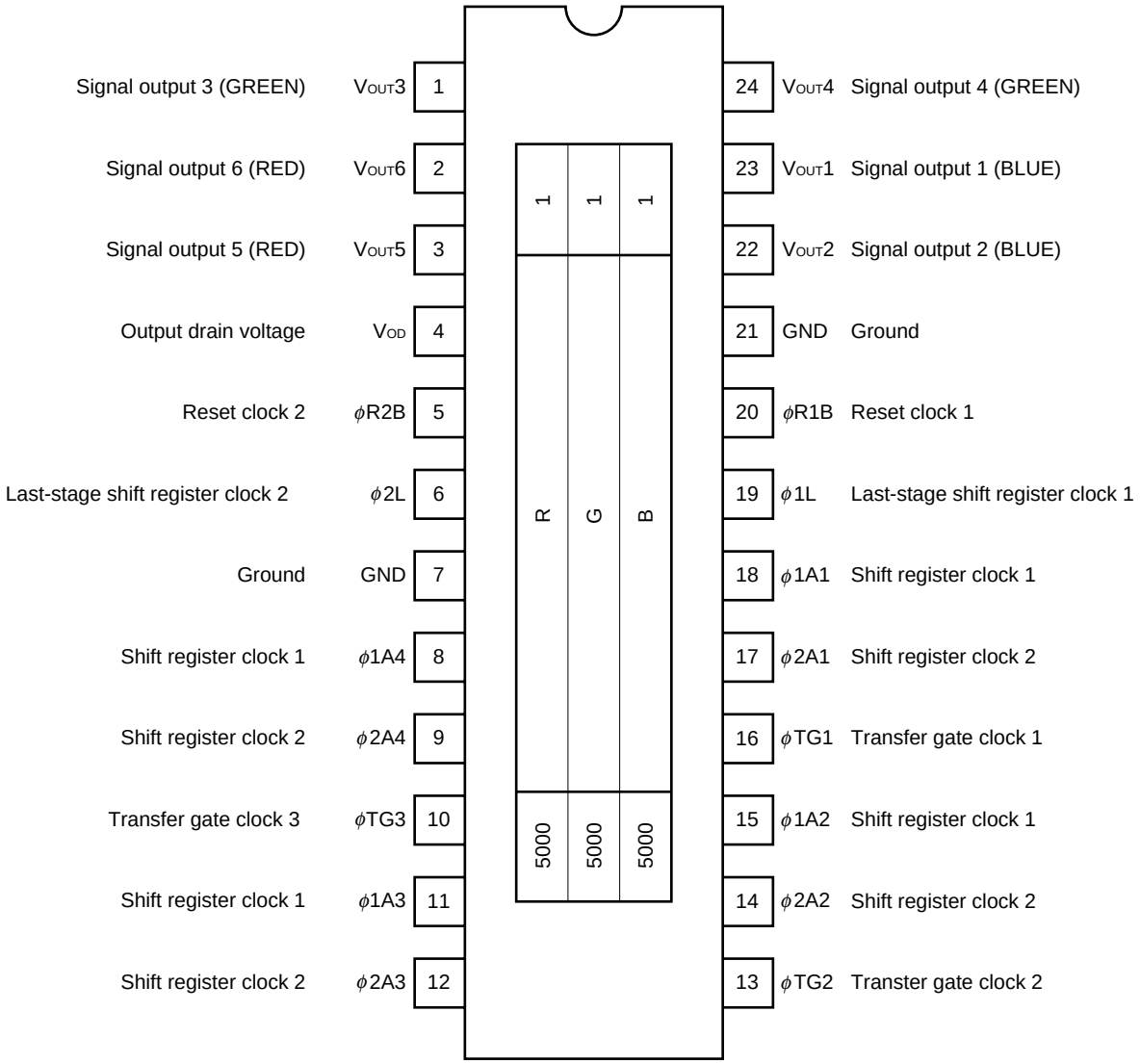
Document No. S11324EJ1V0DS00 (1st edition)
Date Published March 1996 P
Printed in Japan

BLOCK DIAGRAM

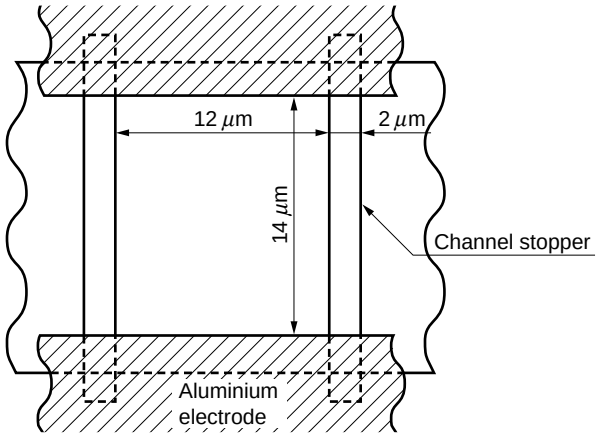


PIN CONFIGURATIONS (Top View)

CCD linear image sensor 24-pin ceramic DIP (600 mil)



PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	–0.3 to +15	V
Reset signal voltage	$V_{\phi R1B}$, $V_{\phi R2B}$	–0.3 to +15	V
Transfer gate signal voltage	$V_{\phi TG}$	–0.3 to +15	V
Operating ambient temperature	T_A	–25 to +60	°C
Storage temperature	T_{stg}	–40 to +100	°C

Caution Exposure to Absolute Maximum Rating for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

RECOMMENDED OPERATING CONDITIONS (T_A = +25 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock signal high level	$V_{\phi 1H}$, $V_{\phi 2H}$	4.5	5	5.5	V
Shift register clock signal low level	$V_{\phi 1L}$, $V_{\phi 2L}$	–0.3	0	+0.5	V
Reset signal high level	$V_{\phi R1BH}$, $V_{\phi R2BH}$	4.5	5	5.5	V
Reset signal low level	$V_{\phi R1BL}$, $V_{\phi R2BL}$	–0.3	0	+0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5	5	5.5	V
Transfer gate signal low level	$V_{\phi TGL}$	–0.3	0	+0.5	V
Data rate	$2 \times f_{\phi R1B}$, $2 \times f_{\phi R2B}$	–	2	16	MHz

Remark ϕ1: ϕ1A1 to ϕ1A4, ϕ1L
ϕ2: ϕ2A1 to ϕ2A4, ϕ2L

ELECTRICAL CHARACTERISTICS

T_A = +25 °C, V_{OD} = 12 V, $f_{øR1B}$, $f_{øR2B}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms,
light source: 3200 K halogen lamp +C-500S (infrared cut filter, t = 1 mm), input signal clock = 5 V_{p-p}

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		1.0	1.3	–	V
Saturation exposure	SER			0.3		lx•s
	SEG			0.3		lx•s
	SEB			0.6		lx•s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV		±6	±15	%
Average dark signal	ADS	Light shielding		0.1	5	mV
Dark signal non-uniformity	DSNU	Light shielding	–5	0.5	+5	mV
Power consumption	P_W			300	500	mW
Output impedance	Z_O			0.5	1	kΩ
Response	R_R		2.71	3.87	5.03	V/lx•s
	R_G		2.66	3.80	4.91	V/lx•s
	R_B		1.45	2.07	2.70	V/lx•s
Image lag	IL	V_{OUT} = 500 mV		2	5	%
Offset level[Note 1]	V_{OS}		4	6	8	V
Output fall delay time[Note 2]	t_d		33	40	47	ns
Total transfer efficiency	TTE	$f_{øR1B}$, $f_{øR2B}$ = 8 MHz, data rate = 16 MHz	93.5	98		%
Register imbalance	RI	V_{OUT} = 500 mV	0.0		4.0	%
Red response peak				630		nm
Green response peak				540		nm
Blue response peak				460		nm
Dynamic range	DR	V_{sat}/DSNU		2600		times
Reset feed through noise	RFSN	Light shielding		300	500	mV

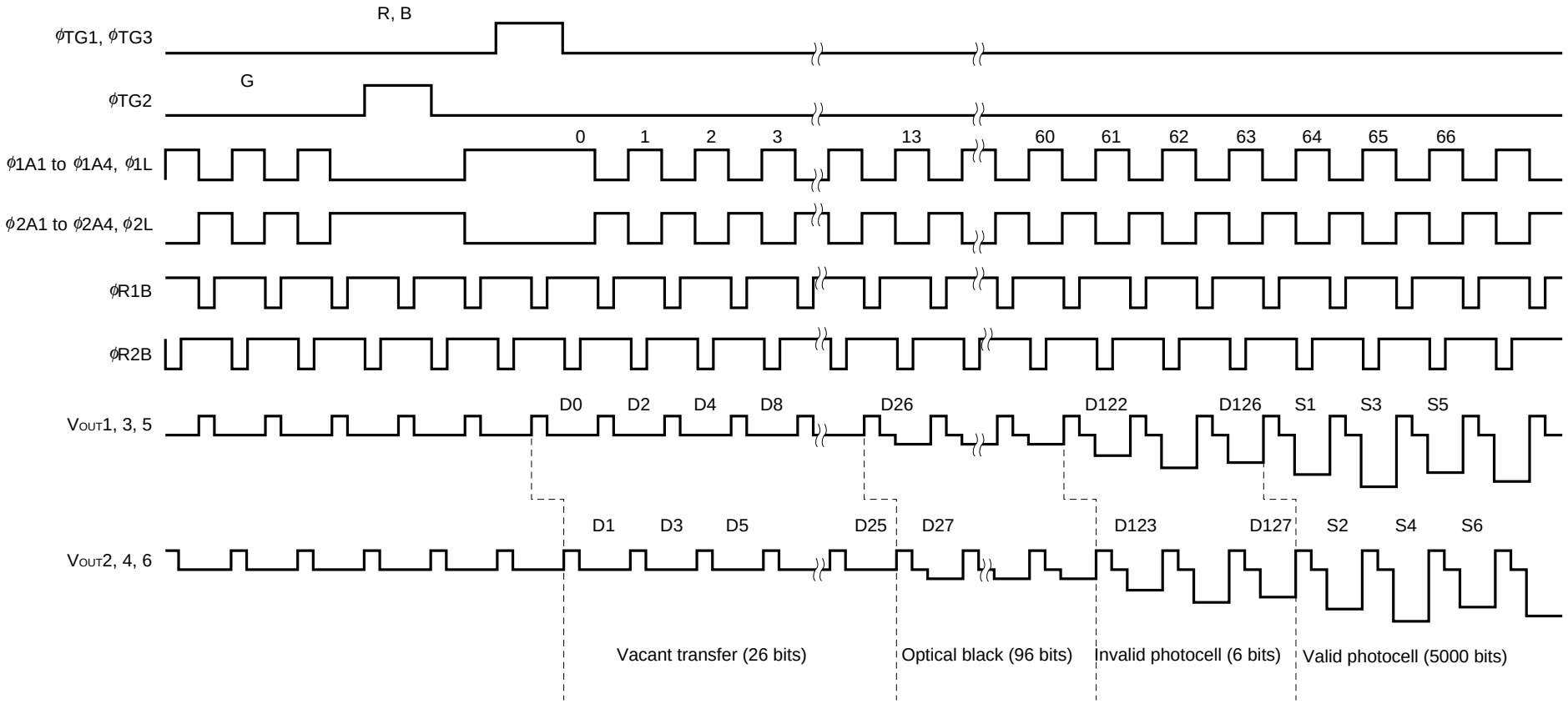
Notes 1. Refer to **TIMING CHART 3, 5**.

2. Each fall delay time of ϕ1L and ϕ2L (t_{11}, t_{27} and t_1, t_{37}) is the TYP. value (refer to **TIMING CHART 3, 5**).

INPUT PIN CAPACITANCE

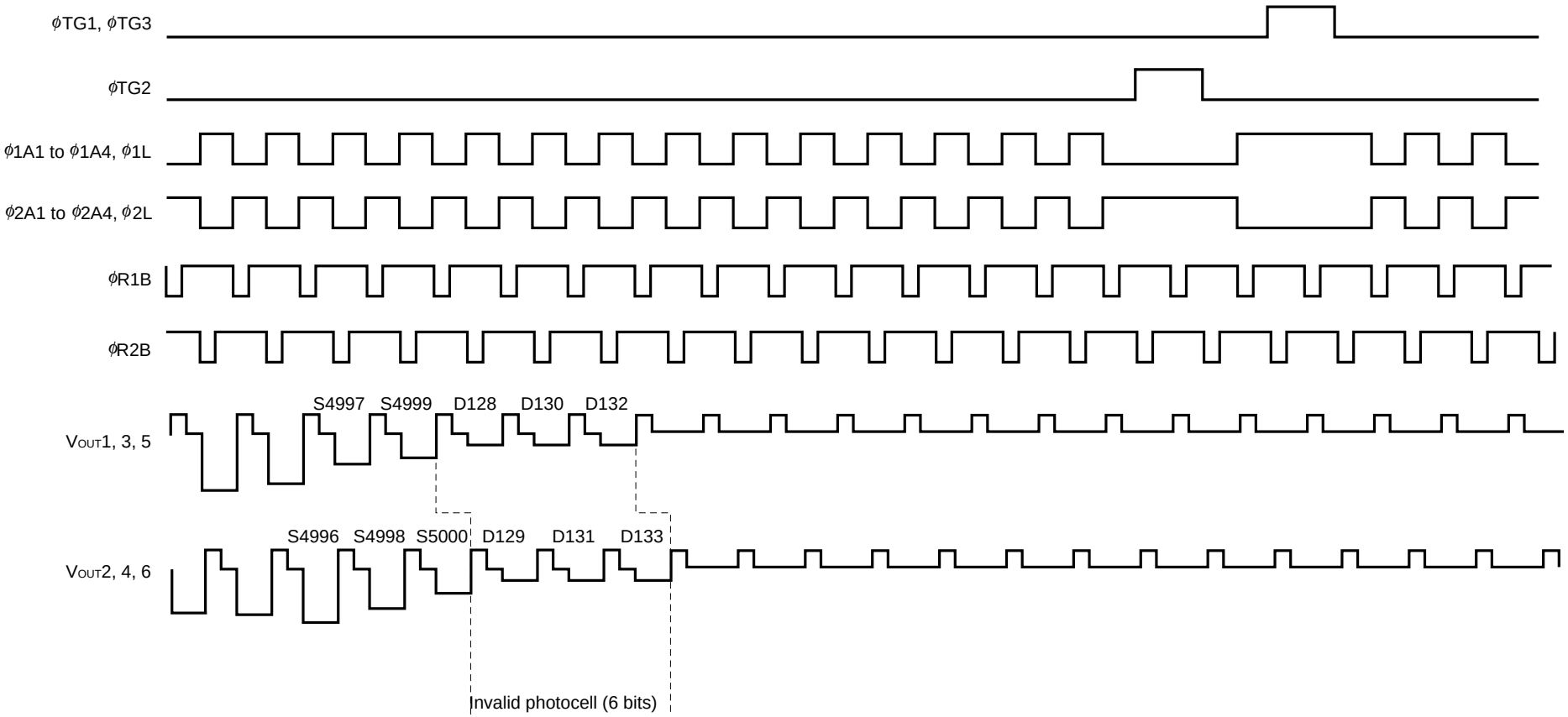
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Transfer gate pin capacitance	$C\phi_{TG}$	ϕTG1	16		300	450	pF
		ϕTG2	13				
		ϕTG3	10				
Reset clock pin capacitance	$C\phi_{R}$	ϕR1B	20		50	80	pF
		ϕR2B	5				
Last stage shift register clock pin capacitance	$C\phi_{L}$	ϕ1L	19		100	150	pF
		ϕ2L	6				
Shift register clock pin capacitance A	$C\phi_{A}$	ϕ1A1	18		250	380	pF
		ϕ1A4	8				
		ϕ2A1	17				
		ϕ2A4	9				
Shift register clock pin capacitance B	$C\phi_{B}$	ϕ1A2	15		500	750	pF
		ϕ1A3	11				
		ϕ2A2	14				
		ϕ2A3	12				

TIMING CHART 1

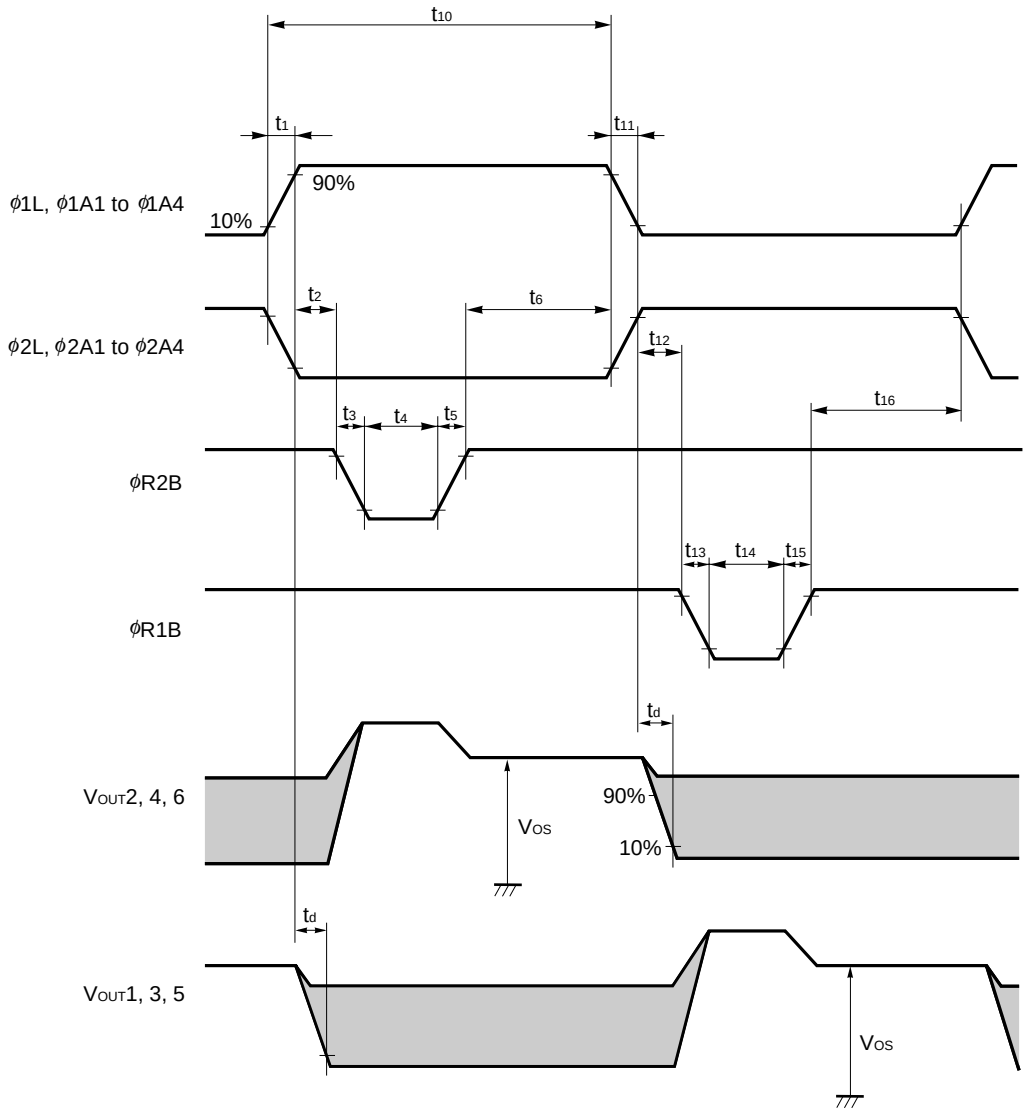


Caution Pins 18 (φ1A1) and 15 (φ1A2), 11 (φ1A3) and 8 (φ1A4) are each connected inside of the device, so do not input different timings to them. And also pins 17 (φ2A1) and 14 (φ2A2), 12 (φ2A3) and 9 (φ2A4) are each connected inside of the device, so do not input different timings to them (refer to BLOCK DIAGRAM).

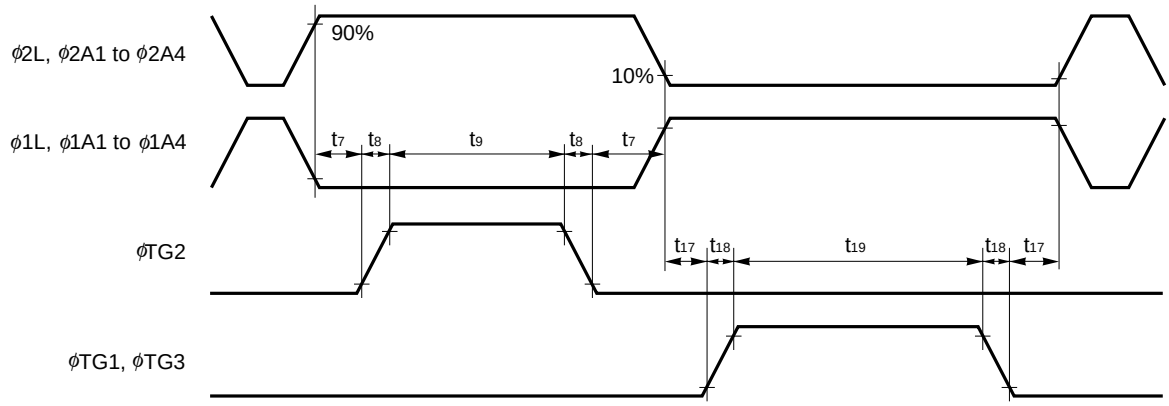
TIMING CHART 2



TIMING CHART 3 (Usual speed drive $f_{\phi R1B}$, $f_{\phi R2B}$ = 1 to 5 MHz)



TIMING CHART 4

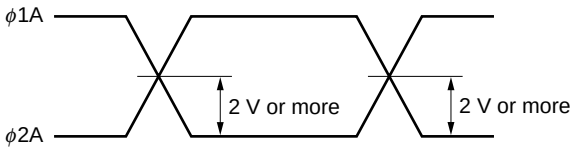


Recommended Timing

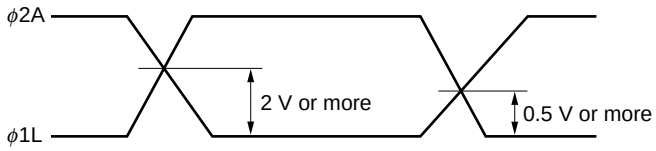
(Unit: ns)

Symbol	MIN.	TYP.	MAX.
t_1, t_{11}	0	10	–
t_2, t_{12}	0	50	–
t_3, t_5, t_{13}, t_{15}	0	5	–
t_4, t_{14}	20	50	–
t_6, t_{16}	20	50	–
t_7, t_{17}	20	50	–
t_8, t_{18}	0	50	–
t_9, t_{19}	1000	2000	–
t_{10}	100	500	–

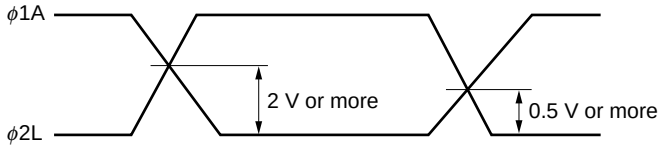
ϕ1A, ϕ2A cross points



ϕ1L, ϕ2A cross points



ϕ1A, ϕ2L cross points

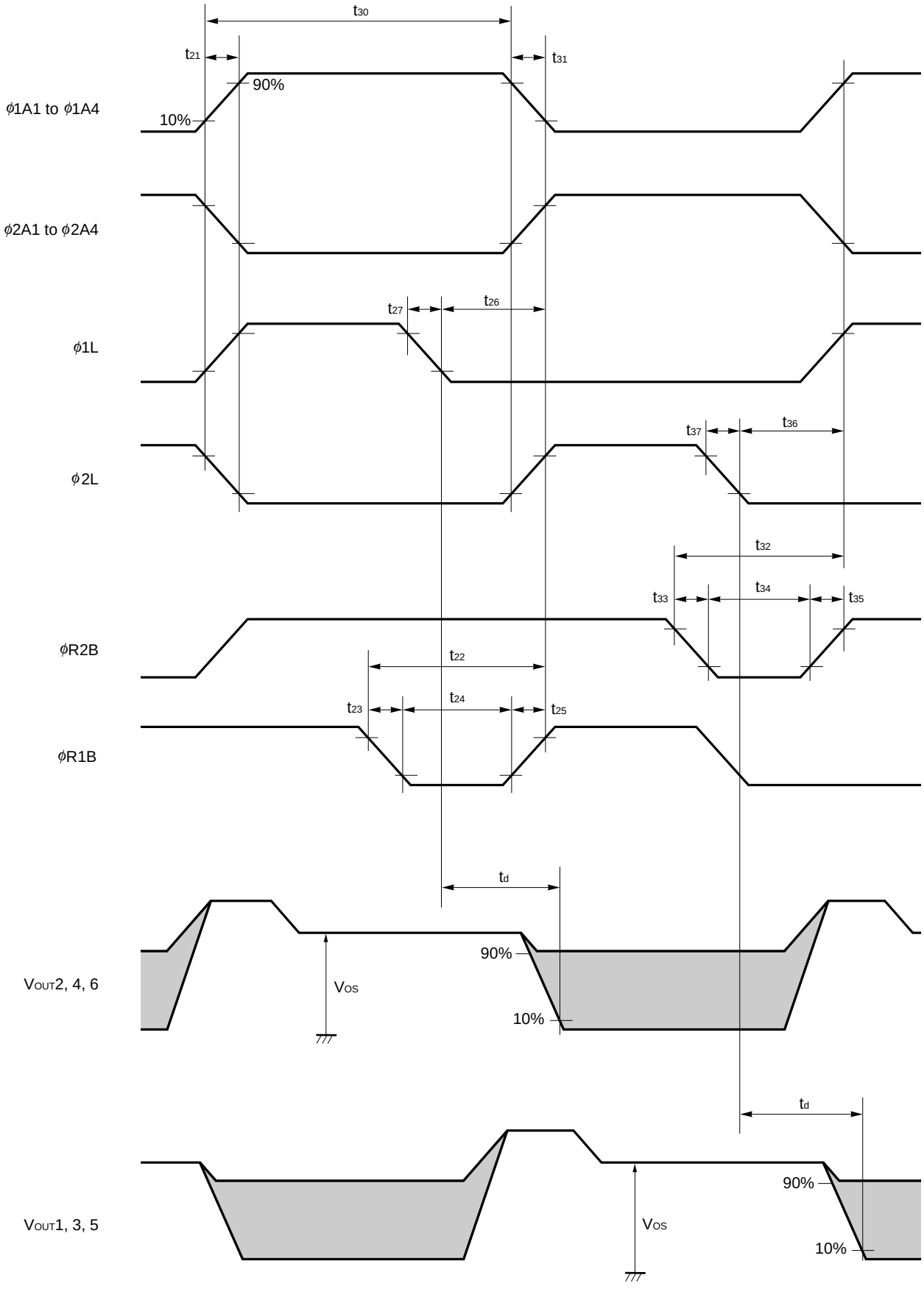


Remark 1. Adjust input resistance of each pin for cross points (ϕ1A, ϕ2A), (ϕ1L, ϕ2A) and (ϕ1A, ϕ2L)

2. ϕ1A: ϕ1A1 to ϕ1A4

ϕ2A: ϕ2A1 to ϕ2A4

TIMING CHART5 (High speed drive $f\phi_{R1B}$, $f\phi_{R2B}$ = 5 to 8 MHz)



Recommended Timing (High speed drive $f_{\phi R1B}$, $f_{\phi R2B}$ = 5 to 8 MHz)

(Unit: ns)

Symbol	MIN.	TYP.	MAX.
t_{21}, t_{31}	0	10	—
t_{22}, t_{32}	0	30	—
t_{23}, t_{25}, t_{33}, t_{35}	0	5	—
t_{24}, t_{34}	20	$t_{30}/2$	—
t_{26}, t_{36}	10	20	—
t_{27}, t_{37}	0	10	—
t_{30}	60	100	—

Caution When driving μPD3725A according to timing shown in TIMING CHART 3 at high speed, period of signal output is shorten, therefore data may not be sampled normally.

To sample data normally, drive μPD3725A according to timing shown in TIMING CHART 5. To extend the period of signal output, falling edge of last gate shift register clock φ1L, φ2L should be earlier than that of shift register clock φ1A, φ2A.

When making the falling edge of φ1L, φ2L early, output signal is effected by noise from reset clock φR1B, φR2B. To avoid the effection of this noise, the falling edge of φR1B, φR2B should be set earlier.

Driving at high speed, drive capability is necessary to be powered up. So design the peripheral circuit referring to peripheral circuit example 2.

DEFINITIONS OF CHARACTERISTIC ITEMS

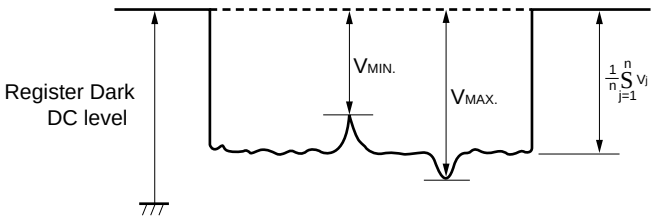
1. Saturation voltage: V_{sat}
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE
   Product of intensity of illumination (I_X) and storage time(s) when saturation of output voltage occurs.

3. Photo response non-uniformity: PRNU
   The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU(\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n} \sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

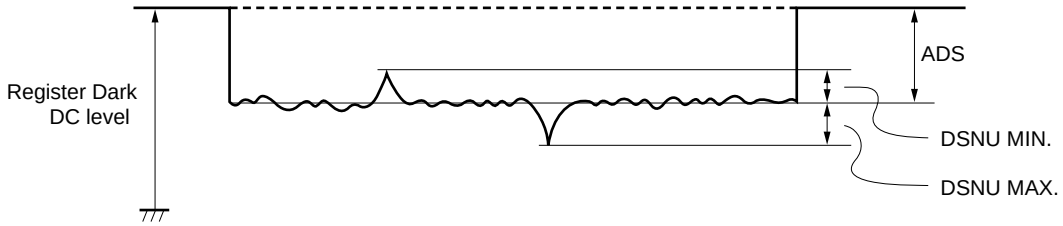
n: Number of valid bits
V_j: Output voltage of each bit



4. Average dark signal: ADS
   Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n} \sum_{j=1}^{n} V_j$$

5. Dark signal non-uniformity: DSNU
   The difference between peak or bottom output voltage in light shielding and ADS.

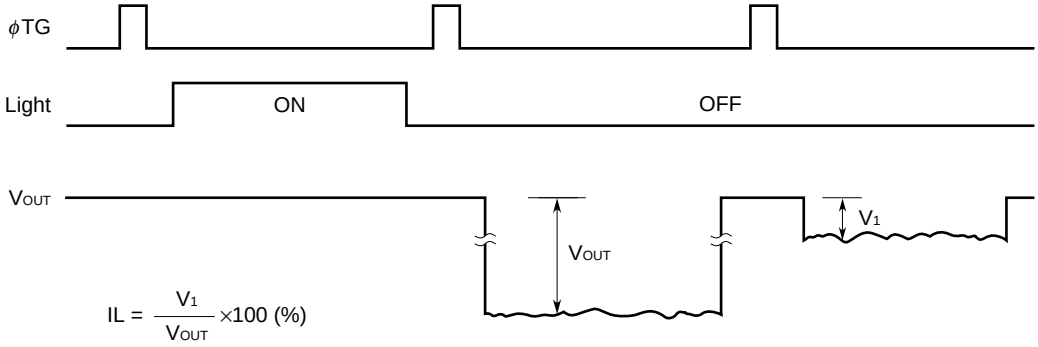


6. Output impedance: Z_O
   Output pin impedance viewed from outside.

7. Response: R
   Output voltage divided by exposure (Ix•s).
   Note that the response varies with a light source.

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.



$$IL = \frac{V_1}{V_{OUT}} \times 100\ (\%)$$

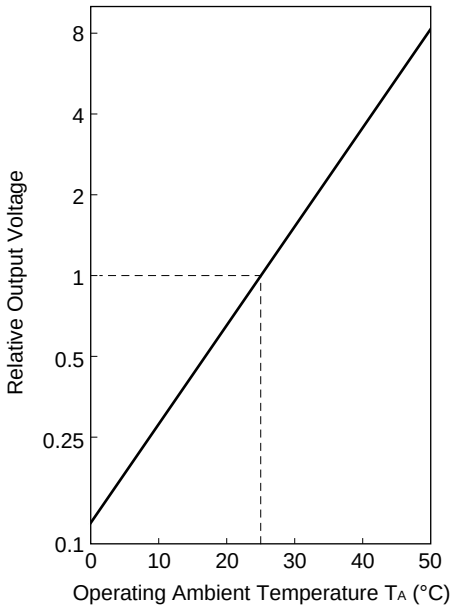
9. Register Imbalance: RI

The rate of the difference between the averages of the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

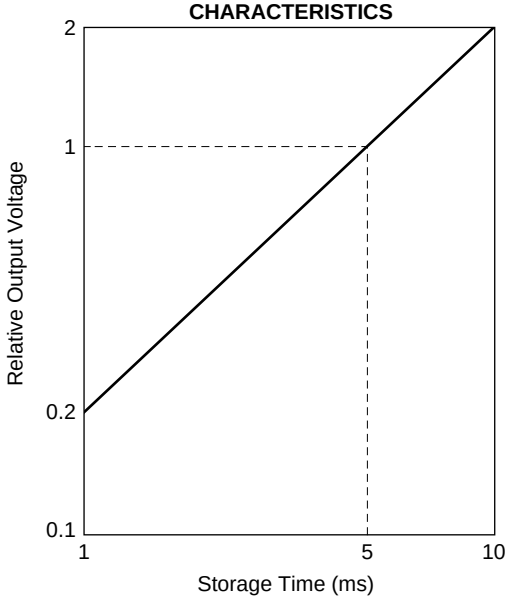
$$RI = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100\ (\%)$$

STANDARD CHARACTERISTIC CURVES (T_A = +25 °C)

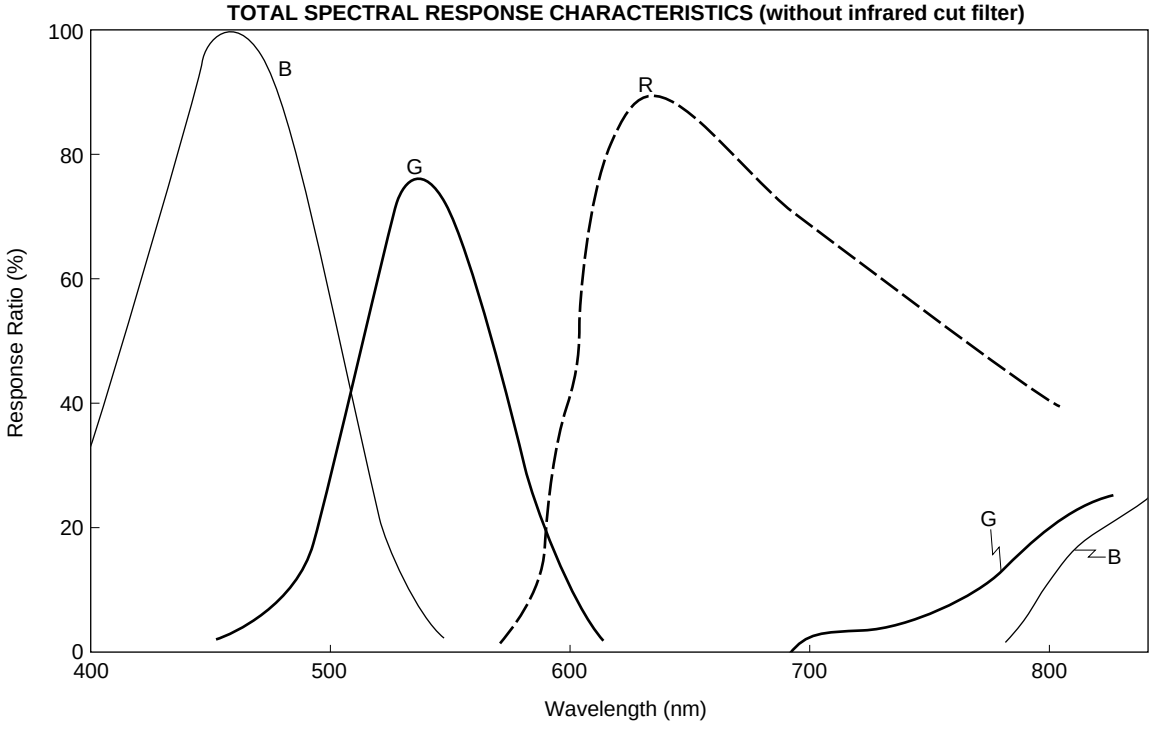
DARK OUTPUT TEMPERATURE CHARACTERISTICS



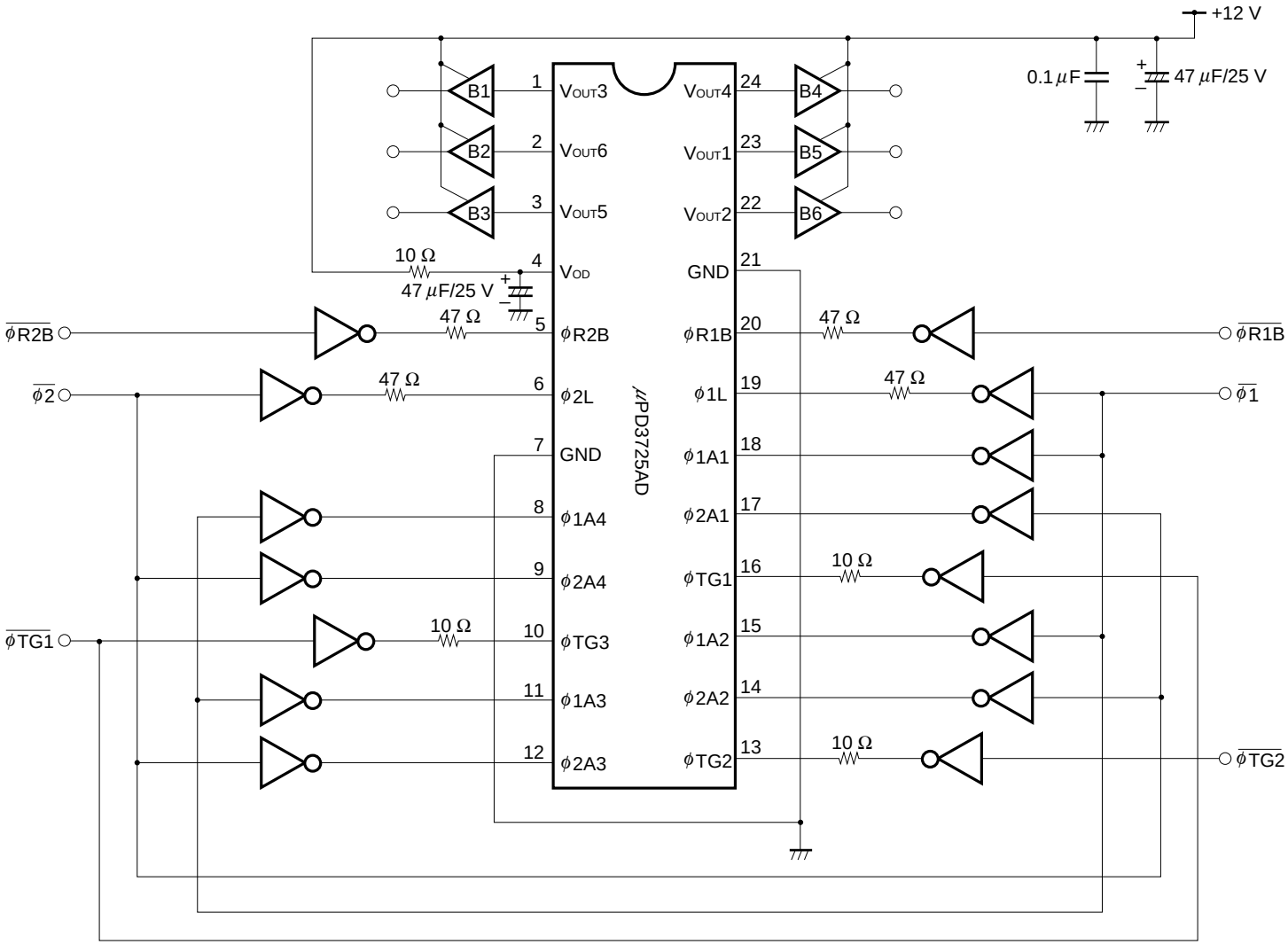
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTICS

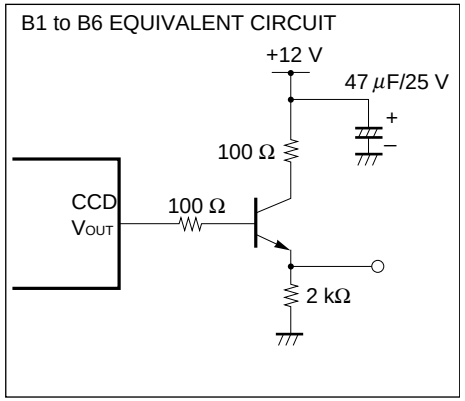


TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter)



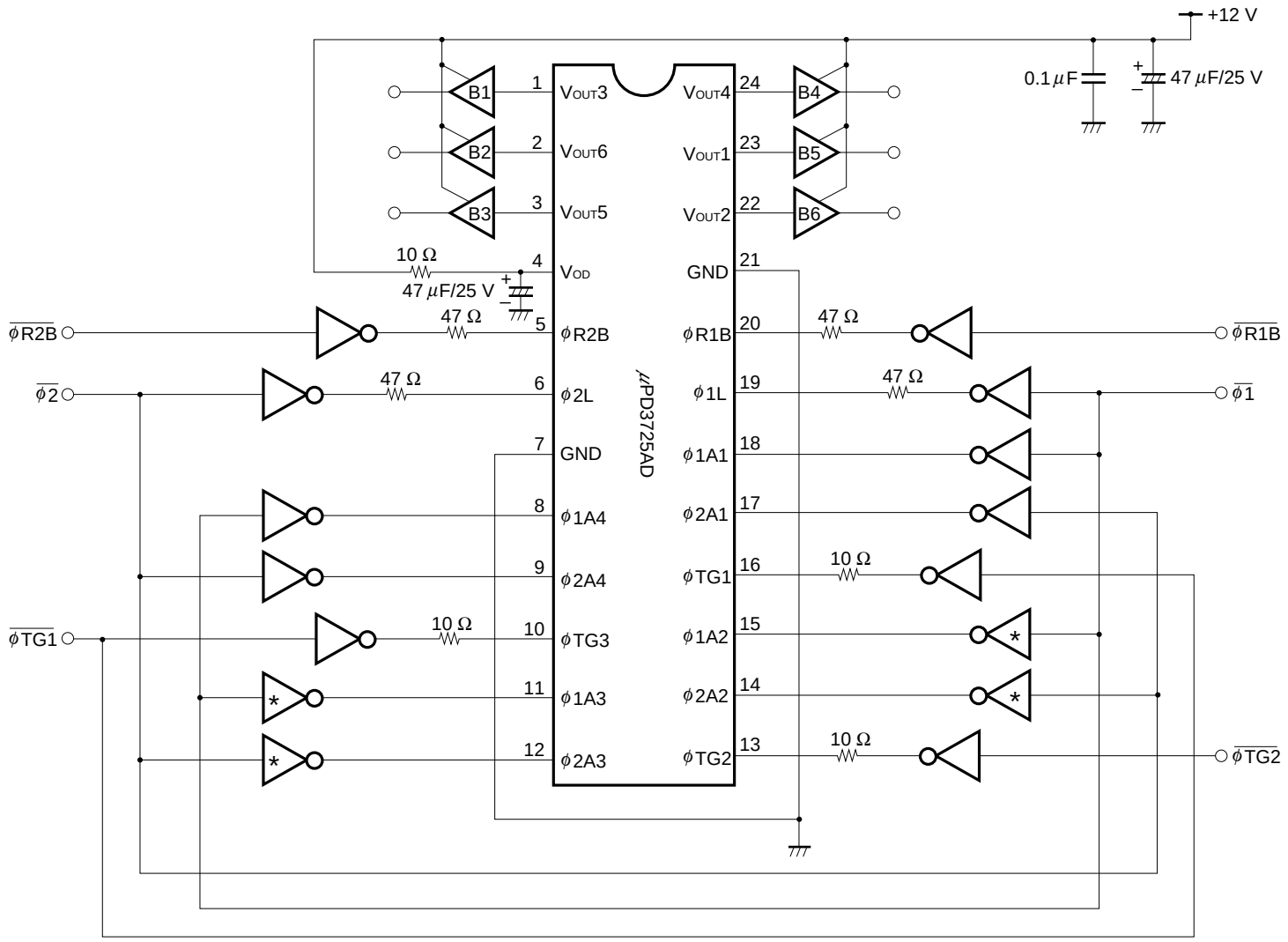
PERIPHERAL CIRCUIT EXAMPLE 1





Remark Inverters: μPD74HC04

PERIPHERAL CIRCUIT EXAMPLE 2 (For high speed drive)



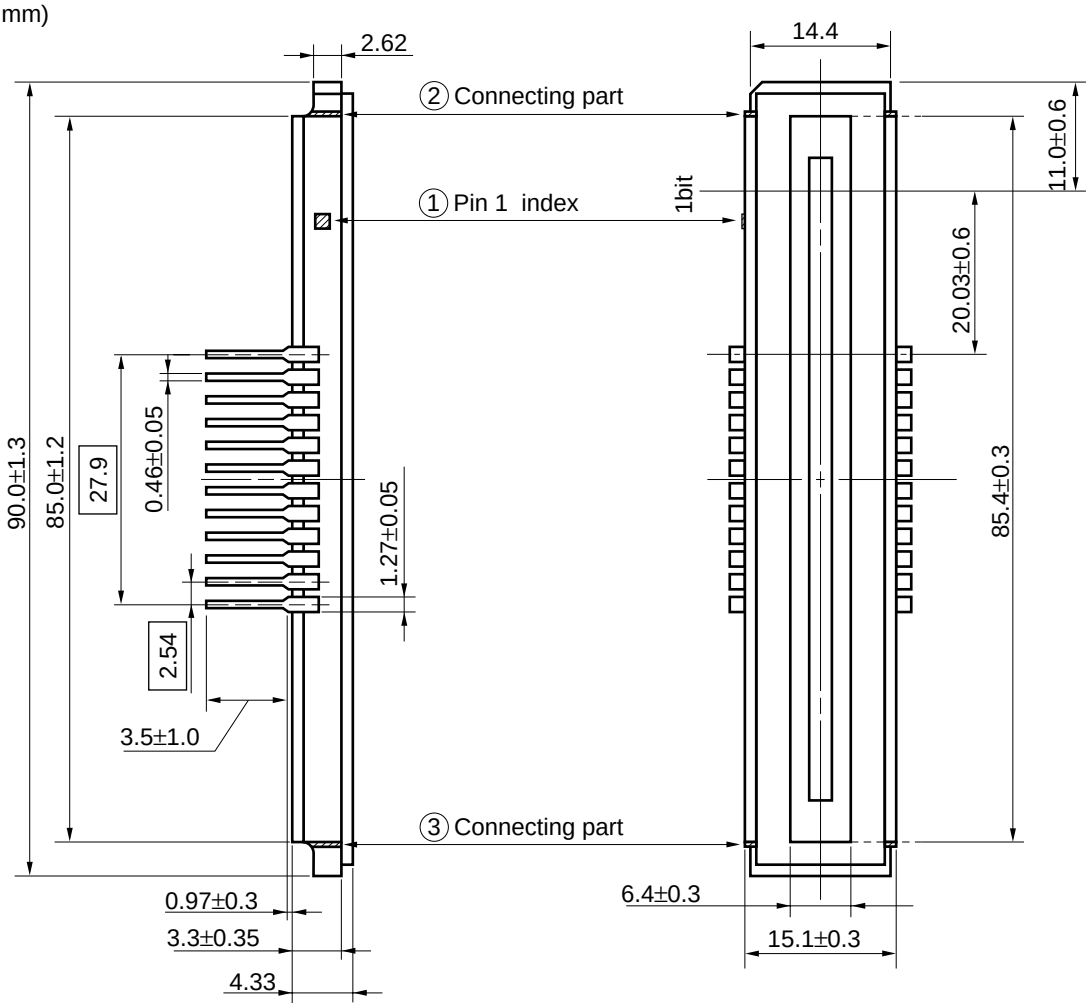
Remarks 1. Inverters: 74AC04

2. For * inverter, use high speed inverter which has double driving capability of 74AC04

PACKAGE DIMENSIONS (Unit: mm)

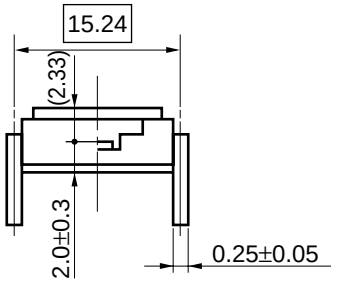
CCD LINEAR IMAGE SENSOR 24PIN CERAMIC DIP (600 mil)

(Unit : mm)



NOTE

① pin 1 index and ②, ③ connecting parts are made of silver wax and plated with gold. As they are electrically connected with GND, be sure not to touch with other wirings on the board.



Name	Dimensions	Refractive index
Glass cap	89.0 × 13.6 × 1.0	1.5

24D-1CCD-PKG-2

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Type of Through Hole Device

μPD3725AD : CCD linear image sensor 24-pin ceramic DIP (600 mil)

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial heating method	Pin temperature: 260 °C or below, Heat time: 10 seconds or less (Per each lead).

Caution For through hole devices, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

M4 94.11