NEC

MOS INTEGRATED CIRCUIT

μPD16680

1/53, 1/40 DUTY, LCD CONTROLLER/DRIVER WITH BUILT-IN RAM

DESCRIPTION

The μPD16680 is a driver which contains a RAM capable of full - dot LCD display. The single μPD16680 IC chip can operate a full - dot (up to 100 by 51 dots) LCD and pictographs (100 pictographs).

The μPD16680 can operate on single 3 V-power supply, is suitable for graphic pagers and cellular.

FEATURES

- LCD driver with a built-in display RAM
- Can operate on single 3 V-power supply
- Booster circuit incorporated : Switchable 3 or 4 folds
- Dot display RAM : 100 x 51 bits
- Pictographic display RAM : 100 bits
- Pictographic display's duty changeable : 1/53 or 1/40 duty
- Output for full-dot : 100 segments and 52 commons
- Data input based on serial & 4-bit / 8-bit parallel switch over
- String resister to output bias level incorporated
- Selectable LCD driving bias level (select from 1/8 bias, 1/7 bias, 1/6 bias)
- Oscillation circuit incorporated
- D/A converter incorporated (for LCD driving voltage adjustment)

ORDERING INFORMATION

Part number	Package
μPD16680W/P	Wafer/Chip(Matched COG mounting)

Remark Purchasing the above products in term of chips per requires an exchange of other documents as well, including a memorandum on the product quality. Therefore those who are interested in this regard are advised to contact an NEC salesperson for further details.

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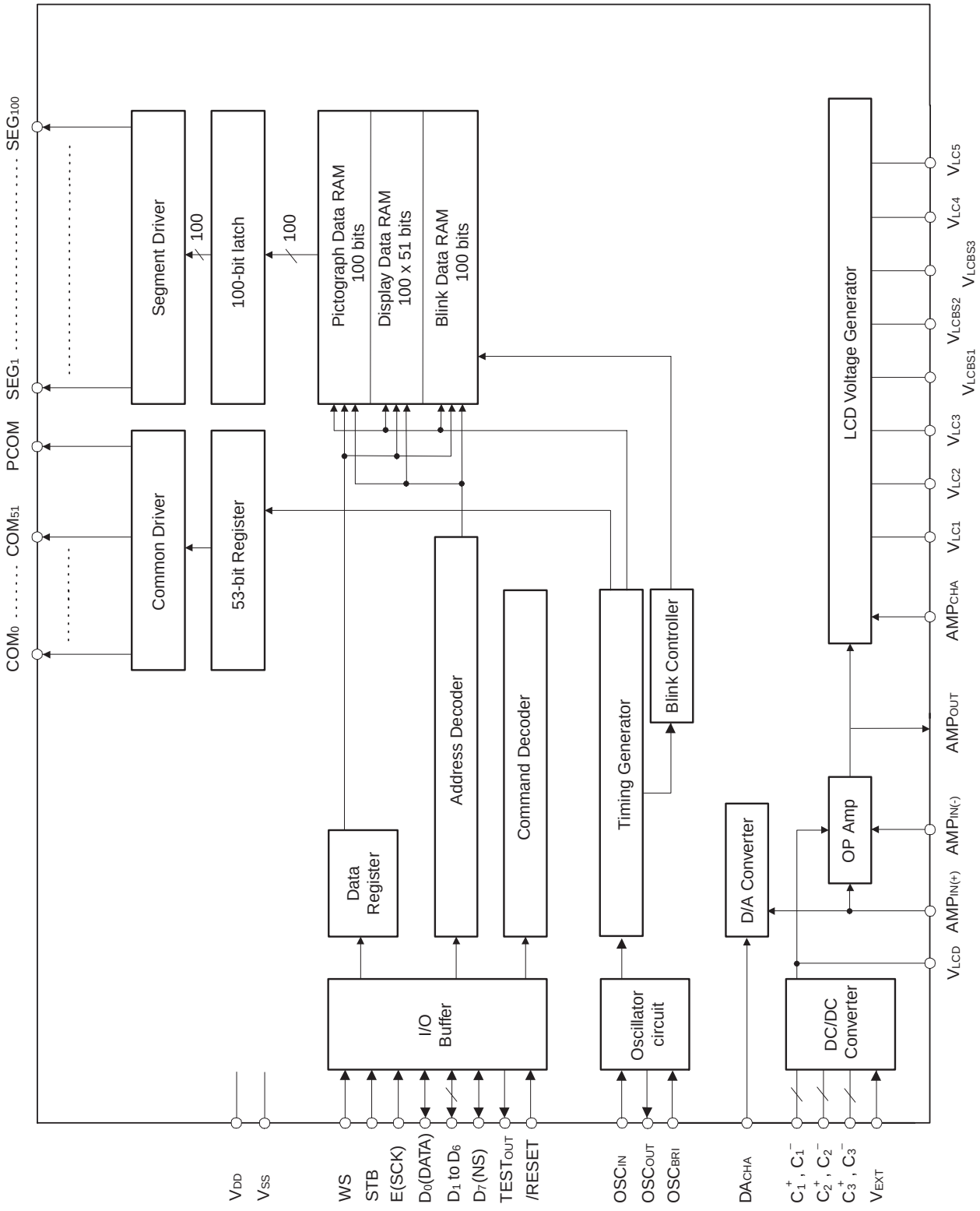
The mark ★ shows major revised points.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signals.

2. PIN CONFIGURATION (Top view)

Chip Size : 12.5 mm x 1.89 mm

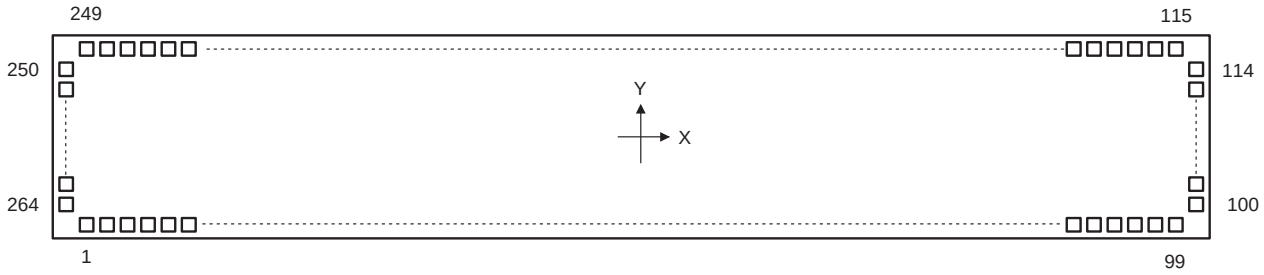


Table 2-1. Pad Layout (1/2)

Pin No.	Pin Name	X(μm)	Y(μm)
1	Dummy	–5883.2	–811.0
2	Dummy	–5763.2	–811.0
3	Dummy	–5643.2	–811.0
4	V_{LCBS1}	–5523.2	–811.0
5	V_{LCBS1}	–5403.2	–811.0
6	Dummy	–5283.2	–811.0
7	V_{LCBS2}	–5163.2	–811.0
8	V_{LCBS2}	–5043.2	–811.0
9	Dummy	–4923.2	–811.0
10	V_{LCBS3}	–4803.2	–811.0
11	V_{LCBS3}	–4683.2	–811.0
12	Dummy	–4563.2	–811.0
13	AMP_{OUT}	–4443.2	–811.0
14	AMP_{OUT}	–4323.2	–811.0
15	Dummy	–4203.2	–811.0
16	$AMP_{IN(-)}$	–4083.2	–811.0
17	$AMP_{IN(-)}$	–3963.2	–811.0
18	Dummy	–3843.2	–811.0
19	$AMP_{IN(+)}$	–3723.2	–811.0
20	$AMP_{IN(+)}$	–3603.2	–811.0
21	Dummy	–3483.2	–811.0
22	V_{DD}	–3363.2	–811.0
23	V_{DD}	–3243.2	–811.0
24	Dummy	–3123.2	–811.0
25	V_{LC5}	–3003.2	–811.0
26	V_{LC5}	–2883.2	–811.0
27	V_{LC5}	–2763.2	–811.0
28	Dummy	–2643.2	–811.0
29	V_{LC4}	–2523.2	–811.0
30	V_{LC4}	–2403.2	–811.0
31	V_{LC4}	–2283.2	–811.0
32	Dummy	–2163.2	–811.0
33	V_{LC3}	–2043.2	–811.0
34	V_{LC3}	–1923.2	–811.0
35	V_{LC3}	–1803.2	–811.0
36	Dummy	–1683.2	–811.0
37	V_{LC2}	–1563.2	–811.0
38	V_{LC2}	–1443.2	–811.0
39	V_{LC2}	–1323.2	–811.0
40	Dummy	–1203.2	–811.0
41	V_{LC1}	–1083.2	–811.0
42	V_{LC1}	–963.2	–811.0
43	V_{LC1}	–843.2	–811.0
44	Dummy	–723.2	–811.0
45	V_{LCD}	–603.2	–811.0
46	V_{LCD}	–483.2	–811.0
47	V_{LCD}	–363.2	–811.0
48	V_{DD}	–243.2	–811.0
49	V_{DD}	–123.2	–811.0
50	V_{DD}	–3.2	–811.0
51	V_{SS}	116.8	–811.0
52	V_{SS}	236.8	–811.0
53	V_{SS}	356.8	–811.0
54	Dummy	476.8	–811.0
55	C_1^+	596.8	–811.0
56	C_1^+	716.8	–811.0
57	C_1^+	836.8	–811.0
58	C_1^-	956.8	–811.0
59	C_1^-	1076.8	–811.0
60	C_1^-	1196.8	–811.0
61	C_2^+	1316.8	–811.0
62	C_2^+	1436.8	–811.0
63	C_2^+	1556.8	–811.0
64	C_2^-	1676.8	–811.0
65	C_2^-	1796.8	–811.0
66	C_2^-	1916.8	–811.0

Pin No.	Pin Name	X(μm)	Y(μm)
67	C_3^+	2036.8	–811.0
68	C_3^+	2156.8	–811.0
69	C_3^+	2276.8	–811.0
70	C_3^-	2396.8	–811.0
71	C_3^-	2516.8	–811.0
72	C_3^-	2636.8	–811.0
73	V_{DD}	2756.8	–811.0
74	V_{DD}	2876.8	–811.0
75	V_{DD}	2996.8	–811.0
76	Dummy	3116.8	–811.0
77	V_{EXT}	3236.8	–811.0
78	DA_{CHA}	3356.8	–811.0
79	AMP_{CHA}	3476.8	–811.0
80	OSC_{IN}	3596.8	–811.0
81	OSC_{OUT}	3716.8	–811.0
82	V_{DD}	3836.8	–811.0
83	OSC_{BRI}	3956.8	–811.0
84	D_0(DATA)	4076.8	–811.0
85	D_1	4196.8	–811.0
86	D_2	4316.8	–811.0
87	D_3	4436.8	–811.0
88	D_4	4556.8	–811.0
89	D_5	4676.8	–811.0
90	D_6	4796.8	–811.0
91	D_7(NS)	4916.8	–811.0
92	WS	5036.8	–811.0
93	STB	5156.8	–811.0
94	E(SCK)	5276.8	–811.0
95	/RESET	5396.8	–811.0
96	V_{DD}	5516.8	–811.0
97	$TEST_{OUT}$	5636.8	–811.0
98	Dummy	5756.8	–811.0
99	Dummy	5876.8	–811.0
100	Dummy	6112.0	–682.2
101	Dummy	6112.0	–592.2
102	COM_{27}	6112.0	–502.2
103	COM_{28}	6112.0	–412.2
104	COM_{29}	6112.0	–322.2
105	COM_{30}	6112.0	–232.2
106	COM_{31}	6112.0	–142.2
107	COM_{32}	6112.0	–52.2
108	COM_{33}	6112.0	37.8
109	COM_{34}	6112.0	127.8
110	COM_{35}	6112.0	217.8
111	COM_{36}	6112.0	307.8
112	COM_{37}	6112.0	397.8
113	Dummy	6112.0	487.8
114	Dummy	6112.0	577.8
115	Dummy	6030.0	817.8
116	Dummy	5940.0	817.8
117	COM_{38}	5850.0	817.8
118	COM_{39}	5760.0	817.8
119	COM_{40}	5670.0	817.8
120	COM_{41}	5580.0	817.8
121	COM_{42}	5490.0	817.8
122	COM_{43}	5400.0	817.8
123	COM_{44}	5310.0	817.8
124	COM_{45}	5220.0	817.8
125	COM_{46}	5130.0	817.8
126	COM_{47}	5040.0	817.8
127	COM_{48}	4950.0	817.8
128	COM_{49}	4860.0	817.8
129	COM_{50}	4770.0	817.8
130	COM_{51}	4680.0	817.8
131	PCOM	4590.0	817.8
132	SEG_{100}	4500.0	817.8

Table 2-1. Pad Layout (2/2)

Pin No.	Pin Name	X(μm)	Y(μm)
133	SEG_{99}	4410.0	817.8
134	SEG_{98}	4320.0	817.8
135	SEG_{97}	4230.0	817.8
136	SEG_{96}	4140.0	817.8
137	SEG_{95}	4050.0	817.8
138	SEG_{94}	3960.0	817.8
139	SEG_{93}	3870.0	817.8
140	SEG_{92}	3780.0	817.8
141	SEG_{91}	3690.0	817.8
142	SEG_{90}	3600.0	817.8
143	SEG_{89}	3510.0	817.8
144	SEG_{88}	3420.0	817.8
145	SEG_{87}	3330.0	817.8
146	SEG_{86}	3240.0	817.8
147	SEG_{85}	3150.0	817.8
148	SEG_{84}	3060.0	817.8
149	SEG_{83}	2970.0	817.8
150	SEG_{82}	2880.0	817.8
151	SEG_{81}	2790.0	817.8
152	SEG_{80}	2700.0	817.8
153	SEG_{79}	2610.0	817.8
154	SEG_{78}	2520.0	817.8
155	SEG_{77}	2430.0	817.8
156	SEG_{76}	2340.0	817.8
157	SEG_{75}	2250.0	817.8
158	SEG_{74}	2160.0	817.8
159	SEG_{73}	2070.0	817.8
160	SEG_{72}	1980.0	817.8
161	SEG_{71}	1890.0	817.8
162	SEG_{70}	1800.0	817.8
163	SEG_{69}	1710.0	817.8
164	SEG_{68}	1620.0	817.8
165	SEG_{67}	1530.0	817.8
166	SEG_{66}	1440.0	817.8
167	SEG_{65}	1350.0	817.8
168	SEG_{64}	1260.0	817.8
169	SEG_{63}	1170.0	817.8
170	SEG_{62}	1080.0	817.8
171	SEG_{61}	990.0	817.8
172	SEG_{60}	900.0	817.8
173	SEG_{59}	810.0	817.8
174	SEG_{58}	720.0	817.8
175	SEG_{57}	630.0	817.8
176	SEG_{56}	540.0	817.8
177	SEG_{55}	450.0	817.8
178	SEG_{54}	360.0	817.8
179	SEG_{53}	270.0	817.8
180	SEG_{52}	180.0	817.8
181	SEG_{51}	90.0	817.8
182	SEG_{50}	0.0	817.8
183	SEG_{49}	–90.0	817.8
184	SEG_{48}	–180.0	817.8
185	SEG_{47}	–270.0	817.8
186	SEG_{46}	–360.0	817.8
187	SEG_{45}	–450.0	817.8
188	SEG_{44}	–540.0	817.8
189	SEG_{43}	–630.0	817.8
190	SEG_{42}	–720.0	817.8
191	SEG_{41}	–810.0	817.8
192	SEG_{40}	–900.0	817.8
193	SEG_{39}	–990.0	817.8
194	SEG_{38}	–1080.0	817.8
195	SEG_{37}	–1170.0	817.8
196	SEG_{36}	–1260.0	817.8
197	SEG_{35}	–1350.0	817.8
198	SEG_{34}	–1440.0	817.8

Pin No.	Pin Name	X(μm)	Y(μm)
199	SEG_{33}	–1530.0	817.8
200	SEG_{32}	–1620.0	817.8
201	SEG_{31}	–1710.0	817.8
202	SEG_{30}	–1800.0	817.8
203	SEG_{29}	–1890.0	817.8
204	SEG_{28}	–1980.0	817.8
205	SEG_{27}	–2070.0	817.8
206	SEG_{26}	–2160.0	817.8
207	SEG_{25}	–2250.0	817.8
208	SEG_{24}	–2340.0	817.8
209	SEG_{23}	–2430.0	817.8
210	SEG_{22}	–2520.0	817.8
211	SEG_{21}	–2610.0	817.8
212	SEG_{20}	–2700.0	817.8
213	SEG_{19}	–2790.0	817.8
214	SEG_{18}	–2880.0	817.8
215	SEG_{17}	–2970.0	817.8
216	SEG_{16}	–3060.0	817.8
217	SEG_{15}	–3150.0	817.8
218	SEG_{14}	–3240.0	817.8
219	SEG_{13}	–3330.0	817.8
220	SEG_{12}	–3420.0	817.8
221	SEG_{11}	–3510.0	817.8
222	SEG_{10}	–3600.0	817.8
223	SEG_{9}	–3690.0	817.8
224	SEG_{8}	–3780.0	817.8
225	SEG_{7}	–3870.0	817.8
226	SEG_{6}	–3960.0	817.8
227	SEG_{5}	–4050.0	817.8
228	SEG_{4}	–4140.0	817.8
229	SEG_{3}	–4230.0	817.8
230	SEG_{2}	–4320.0	817.8
231	SEG_{1}	–4410.0	817.8
232	COM_{26}	–4500.0	817.8
233	COM_{25}	–4590.0	817.8
234	COM_{24}	–4680.0	817.8
235	COM_{23}	–4770.0	817.8
236	COM_{22}	–4860.0	817.8
237	COM_{21}	–4950.0	817.8
238	COM_{20}	–5040.0	817.8
239	COM_{19}	–5130.0	817.8
240	COM_{18}	–5220.0	817.8
241	COM_{17}	–5310.0	817.8
242	COM_{16}	–5400.0	817.8
243	COM_{15}	–5490.0	817.8
244	COM_{14}	–5580.0	817.8
245	COM_{13}	–5670.0	817.8
246	COM_{12}	–5760.0	817.8
247	COM_{11}	–5850.0	817.8
248	Dummy	–5940.0	817.8
249	Dummy	–6030.0	817.8
250	Dummy	–6112.0	577.8
251	Dummy	–6112.0	487.8
252	COM_{10}	–6112.0	397.8
253	COM_{9}	–6112.0	307.8
254	COM_{8}	–6112.0	217.8
255	COM_{7}	–6112.0	127.8
256	COM_{6}	–6112.0	37.8
257	COM_{5}	–6112.0	-52.2
258	COM_{4}	–6112.0	-142.2
259	COM_{3}	–6112.0	-232.2
260	COM_{2}	–6112.0	-322.2
261	COM_{1}	–6112.0	-412.2
262	PCOM	–6112.0	-502.2
263	Dummy	–6112.0	-592.2
264	Dummy	–6112.0	-682.2

3. PIN DESCRIPTIONS

3.1 Power System Pins

Pin Symbol	Pin Name	Pin No.	I/O	Function Description
V_{DD}	Logic and booster power supply pin	22, 23, 48 to 50, 73 to 75, 82, 96	-	Power supply pin for logic and booster circuit.
V_{SS}	Logic and driver ground pin	51 to 53	-	Ground pin for logic and driver circuit.
V_{LCD}	Driver power supply pin	45 to 47	-	Driver power supply pin. Output pin of internal booster circuit. Please connect with a 1 μF booster capacitor to ground. When not using the internal booster circuit, the driver power can be turned on directly.
★ V_{LC1} to V_{LC5}	Driver reference power supply	25 to 27, 29 to 31, 33 to 35, 37 to 39, 41 to 43	-	Reference power supply pin for LCD drive. When the internal bias is selected, be sure to leave it open. When display contrast is bad, connect a capacitor between these pins and ground.
V_{LCBS1} to V_{LCBS3}	Bias level select pin	4, 5, 7, 8, 10, 11	-	When the internal bias is selected, Connecting these pins outside the IC, the bias level can be changed.
C_1^+, C_1^- C_2^+, C_2^- C_3^+, C_3^-	Capacitor connection pins	55 to 72	-	Capacitor connection pins for booster circuit. When using internal booster circuit, connect a 1μF capacitor between these pins.

3.2 Logic System Pins (1/2)

Pin Symbol	Pin Name	Pin No.	I/O	Function Description
WS	Word length select pin (Word Select)	92	I	This pin selects the word length. At High level, it become an 8-bit parallel interface. At Low level, when D_7(NS) is High level, it become a serial interface. When the word length is 4 bits, data is transferred in the upper-to-low sequence by mean of data busses D_0 to D_3. The word length cannot be changed after power-on.
DA_{CHA}	D/A converter select pin	78	I	This pin selects whether to use the internal D/A converter for LCD driving voltage adjustment or not. At High level, D/A converter is used. At Low level, unused.
STB	Strobe	93	I	This pin is select signal of device, strobe signal for data transfer. Data transfer is initialized at falling/rising edge of STB. Data can be input/output at Low level either in parallel interface or serial interface mode. When STB is High level, Enable/shift clock is bypassed.
E(SCK)	Enable(shift clock)	94	I	When using parallel interface mode, this pin becomes the data enable input. In reading-in, data is fetched into the interface buffer at rising edge. In reading-out, data is fetched from interface buffer at falling edge. When using serial interface mode, this pin becomes the data shit clock. In reading-in, data is fetched into the interface buffer at rising edge. In reading-out, data is fetched from interface buffer at falling edge.
D_0(DATA)	Data-bus(data)	84	I/O	When using parallel interface mode, this pin becomes the D_0 bit of data-bus. When using serial interface mode, this pin becomes the input/output pin of the command and display data (3 states).
D_1 to D_3	Data-bus	85 to 87	I/O	When using parallel interface mode, these pin becomes the D_1 to D_3 bits of data-bus. When using serial interface mode, keep them H or L.
D_4 to D_6	Data-bus	88 to 90	I/O	When using parallel interface mode, these pin become the D_4 to D_6 bits of data-bus. When using serial interface mode, keep them H or L.
D_7(NS)	Data-bus(nibble select)	91	I/O	When word select (WS) is High level, this pin becomes the D_7 bit of data-bus. When word select (WS) is Low level, This pin becomes nibble select pin. At High level, selected 4-bit parallel interface. At Low level, selected serial interface.
$TEST_{OUT}$	TEST signal output	97	O	When to do test, this pin is output for test signal. When using in normal operation, this pin leave open.
/RESET	Reset	95	I	At Low level, the μPD16680 is initialized.

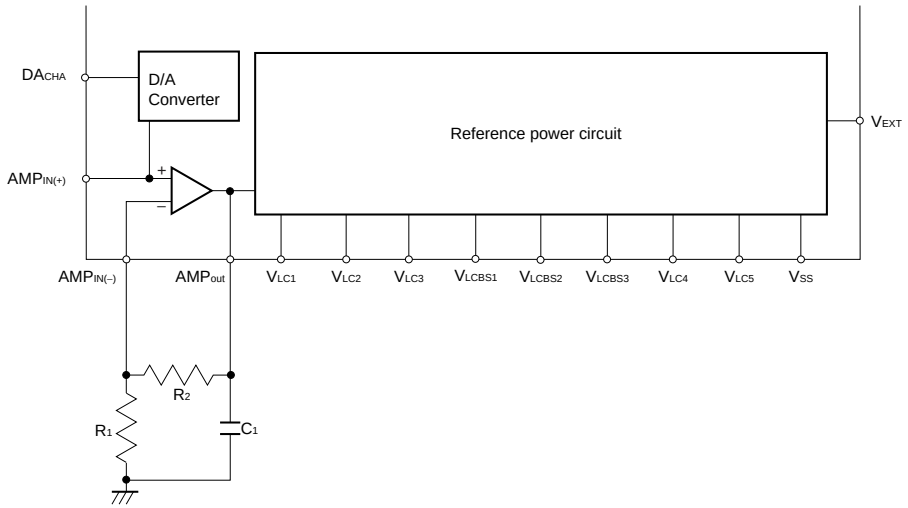
3.2 Logic System Pins (2/2)

Pin Symbol	Pin Name	Pin No.	I/O	Function Description
AMP_{CHA}	Amp mode select pin	79	I	Select operational amplifier mode. At High level, “Level capacitor mode”. At Low level, “LCD driving mode”.
V_{EXT}	LCD reference supply switching	77	I	Select the method for supplying LCD power circuit. At High level, LCD driving voltage is supplied external circuit. At Low level, it is supplied internal circuit.
OSC_{IN}	Oscillation pin	80	I	These pins are connected with the 1 MΩ resistor. When using external oscillation, input into the OSC_{IN} , and leaving the OSC_{OUT} open.
OSC_{OUT}		81	O	
OSC_{BRI}	Blinking Clock	83	I	This pin is oscillation input for Blinking. To input 2 Hz external clock, when to use Blinking by external clock mode. When not to use this pin, keep it H or L.

3.3 Driver System Pins

Pin Symbol	Pin Name	Pin No.	I/O	Function Description
SEG_1 to SEG_{100}	Segment	132 to 231	O	Segment output pins.
COM_1 to COM_{51}	Common	102 to 112, 117 to 130, 232 to 247, 252 to 261	O	Common output pins
PCOM	Pictographic common	131, 262	O	Common output pins for pictograph. (Same waveform output from these pins.)
AMP_{IN}(+)	Operational amplifier input	19, 20	I	These pins are the input pins of operational amplifier for LCD driving voltage adjustment. When using the internal D/A converter, leave $AMP_{IN(+)}$ open. When not using the internal D/A converter, it is necessary to input the reference voltage. $AMP_{IN(-)}$ is connected to the resister for LCD driving voltage adjustment. See **4. LCD DRIVING VOLTAGE CONTROL CIRCUIT**.
AMP_{IN}(-)		16,17		
AMP_{OUT}	Operational amplifier output	13,14	O	This is the input pin of operational amplifier for LCD driving voltage adjustment. Normally it is connected to the resister for LCD driving voltage adjustment. See **4. LCD DRIVING VOLTAGE CONTROL CIRCUIT**. It recommends to connect to this pin a 0.1 to 1 μF capacitor to make the output of the internal operational amplifier be stable.
Dummy	Dummy pad	1, 2, 3, 9, 12, 15, 18, 21, 24, 28, 32, 33, 40, 44, 54, 76, 98 to 101, 113 to 116, 248 to 251, 263, 264	-	Dummy pins are not connected to the internal circuit. Leave open if they are not used.

4. LCD DRIVING VOLTAGE CONTROL CIRCUIT



5. POWER CIRCUIT

The μPD16680 incorporate the booster circuit is switchable between 3 and 4 folds. The boosting magnitude of internal booster circuit is selected by the capacitor connection.

The reference power circuit is switchable between internal driving circuit and external driving circuit. The method for supplying the reference circuit selected by V_{EXT} pin (H : External, L : Internal).

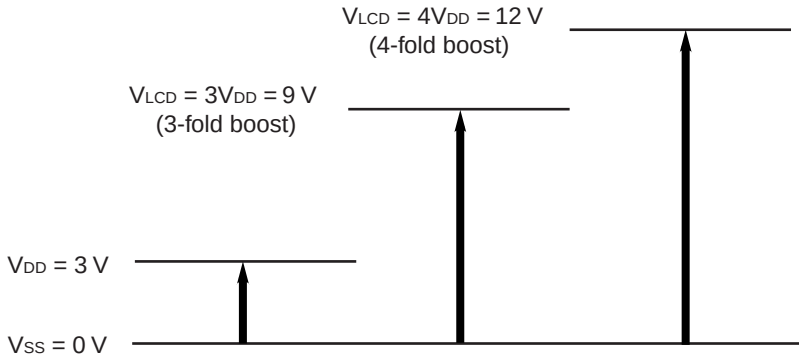
5.1 Booster circuit

Using Internal driving circuit, to connect condenser for boosting between C_1^+ and C_1^-, C_2^+ and C_2^-, C_3^+ and C_3^- , to connect condenser between V_{LCD} and V_{DD} to be stable boosting voltage. And to set V_{EXT} pin to low level, internal booster circuit boost voltage between V_{DD} and V_{SS} to 3 or 4 folds.

The booster circuit is using clock made by internal oscillation circuit. It is necessary that oscillation to be operated.

C_1^+, C_1^- ,C_2^+ ,C_2^- ,C_3^+ ,C_3^-, V_{DD} are pins for booster circuit. To use the wire that have low register value to connect these pins.

Figure 5-1 3x and 4x Booster Circuits



Remarks 1. When to use 3-fold booster circuit, not to connect condenser between C_3^+ and C_2^-, C_1^+ and C_1^-, leave open C_2^+ and C_3^-.

2. When to use external power supply circuit, booster circuit is not operating.

5.2 LCD driving circuit

5.2.1 To use internal driving circuit, not to use D/A converter (V_{EXT} = L , DA_{CHA} = L)

When to internal driving circuit is chosen, boosted voltage be used for power of internal operational amplifier adjusting LCD driving voltage. To connect external resister R_1, R_2, and input reference voltage to $AMP_{IN(+)}$ pin. It is possible to adjust LCD driving voltage of V_{LC1} . If using thermistor to adjust LCD driving voltage according to the temperature characteristic of LCD panel, we recommend connecting it with R_2 in parallel.

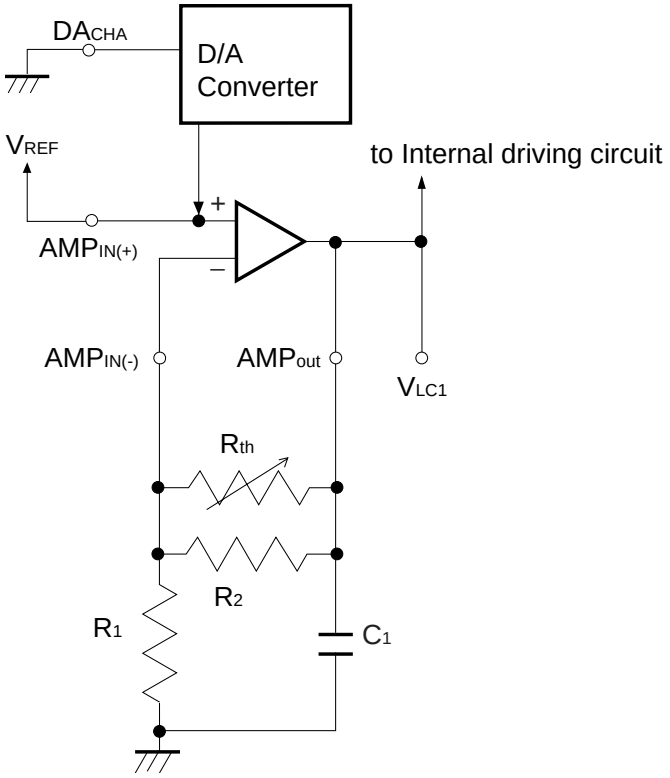
The value of V_{LC1} can be computed by the following formula.

Equation 5-1

$$V_{LC1} = AMP_{IN}(+) = \left(1 + \frac{R_2'}{R_1}\right) V_{REF}$$

Remark $R_2' = \dfrac{R_2 \times R_{th}}{R_2 + R_{th}}$

Figure 5-2 When not using Internal power supply select or D/A converter

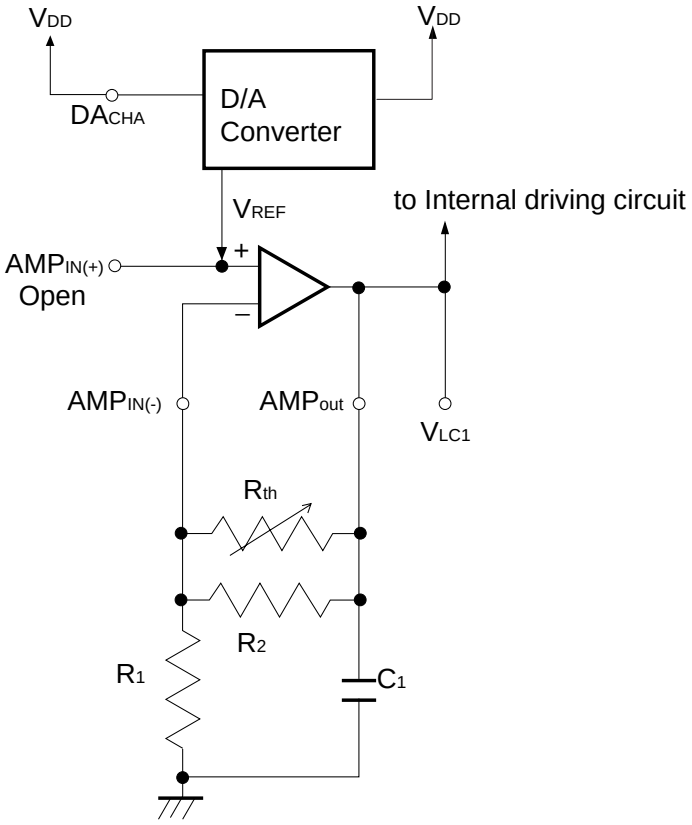


5.2.2 To use internal driving circuit and D/A converter (V_{EXT} = L , DA_{CHA} = H)

To use D/A converter, it is possible to adjust reference voltage V_{REF} inputted to $AMP_{IN(+)}$ pin for LCD driving by command.

To set 6-bit data to D/A converter register, reference voltage V_{REF} is choose one level from 64 level in 1/2 V_{DD} to V_{DD}. The formula of V_{LC1} is as same written in **Equation 5-1**.

Figure 5-3 Using internal power supply select and D/A converter



.

5.2.3 To use external driving circuit (V_{EXT} = H)

When external voltage supply circuit for LCD driving is chosen, operational amplifier incorporated IC is off. Therefore, it is impossible to use operational amplifier for LCD driving and D/A converter function. LCD driving voltage is adjust by the voltage inputted to V_{LCD} and V_{LC1} pins directly.

Remarks 1. Set $V_{LCD} \geq V_{LC1}$.

2. DA_{CHA}, $AMP_{IN(+)}$, $AMP_{IN(-)}$ are CMOS input. Set H level or L level.

3. Set AMP_{OUT} pin "open".

5.3 REFERENCE VOLTAGE CIRCUIT

5.3.1 To use internal reference voltage circuit (V_{EXT} = L)

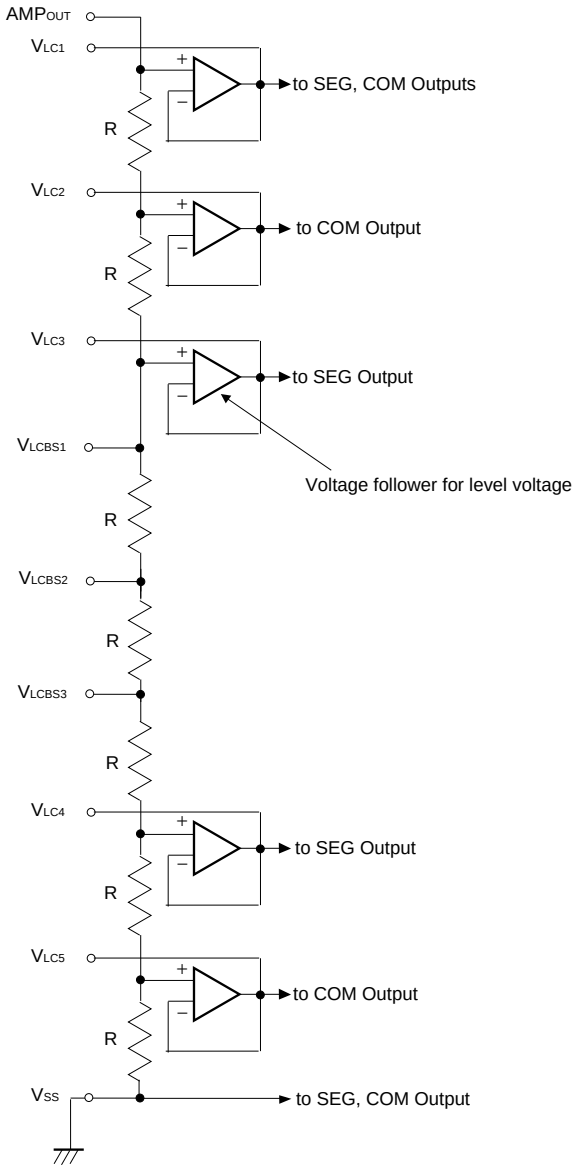
When internal driving circuit is chosen, 6 levels for LCD reference voltage (V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}, V_{LC5}, V_{SS}) is generate by internal breeder resister.

5.3.2 To use external driving circuit (V_{EXT} = H)

When external driving circuit is chosen, operational amplifier incorporated IC is Off. It is necessary to input voltage to V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4} and V_{LC5} directly.

Generally, These levels are made by external breeder resister. The display dignity of LCD declines when these resistance values are big, it is necessary to choose the resistance value which corresponds with the LCD panel.
There is an effect that improves display dignity when connecting a capacitor with each level pins and the ground. It is necessary to choose the condenser value which corresponds with the LCD panel.

★ **Figure 5-3. Reference voltage circuit**



5.4 Setting BIAS value

When internal driving circuit chosen, by connecting the interval of the pin V_{LCBS1}, V_{LCBS2}, V_{LCBS3} outside the IC, the bias value can be set from the 1/6 bias, the 1/7 bias, the 1/8 bias.

Bias value	Pin connection
1/8 bias	V_{LCBS1}, V_{LCBS2}, V_{LCBS3} All open
1/7 bias	To connect V_{LCBS1} and V_{LCBS2}, or V_{LCBS2} and V_{LCBS3}
1/6 bias	To connect V_{LCBS1} and V_{LCBS3}, V_{LCBS2} is open.

5.5 Voltage followers for level power supply

By the input of AMP_{CHA} pin, it controls voltage follower for the LCD drive level power supply.

- LCD driving mode (AMP_{CHA} = L)

  When this mode is chosen, The voltage follower maximizes electric current supply ability for LCD drive. It doesn't need to connect the external capacitor for the level stability.

- Level capacitor mode (AMP_{CHA} = H)

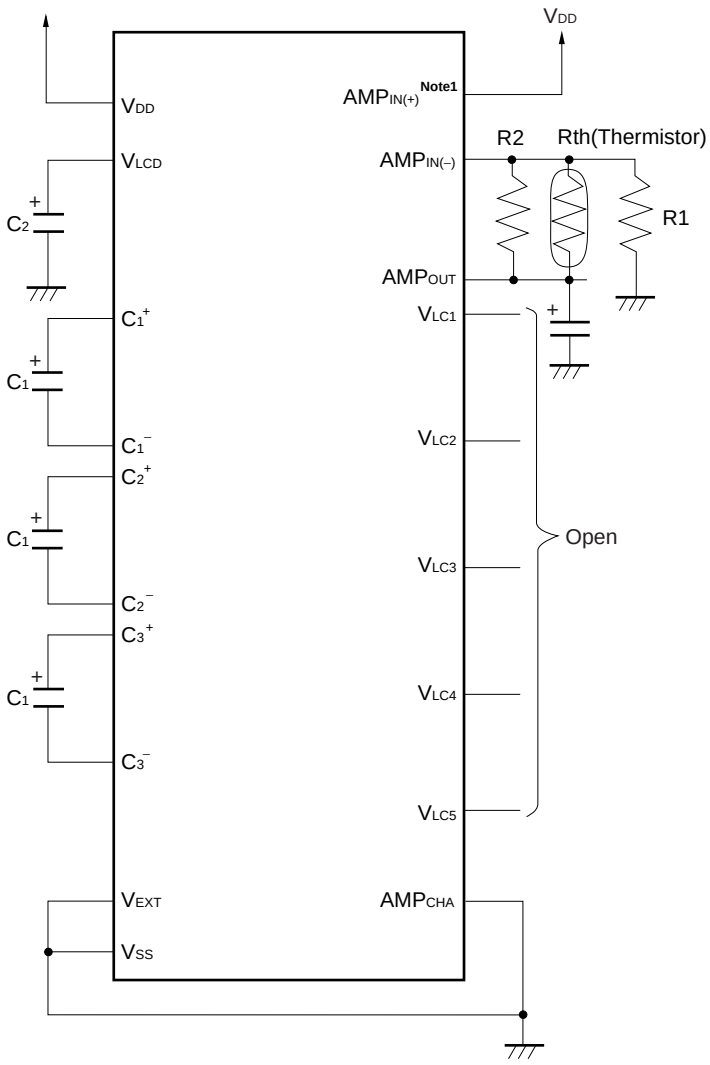
  When this mode is chosen, The voltage follower maximizes electric current supply ability for the external condenser charging. In this mode, it needs to connect the external capacitor (0.1 to 1.0 μF) for the level stability.

Caution When using this mode without connecting capacitor, the display dignity will be bad.

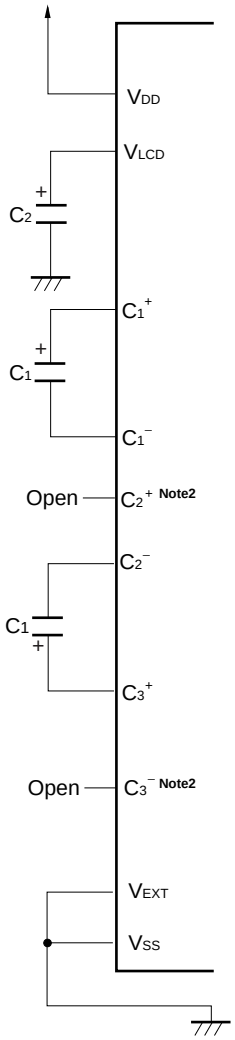
5.6 Application circuit example

5.6.1 To use internal driving circuit, LCD driving mode

A) Boost 4folds (not to use D/A converter)



B) Boost 3 folds



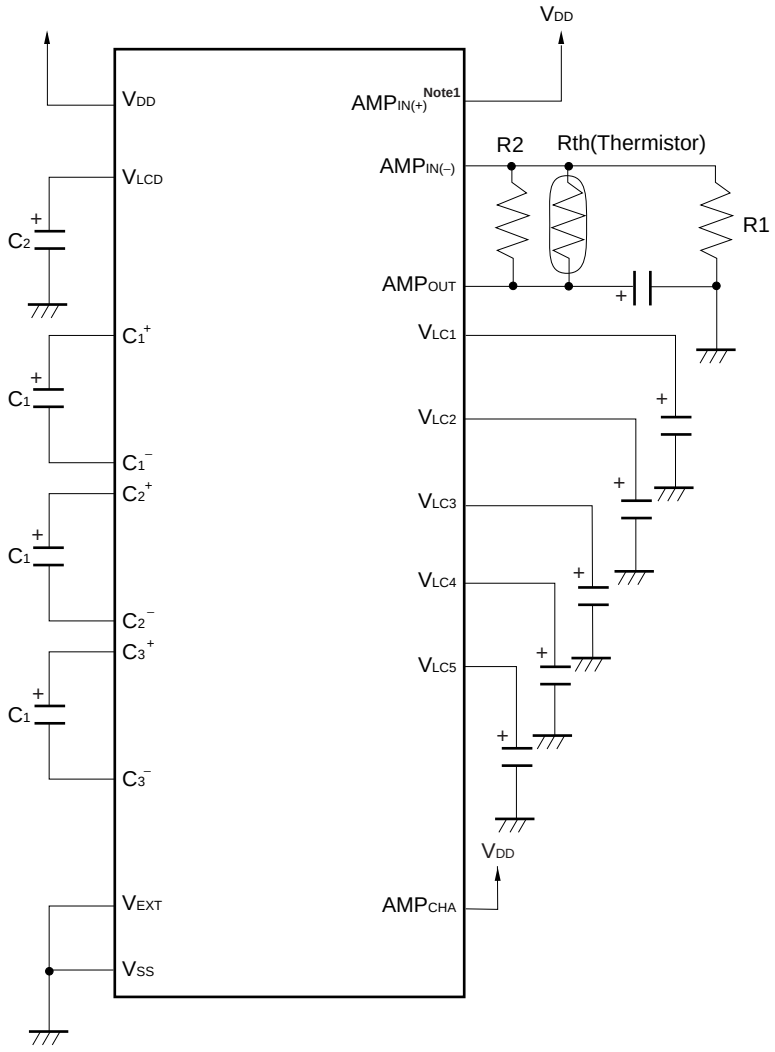
Notes 1. When to use D/A converter, $AMP_{IN(+)}$ is open.

2. C_2^+, C_3^- are open.

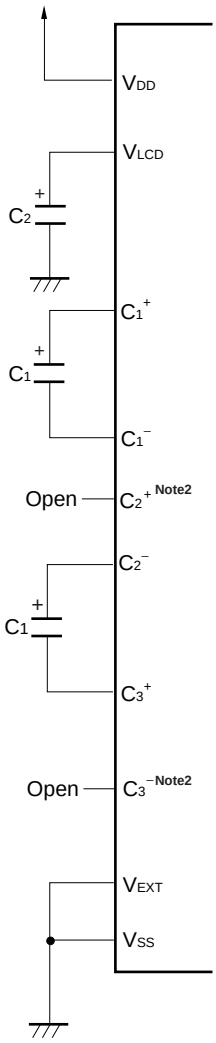
Remark C1 = C2 = 1.0 μm

5.6.2 To use internal driving circuit, LCD driving mode

A) Boost 4folds(not to use D/A converter)



B) Boost 3 folds



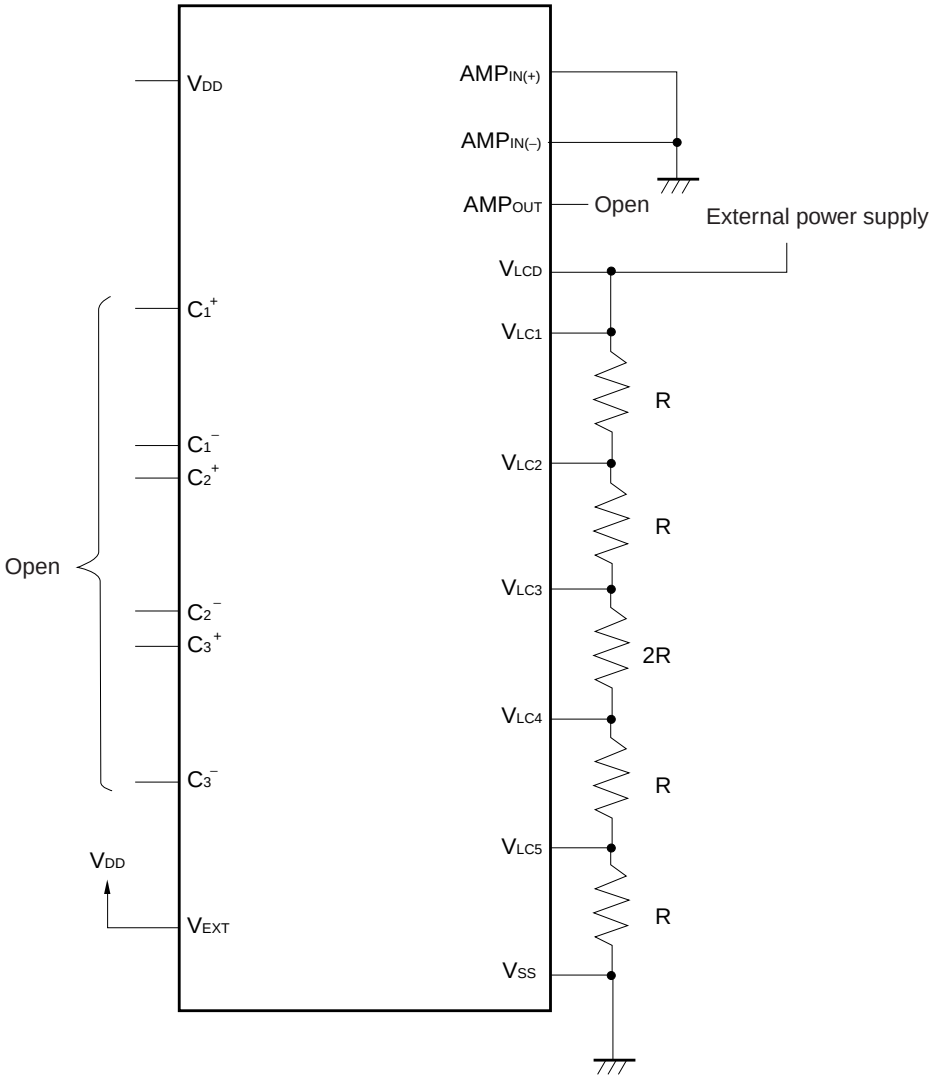
Notes 1. When to use D/A converter, $AMP_{IN(+)}$ is open.

2. C_2^+, C_3^- are open.

Remark C1 = C2 = 1.0 μm

5.6.3 To use external driving circuit

To use 1/6 bias

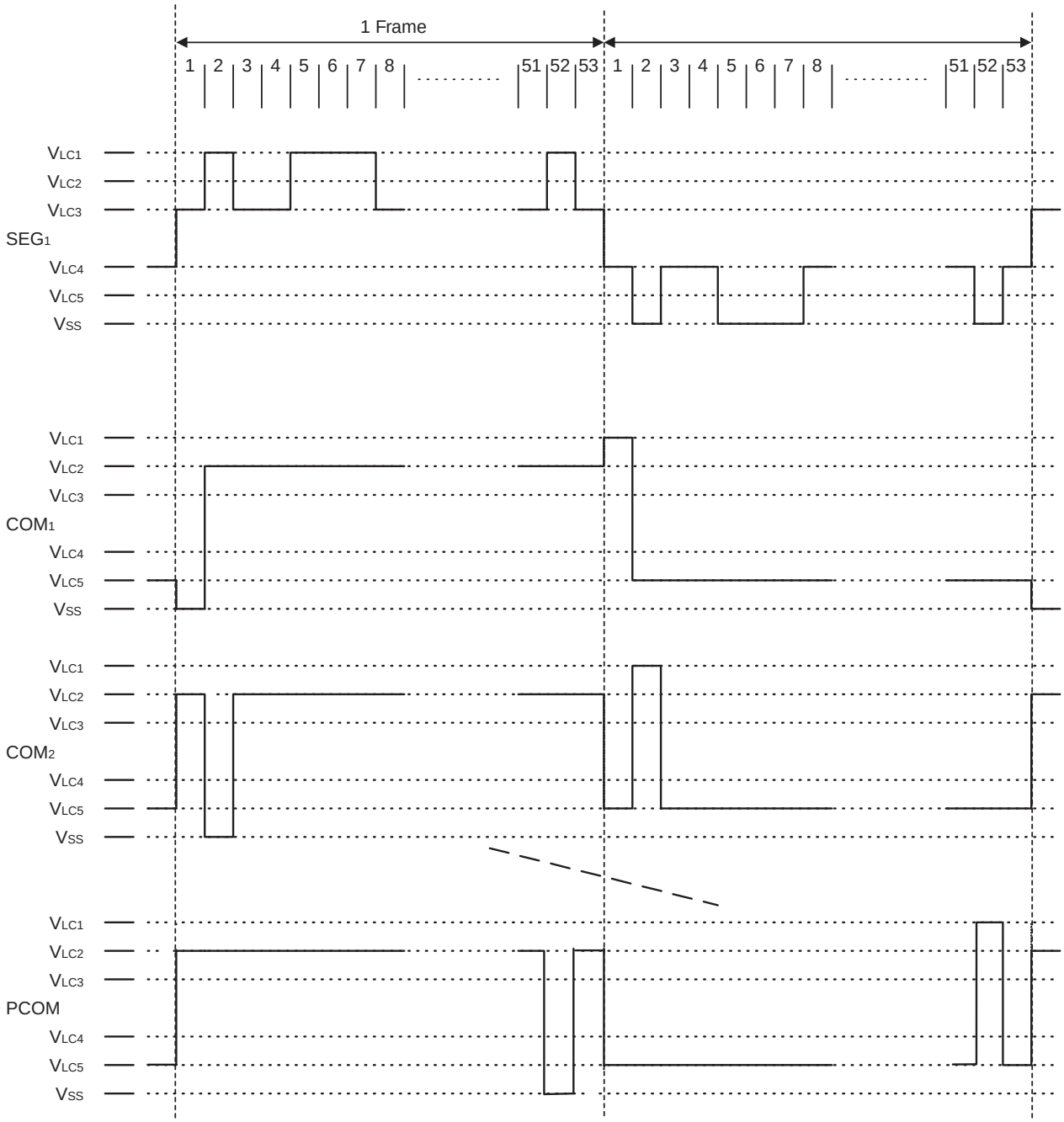


6. LCD DRIVING

The μPD16680 is able to choose duty 1/53 duty or 140 duty.

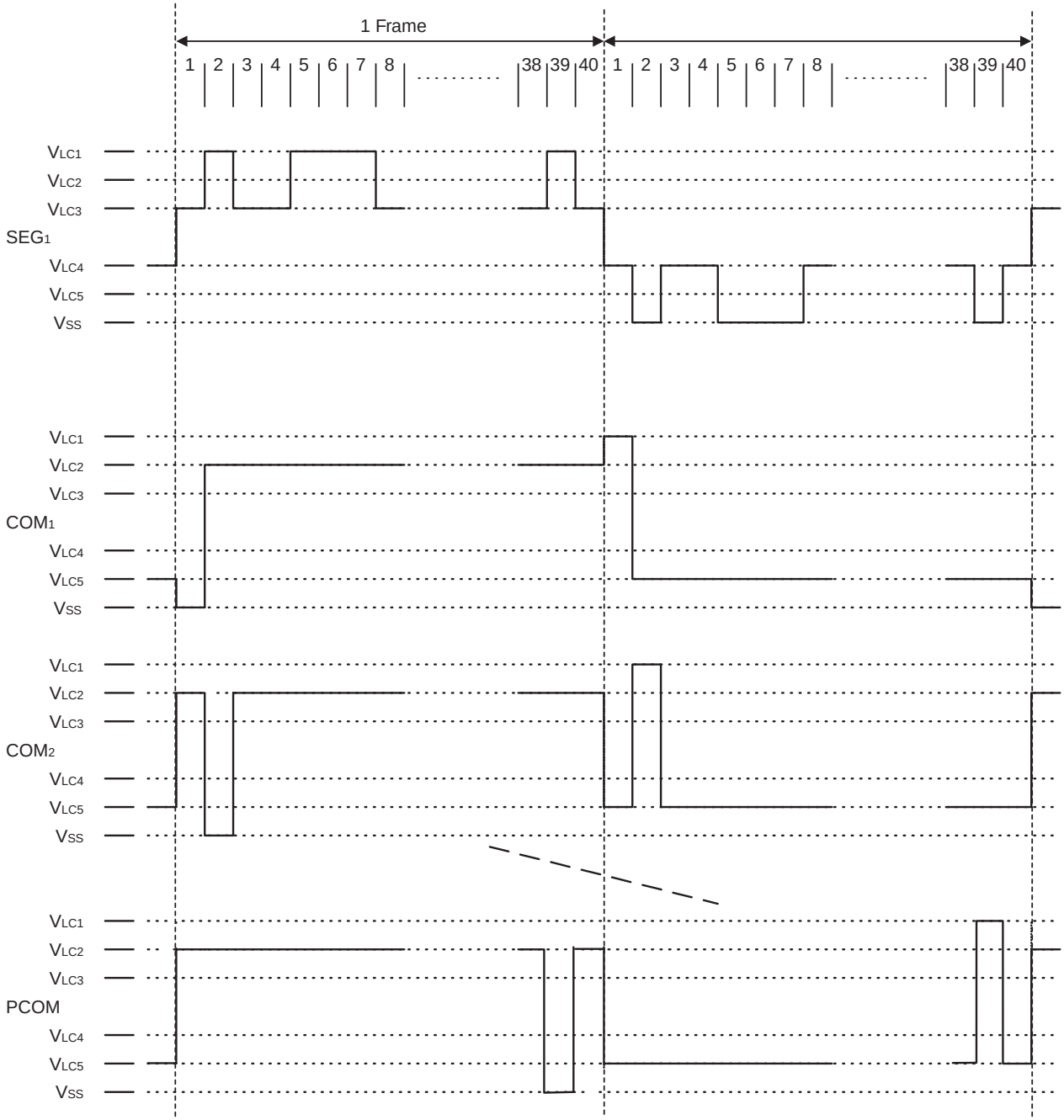
6.1 1/53 duty driving

When 1/53 duty is chosen, the μPD16680 outputs a choice signal once at 1 frame from the dot part common outputs (COM_1 to COM_{51}), the pictograph part common outputs (PCOM).



6.2 1/40 duty driving

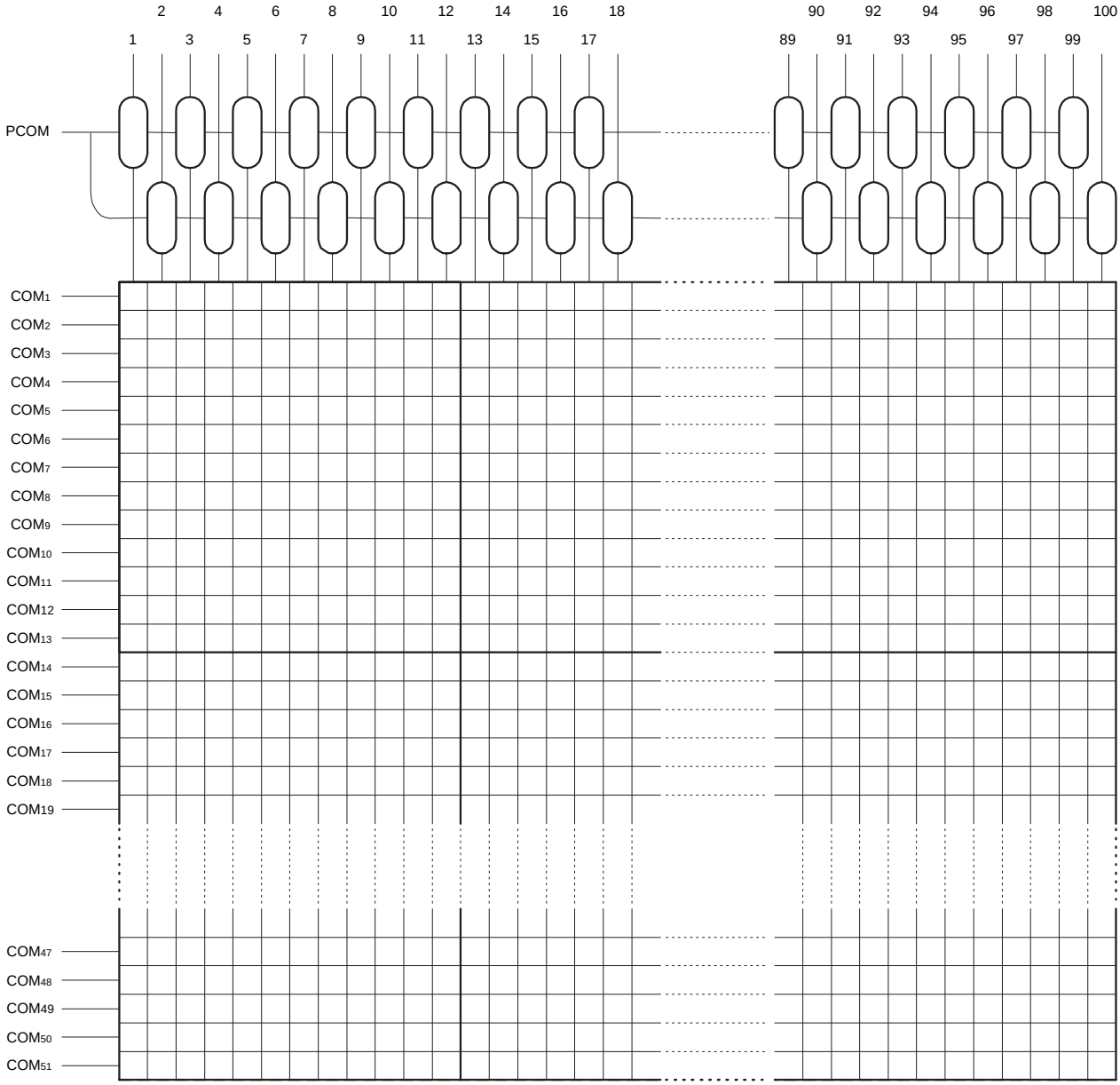
When 1/40 duty is chosen, the μPD16680 outputs a choice signal once at 1 frame from the dot part common outputs (COM_1 to COM_{19}, COM_{27} to COM_{45}), the pictograph part common outputs (PCOM).



7. LCD DISPLAY

The μPD16680 can display 100 by 51 dots (called full-dot display) LCD display and 100 pictographs.

Figure 7-1 LCD matrix

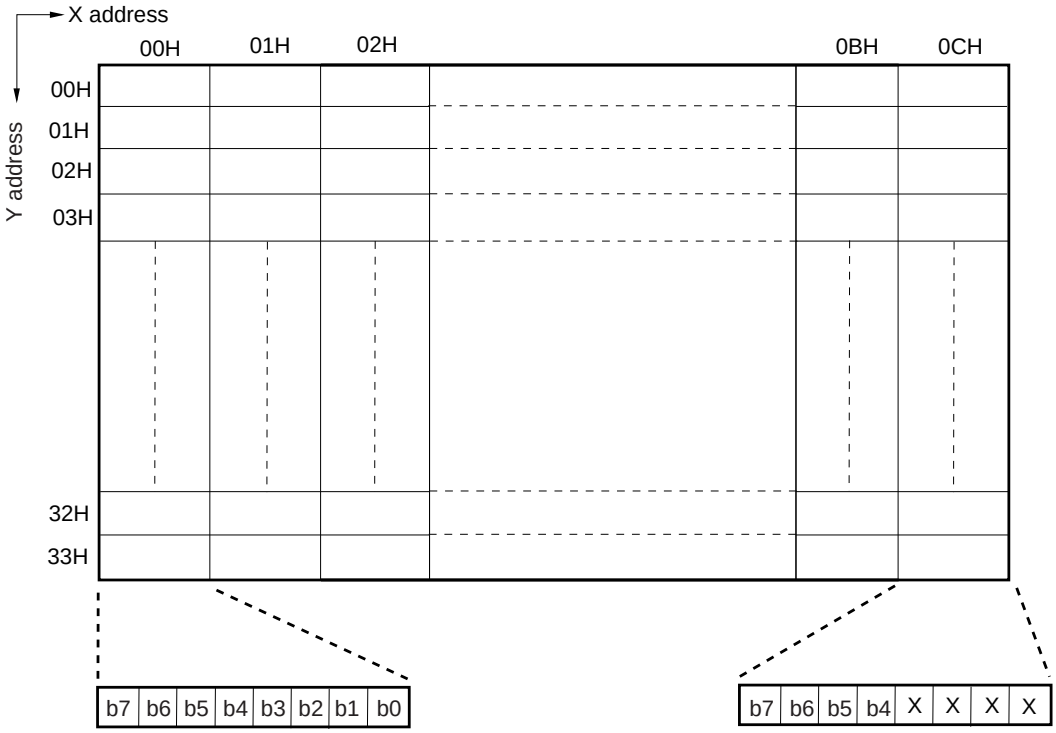


8. GROUP ADDRESSES

8.1 Dot display

The group addresses of dot display are assigned as follows.

To be chosen the address is increment, when X address goes to 0CH, next address is 00H. At this time, Y address goes to next address. When Y address goes to 33H, next address is 00H, too.



Remark Data of X address = 0CH : b7 to b4 are data, b3 to b0 are don't care.

★ When 1/53 duty and using 1/40 duty are used, the RAM addresses and the common pins used are as follows.

Duty	Use RAM Y addresses	Don't use RAM Y addresses	Use common pins	Don't use common pins
1/53 duty	00H to 33H	-	COM1 to COM51	-
1/40 duty	00H to 12H 1AH to 2CH[Note]	13H to 19H 2DH to 33H	COM1 to COM19 COM27 to COM45	COM20 to COM26 COM46 to COM51

Note If address incrementation is set when 1/40 duty is used, the X address value following 0CH is 00H. At the same time the Y address is incremented by 1. The Y address value following 12H is 1AH, and the value following 2CH is 00H.

8.2 Pictograph

The group addresses of pictograph are assigned as follows.

To be chosen the address is increment, X address goes to 0CH, next address is 00H.

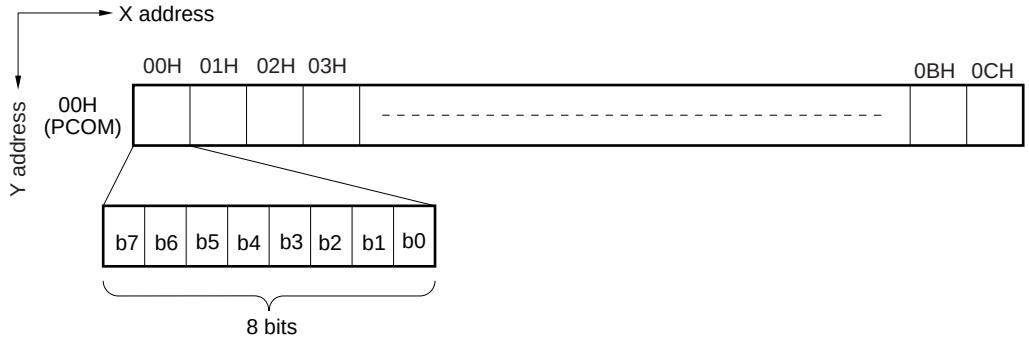


Table 8-1 PCOM (Y address = 00H)

X address	Segment output No.							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	1	2	3	4	5	6	7	8
01H	9	10	11	12	13	14	15	16
02H	17	18	19	20	21	22	23	24
03H	25	26	27	28	29	30	31	32
04H	33	34	35	36	37	38	39	40
05H	41	42	43	44	45	46	47	48
06H	49	50	51	52	53	54	55	56
07H	57	58	59	60	61	62	63	64
08H	65	66	67	68	69	70	71	72
09H	73	74	75	76	77	78	79	80
0AH	81	82	83	84	85	86	87	88
0BH	89	90	91	92	93	94	95	96
0CH	97	98	99	100	X	X	X	X

Remark Data of X address = 0CH :b7 to b4 are data, b3 to b0 are don’t care.

8.3 Blink data

The group addresses of brink data are assigned as follows.

To be chosen the address is increment, when X address goes to 0CH, next address is 00H.

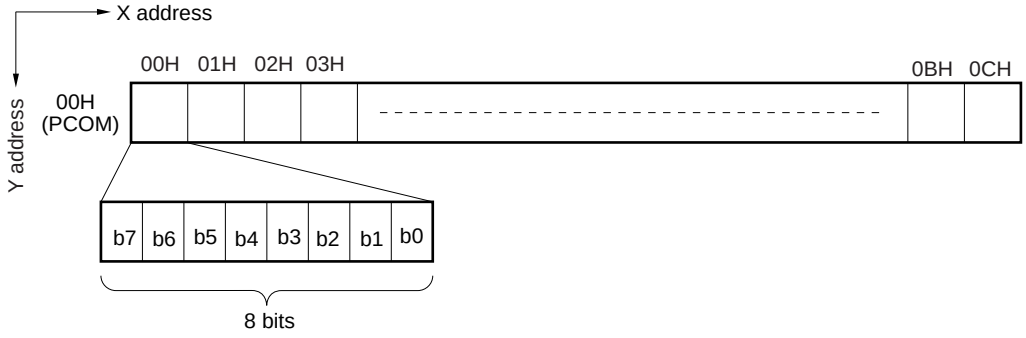


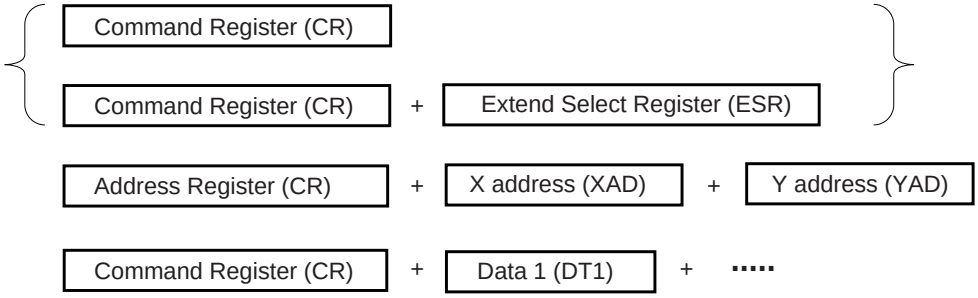
Table 8-2 PCOM (Y address = 00H)

X address	Segment output No.							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	1	2	3	4	5	6	7	8
01H	9	10	11	12	13	14	15	16
02H	17	18	19	20	21	22	23	24
03H	25	26	27	28	29	30	31	32
04H	33	34	35	36	37	38	39	40
05H	41	42	43	44	45	46	47	48
06H	49	50	51	52	53	54	55	56
07H	57	58	59	60	61	62	63	64
08H	65	66	67	68	69	70	71	72
09H	73	74	75	76	77	78	79	80
0AH	81	82	83	84	85	86	87	88
0BH	89	90	91	92	93	94	95	96
0CH	97	98	99	100	X	X	X	X

Remark Data of X address = 0CH :b7 to b4 are data, b3 to b0 are don't care.

9. COMMAND

9.1 Basic form



9.2 Command register

The command register's basic configuration is as follows.

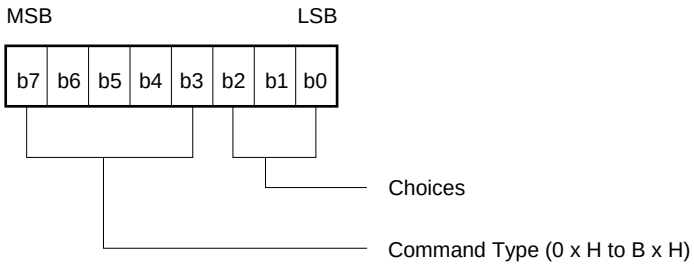


Table 7-1 Command Table

Command	Register							
	D7	D6	D5	D4	D3	D2	D1	D0
Reset	0	0	1	0	0	1	1	1
Display ON/OFF	0	0	0	0	1	b2	b1	b0
Standby	0	0	0	1	0	b2	b1	b0
D/A converter setting	0	0	1	0	1	0	0	0
Duty setting	0	0	0	1	1	b3	b2	b0
Blink setting	0	1	0	0	0	b2	b1	b0
Data R/W mode	1	0	1	1	0	b2	b1	b0
Test mode	1	0	1	1	1	b2	b1	b0

9.2.1 Reset

The all IC's commands are initialized.

MSB							LSB
0	0	1	0	0	1	1	1

9.2.2 Display ON/OFF

ON/OFF of the display is controlled.

MSB							LSB
0	0	0	0	1	b2	b1	b0

Choices

000 : LCD OFF (SEG_n, COM_n, $PCOM_n = V_{ss}$)

001 : LCD OFF (SEG_n, COM_n, $PCOM_n$ = non-serective output)

111 : LCD ON

9.2.3 Standby

The DC/DC converter is stopped, thus reducing the supply current. This display is placed in the OFF state (SEGn, COMn = V_{SS}).

Even at Standby, it is possible to write command and data.

MSB							LSB
0	0	0	1	0	b2	b1	b0

Cohices

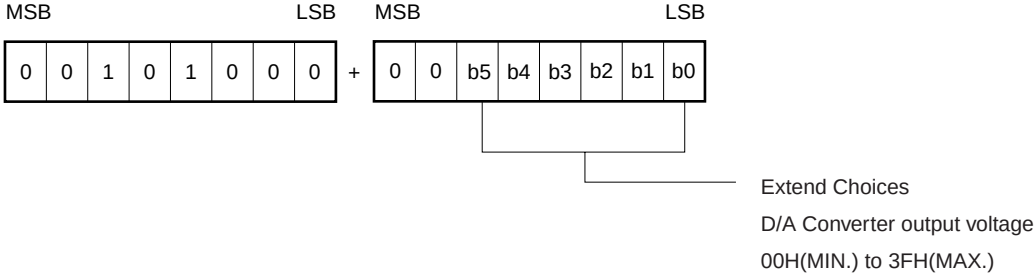
000 : Nomal operation

001 : Standby (DC/DC converter halt, all display OFF[Note], OSC halt)

Note SEG_n, COM_n, PCOM = V_{SS}

9.2.4 D/A converter setting

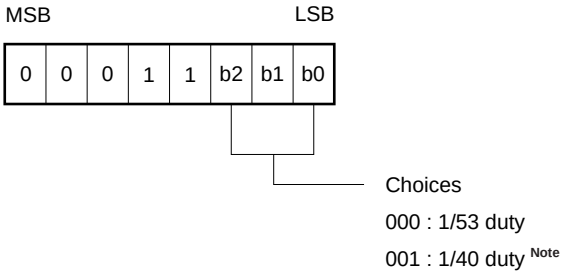
The internal D/A converter is set. D/A converter output voltage is controlled from 1/2V_{DD} to V_{DD}.



Caution After resetting, it is set to 20H.

9.2.5 Duty setting

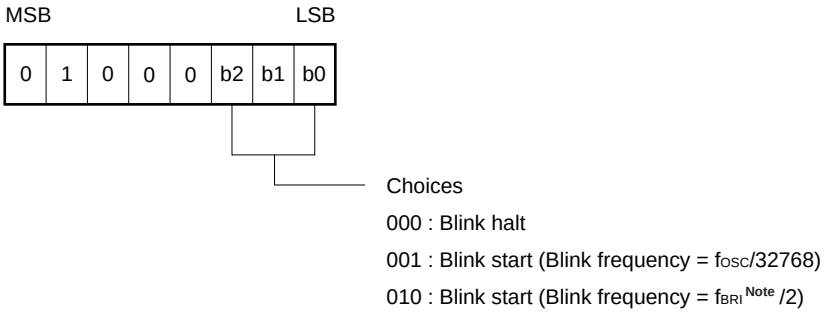
The duty is set.



Note If the duty cycle is 1/40, leave open from COM_{39} to COM_{51}.

9.2.6 Blink setting

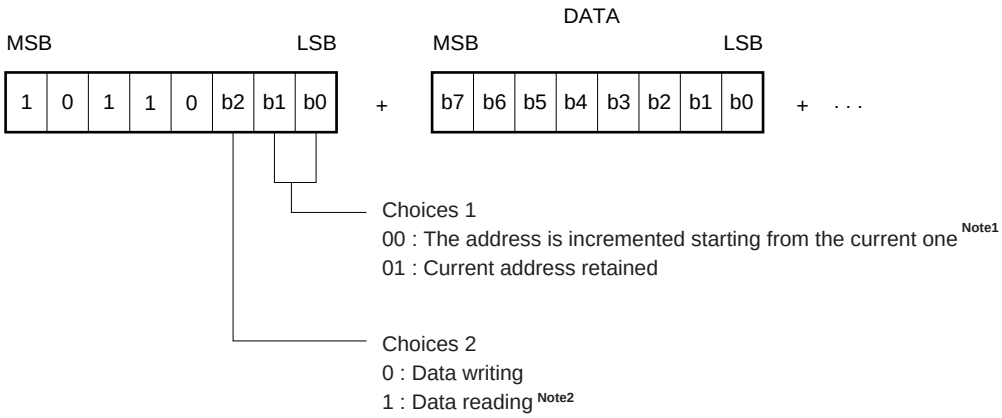
The blinks of the pictograph of the address whose blink data is “1” are controlled.



Note This refers to the frequency of the external clock which is input from the OSC_{BR1} pin.

9.2.7 Data R/W mode

Data Read/Write (R/W), increment, address counter resetting, etc. are set in this mode.



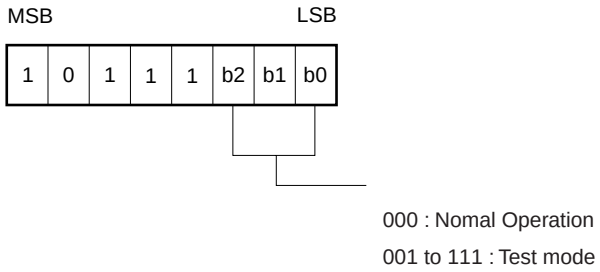
Notes 1. When X address and Y address goes to last address, next address is 00H.

2. The data read mode is canceled at STB's rising edge (Switched to data write mode).

Remark When using serial data transfer, it is necessary to write 8-bit data. No assurance is IC's operation when STB is rising during data transfer.

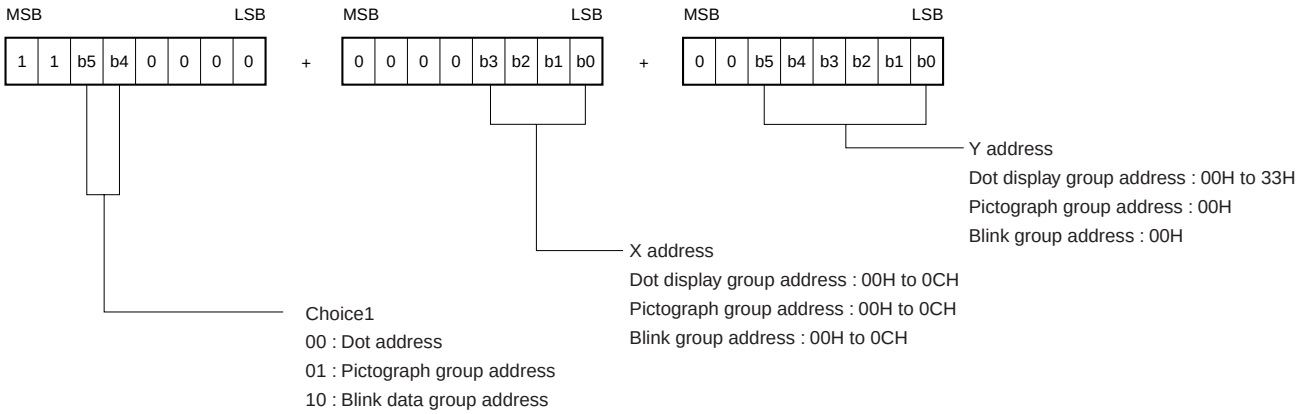
9.2.8 Test mode

The test mode is set. The test mode is for checking IC's operation, and no assurance is made for its regular use or continued operation.



★ 9.3 Address register

Selects the address type and specifies the address.



Caution If unspecified addresses have been set, operation is not assured.

10. RESETTING

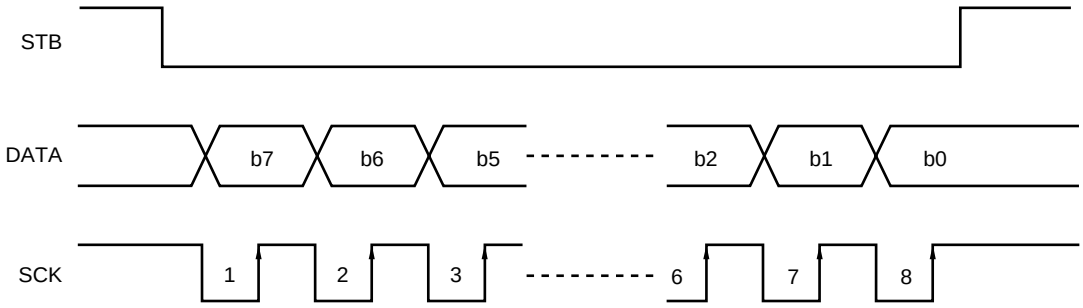
When reset (command reset, hardware (terminal) reset), the contents of each register are as follows.

Register name	Register contents								Status
	b7	b6	b5	b4	b3	b2	b1	b0	
Display ON / OFF	0	0	0	0	1	0	0	0	LCD OFF (SEG_n, COM_n, PCOM = V_{SS})
Standby	0	0	0	1	0	0	0	0	Normal operation
Duty setting	0	0	0	1	1	0	0	0	1/53 duty
D/A converter setting	1	0	0	0	0	0	0	0	To set 20H
Blink setting	0	1	0	0	0	0	0	0	Blink halt
Data R/W mode	1	0	1	1	0	0	0	0	Data write, the address is incremented(+1) starting from current address.
Test mode	1	0	1	1	1	0	0	0	Normal operation

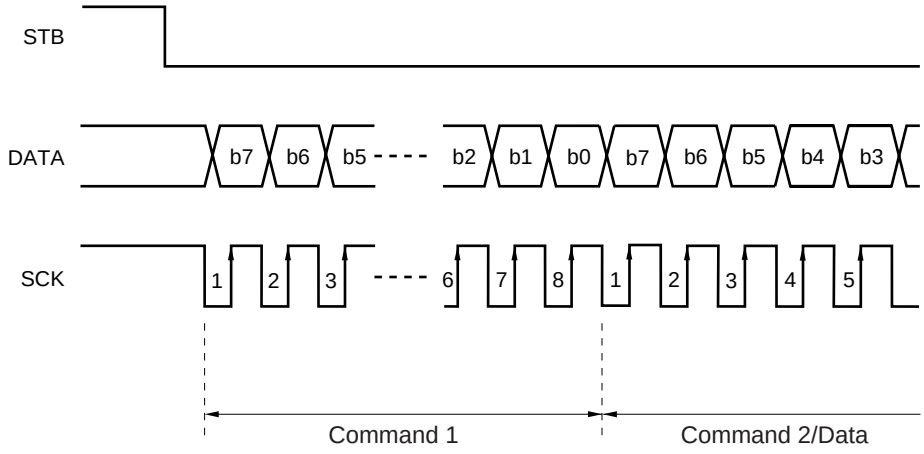
11. COMMUNICATION FORMAT

11.1 serial

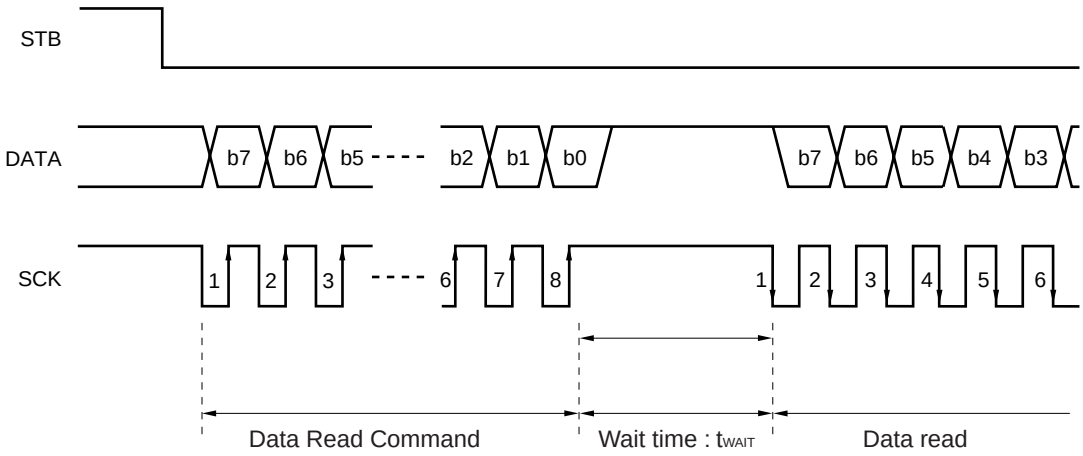
11.1.1 Reception 1 (Command/Data write : 1 byte)



11.1.2 Reception 2 (Command/Data write : 2 bytes or more)

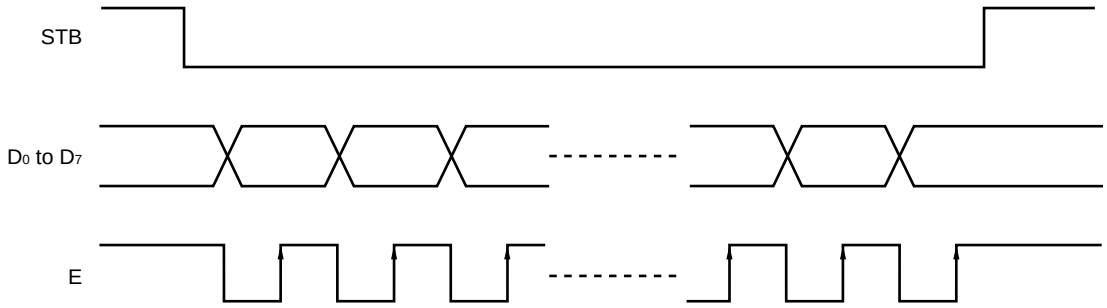


11.1.3 Transmission (Command/Data read)

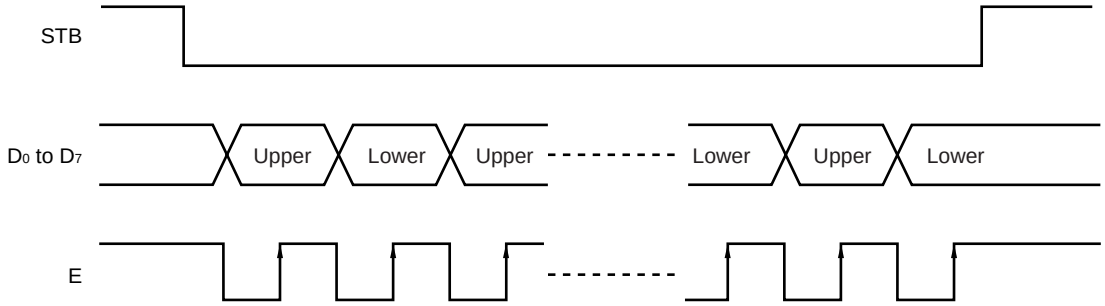


11.2 Parallel

11.2.1 8-bit parallel interface



11.2.2 4-bit parallel interface



12 CPU ACCESS EXAMPLE

12.1 Initialize and write data

Item	STB	Command / Data								Explanation
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	x	x	x	x	x	x	x	x	
Reset	L	0	0	1	0	0	1	1	1	
	H	x	x	x	x	x	x	x	x	
Duty setting	L	0	0	0	1	1	0	0	0	1/53 duty
	H	x	x	x	x	x	x	x	x	
Address Register 1	L	1	1	0	0	0	0	0	0	Dot address
Address Register 2	L	0	0	0	0	0	0	0	0	X address = 00H
Address Register 3	L	0	0	0	0	0	0	0	0	Y address = 00H
	H	x	x	x	x	x	x	x	x	
Data R/W mode	L	1	0	1	1	0	0	0	0	Data write, The address is incremented starting from the current one.
Dot display Data 1	L	D	D	D	D	D	D	D	D	Dot data (63 bytes)
Dot display Data 663	L	D	D	D	D	D	D	D	D	
	H	x	x	x	x	x	x	x	x	
Address Register 1	L	1	1	0	1	0	0	0	0	Pictograph group address
Address Register 2	L	0	0	0	0	0	0	0	0	X address = 00H
Address Register 3	L	0	0	0	0	0	0	0	0	Y address = 00H
	H	x	x	x	x	x	x	x	x	
Data R/W mode	L	1	0	1	1	0	0	0	0	Data write, The address is incremented starting from the current one.
Pictograph Data 1	L	D	D	D	D	D	D	D	D	Pictograph data (13 bytes)
Pictograph Data 13	L	D	D	D	D	D	D	D	D	
	H	x	x	x	x	x	x	x	x	
Display ON / OFF	L	0	0	0	0	1	1	1	1	LCD ON
End	H	x	x	x	x	x	x	x	x	

Remark x = Don't Care, D = data

12.2 Change display data and pictograph data (All data are changed)

Item	STB	Command / Data								Explanation
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	x	x	x	x	x	x	x	x	
Address Register 1	L	1	1	0	0	0	0	0	0	Dot address
Address Register 2	L	0	0	0	0	0	0	0	0	X address = 00H
Address Register 3	L	0	0	0	0	0	0	0	0	Y address = 00H
	H	x	x	x	x	x	x	x	x	
Data R/W mode	L	1	0	1	1	0	0	0	0	Data write, The address is incremented starting from the current one.
Dot display Data 1	L	D	D	D	D	D	D	D	D	Dot data (663 bytes)
Dot display Data 663	L	D	D	D	D	D	D	D	D	
	H	x	x	x	x	x	x	x	x	
Address Register 1	L	1	1	0	1	0	0	0	0	Pictograph group address
Address Register 2	L	0	0	0	0	0	0	0	0	X address = 00H
Address Register 3	L	0	0	0	0	0	0	0	0	Y address = 00H
	H	x	x	x	x	x	x	x	x	
Data R/W mode	L	1	0	1	1	0	0	0	0	Data write, The address is incremented starting from the current one.
Pictograph Data 1	L	D	D	D	D	D	D	D	D	Pictograph data (13 bytes)
Pictograph Data 13	L	D	D	D	D	D	D	D	D	
End	H	x	x	x	x	x	x	x	x	

Remark x = Don't Care, D = data

12.3 Read display data and pictograph data (All data are read)

Item	STB	Command / Data								Explanation
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	x	x	x	x	x	x	x	x	
Address Register 1	L	1	1	0	0	0	0	0	0	Dot address
Address Register 2	L	0	0	0	0	0	0	0	0	X address = 00H
Address Register 3	L	0	0	0	0	0	0	0	0	Y address = 00H
	H	x	x	x	x	x	x	x	x	
Data R/W mode	L	1	0	1	1	0	1	0	0	Data read, The address is incremented starting from the current one.
Dot display Data 1	L	D	D	D	D	D	D	D	D	Dot data (663 bytes)
Dot display Data 663	L	D	D	D	D	D	D	D	D	
	H	x	x	x	x	x	x	x	x	
Address Register 1	L	1	1	0	1	0	0	0	0	Pictograph group address
Address Register 2	L	0	0	0	0	0	0	0	0	X address = 00H
Address Register 3	L	0	0	0	0	0	0	0	0	Y address = 00H
	H	x	x	x	x	x	x	x	x	
Data R/W mode	L	1	0	1	1	0	1	0	0	Data read, The address is incremented starting from the current one.
Pictograph Data 1	L	D	D	D	D	D	D	D	D	Pictograph data (13 bytes)
Pictograph Data 13	L	D	D	D	D	D	D	D	D	
End	H	x	x	x	x	x	x	x	x	

Remark x = Don't Care, D = data

12.4 Blink data setting

	Item	STB	Command / Data								Explanation
			b7	b6	b5	b4	b3	b2	b1	b0	
	Start	H	x	x	x	x	x	x	x	X	
	Address Register 1	L	1	1	1	0	0	0	0	0	Blink group address
	Address Register 2	L	0	0	0	0	0	0	0	0	X address = 00H
	Address Register 3	L	0	0	0	0	0	0	0	0	Y address = 00H
		H	x	x	x	x	x	x	x	x	
	Data R/W mode	L	1	0	1	1	0	0	0	0	Data write, The address is incremented starting from the current one.
★	Blink Data 1	L	D	D	D	D	D	D	D	D	Blink data (13 bytes)
	Blink Data 13	L	D	D	D	D	D	D	D	D	
★		H	x	x	x	x	x	x	x	x	
★	Blink setting	L	0	1	0	0	0	0	1	0	Blink start, blink frequency = $f_{BRI}/2$
	End	H	x	x	x	x	x	x	x	x	

Remark x= Don't Care, D = data

13. ELECTRICAL SPECIFICATIONS

Absolute maximum ratings (T_A =+25°C, V_{SS} =0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (4-fold voltage mode)	V_{DD}	–0.3 to +3.75	V
Supply voltage (3-fold voltage mode)	V_{DD}	–0.3 to +5.0	V
Driver supply voltage	V_{LCD}	–0.3 to +15.0, $V_{DD} \leq V_{LCD}$	V
Driver reference supply input voltage	V_{LC1} to V_{LC5}	–0.3 to V_{LCD}+0.3	V
Logic system input voltage	V_{IN1}	–0.3 to V_{DD}+0.3	V
Logic system output voltage	V_{OUT1}	–0.3 to V_{DD}+0.3	V
Logic system input/output voltage	$V_{I/01}$	–0.3 to V_{DD}+0.3	V
Driver system input voltage	V_{IN2}	–0.3 to V_{LCD}+0.3	V
Driver system output voltage	V_{OUT2}	–0.3 to V_{LCD}+0.3	V
Operating temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +150	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended operating range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage (4-fold voltage mode)	V_{DD}	2.4		3.0	V
Supply voltage (3-fold voltage mode)	V_{DD}	2.4		4.0	V
Driver supply voltage[Note]	V_{LCD}	5.0	10	12	V
Logic system input voltage	V_{IN}	0		V_{DD}	V
Driver system input voltage	V_{LC1} to V_{LC5}	0		V_{LCD}	V

Note When to use external LCD driving, this parameter is recommended.

Remarks1. When to use external LCD driving, keep $V_{SS} < V_{LC5} < V_{LC4} < V_{LC3} < V_{LC2} < V_{LC1} \leq V_{LCD}$

2. When power on or power off moment, keep $V_{DD} \leq V_{LCD}$

3. When to use internal LCD driving circuit and not to use D/A converter, keep voltage inputted to $AMP_{IN(+)}$ pin to 1.0V to V_{DD}.

Electrical characteristics (Unless otherwise specified, T_A = –40 to +85°C, 4-fold voltage mode : V_{DD} = 2.7 to 3.0V or 3-fold voltage mode : V_{DD} = 2.7 to 4.0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	High-level input voltage	V_{IH}		0.8 V_{DD}			V
	Low-level input voltage	V_{IL}				0.2 V_{DD}	V
	High-level input current	I_{IH1}	Except D_O/DATA, D_1 to D_7			1	μA
	Low-level input current	I_{IL1}	Except D_O/DATA, D_1 to D_7			–1	μA
	High-level output voltage	V_{OH}	I_{OUT} = –1.5 mA, Except OSC_{OUT}	V_{DD}–0.5			V
	Low-level output voltage	V_{OL}	I_{OUT} = 4 mA, Except OSC_{OUT}			0.5	V
	High-level leakage current	I_{LOH}	D_O/DATA, D_1 to D_7 $V_{IN/OUT}$ = V_{DD}			10	μA
	Low -level leakage current	I_{LOL}	D_O/DATA, D_1 to D_7 $V_{IN/OUT}$ = V_{SS}			–10	μA
	Common output ON resistance	R_{COM}	V_{LCn}→COM_n, $V_{LCD} \geq 3V_{DD}$ IIoI = 50 μA			2	kΩ
	Segment output ON resistance	R_{SEG}	V_{LCn}→SEG_n, $V_{LCD} \geq 3V_{DD}$ IIoI = 50 μA			4	kΩ
★	Driver voltage (Booster voltage)	V_{LCD}	3-fold voltage mode	2.7 V_{DD}		3.0 V_{DD}	V
			4-fold voltage mode	3.6 V_{DD}		4.0 V_{DD}	V
★	Current consumption (V_{DD}) Level condenser mode	I_{DD11}	f_{OSC} = 32 kHz, Display-off data output V_{DD} = 3.0 V,3-fold voltage mode Not to access to RAM.			95	μA
			f_{OSC} = 32 kHz, Display-off data output V_{DD} = 3.0 V,4-fold voltage mode Not to access to RAM.			125	μA
★	Current consumption (V_{DD}) LCD driving mode	I_{DD12}	f_{OSC} = 32 kHz, Display-off data output V_{DD} = 3.0 V,3-fold voltage mode Not to access to RAM.			160	μA
			f_{OSC} = 32 kHz, Display-off data output V_{DD} = 3.0 V,4-fold voltage mode Not to access to RAM.			250	μA
	Driver current consumption (V_{DD}, Standby)	I_{DD21}	V_{DD} = 3.0 V			10	μA

Switching characteristics (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = 2.7 to 3.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	F_{OSC}	Self-oscillation	25	32	38	kHz
Transfer delay time 1	t_{PHL}	SCK↓ → DATA↓			100	ns
Transfer delay time 2	t_{PLH}	SCK↓ → DATA↑			300	ns

★ **Remarks 1.** The TYP. value is a reference value when T_A =+25°C.

2. The time for one frame is found from the following formula.

1 frame = 1/fosc x 8 x number of duties

(Example)

f_{OSC} = 32 kHz, 1/53, then the result is :

1 frame = 33 μs x 8 x 53 = 13.25 ms ≅ 75.5 Hz

Required conditions for timing (Unless otherwise specified, T_A = –40 to +85°C, V_{DD} = 2.7 to 3.3 V)

1. Common

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{OSC}	OSC_{IN} external clock	20	32	50	kHz
High-level clock pulse width	t_{WHC1}	OSC_{IN} external clock	10		25	μs
Low -level clock pulse width	t_{WLC1}	OSC_{IN} external clock	10		25	μs
High-level clock pulse width	t_{WHC2}	OSC_{BRI} external clock	400			ns
Low -level clock pulse width	t_{WLC2}	OSC_{BRI} external clock	400			ns
Rise/Fall time	t_r, t_f	OSC_{BRI} external clock			100	ns
Reset pulse width	t_{WRE}	/RESET pin	50			μs

Remark The TYP. value is a reference value when T_A =+25°C.

2. Serial interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Shift clock cycle	t_{CYK}	SCK	900			ns
High-level shift clock pulse width	t_{WHK}	SCK	295			ns
Low-level shift clock pulse width	t_{WLK}	SCK	295			ns
Shift clock hold time	t_{HSTBK}	STB↓ → SCK↓	400			ns
Data setup time	t_{DS1}	DATA → SCK↑	40			ns
Data hold time	t_{DH1}	SCK↑ → DATA	40			ns
STB hold time	t_{HKSTB}	SCK↑ → STB↑	400			ns
STB pulse width	t_{WSTB}		210			ns
Wait time[Note]	t_{WAIT}	8th CLK↑ →1st CLK↓	100			ns

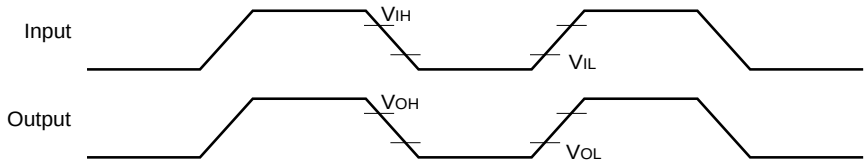
Note See **11.1.3 Transmission (Command/Data read)**.

3. Parallel interface

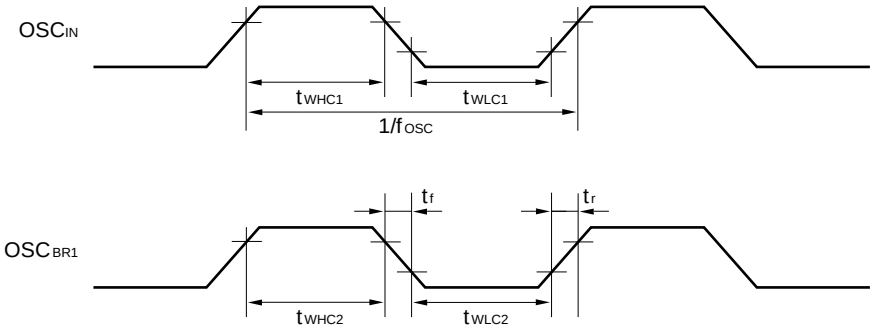
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Enable cycle time	t_{CYCE}	E↑ → E↑	900			ns
High-level enable pulse width	t_{WHE}	E	295			ns
Low-level enable pulse width	t_{WLE}	E	295			ns
STB pulse width	t_{WSTB}		210			ns
STB hold time	t_{HKSTB}		400			ns
Enable hold time	t_{HSTBK}		400			ns
Data setup time	t_{DS2}	D_0 to D_7 → E↑	40			ns
Data hold time	t_{DH2}	D_0 to D_7 → E↓	40			ns

Switching characteristics waveforms

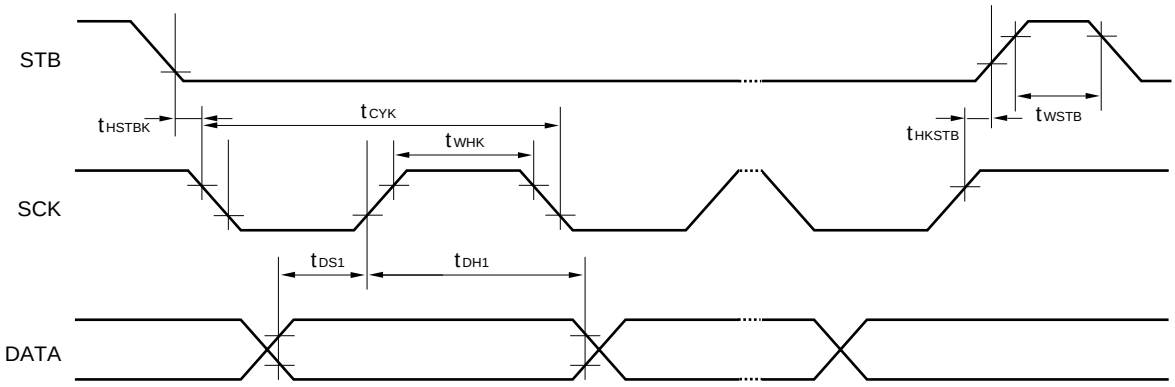
AC measurement point



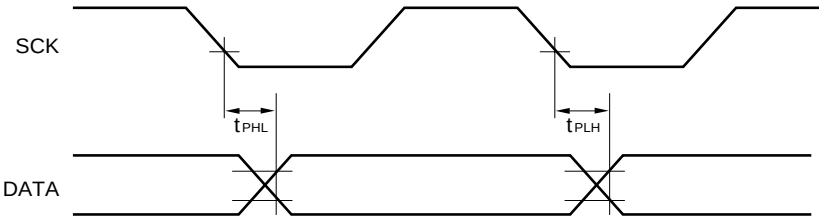
AC characteristics waveform



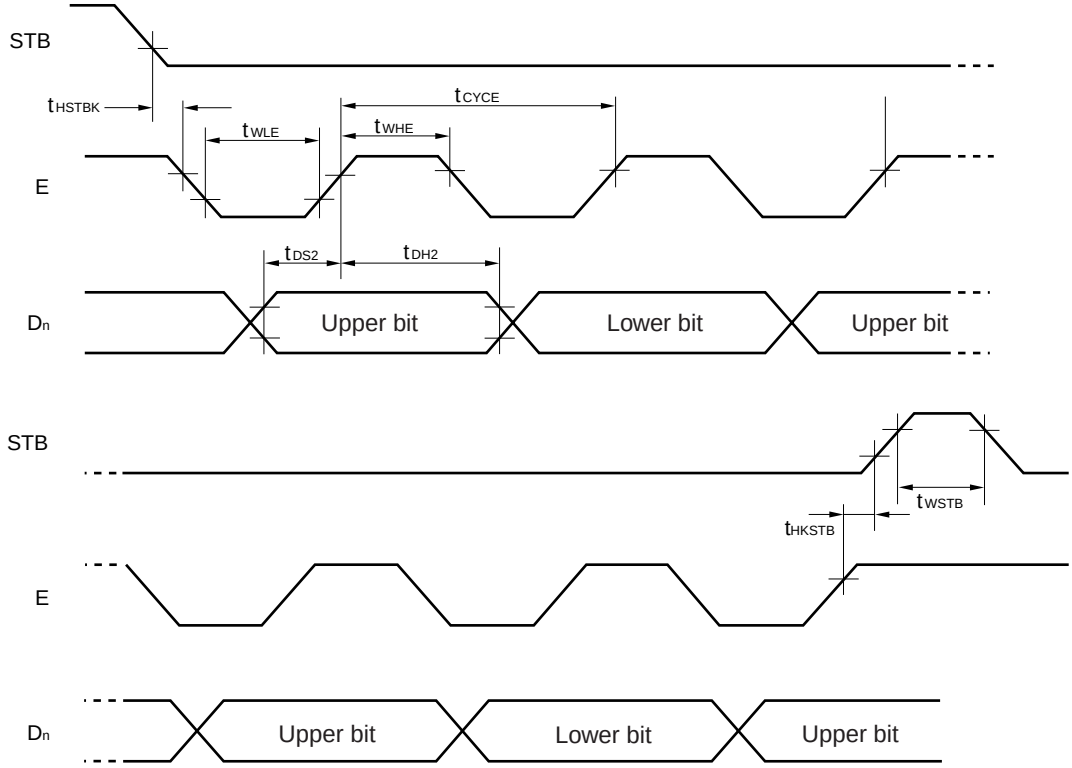
Serial interface (Input)



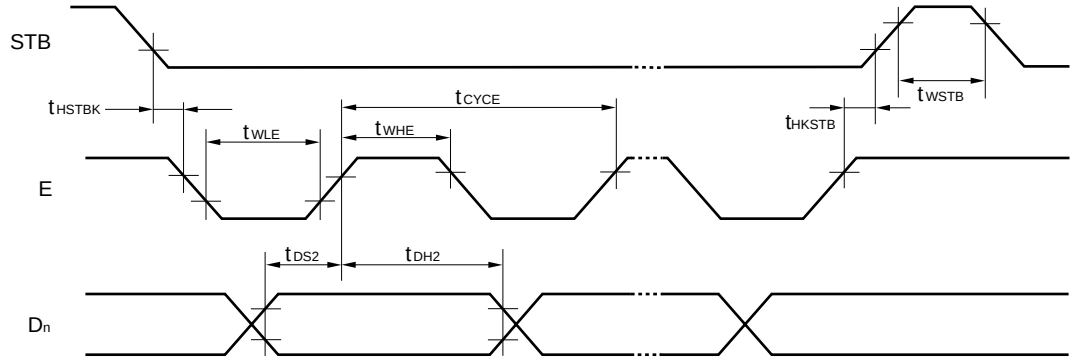
Serial interface (Output)



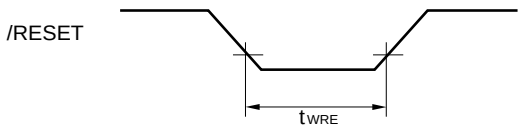
4-bit parallel interface



8-bit parallel interface



Reset



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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