NEC

MOS INTEGRATED CIRCUIT

μPD16666A

240-OUTPUT LCD ROW DRIVER

DESCRIPTION

The μPD16666A is a row (common) driver which contains a RAM capable of full-dot LCD display. With 240 outputs, this driver can be combined with a column (segment) driver μPD16661A which contains a RAM to display VGA (640 by 480 dots), 1/2 VGA, or 1/4 VGA, etc. By combining it with the μPD16661A, the μPD16666A can provide four gray levels by frame rate control.

With its built-in display RAM in the column driver, the driver kit can reduce current consumption, thus making it most suitable for the display section of a PDA or portable terminal.

FEATURES

- LCD-driven voltage: 20 to 36 V
- Duty: 1/240
- Driving type: 2 lines selected simultaneously
- Output count: 240 outputs
- Capable of gray level display: 4 gray levels (frame rate control)

ORDERING INFORMATION

Part No.	Package
μPD16666AN-XXX	TCP (TAB)
μPD16666AN-051	Standard TCP (OLB: 0.2 mm pitch; folding)

The TCP's external shape is custom-ordered. Therefore, if you have a shape in mind, please contact an NEC salesperson.

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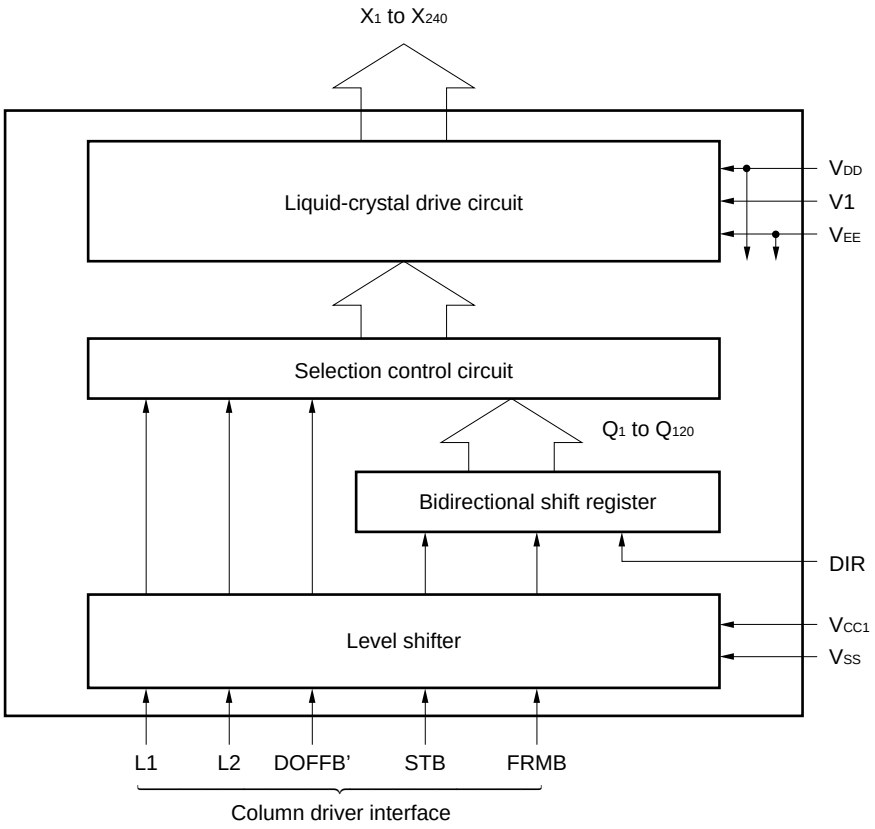
BLOCK DIAGRAM



BLOCK FUNCTION

1. Liquid-crystal drive circuit

This circuit selects and outputs the level for liquid-crystal driving.

One of V_{DD}, V_{EE}, and V1 is selected by the output of the selection control circuit.

2. Selection control circuit

This circuit creates the signal which will select the level of the output signal, based on the output of the shift register circuit and the driving level power selection signals L1 and L2

3. Bidirectional shift register circuit

This refers to the 120-bit bidirectional shift register circuit. The DIR signal can be used to switch over the shift direction.

The data that has been entered from the FRMB terminal is shifted by the row drive signal strobe (STB).

4. Level shifter circuit

This circuit transforms the 5-V signals to the high-voltage signals for liquid-crystal driving.

PIN FUNCTIONS

Classification	Pin Name	Input/Output	Pad No.	Function
Power	V_{CC1} V_{SS} V_{DD} V_{EE} V1			5 V power for level shifter GND power for level shifter Power for logic; liquid-crystal drive level power Power for logic; liquid-crystal drive level power (GND) Liquid-crystal drive level power
Liquid-crystal display timing	STB FRMB DOFFB' L1 L2 DIR	I I I I I I		Row drive strobe signal Frame signal Display OFF signal Drive level power selection signal (1st line) Drive level power selection signal (2nd line) Shift direction selection signal: when L (DIR = V_{EE}), $X_1 \rightarrow X_{240}$ when H (DIR = V_{DD}), $X_{240} \rightarrow X_1$
Liquid-crystal drive output	X_1 to X_{240}	O		Liquid-crystal drive output Selects and outputs one of V_{DD}, V_{EE}, and V1.

DETAILS OF PIN FUNCTIONS

- **STB (input)**
  Refers to the input pin of the row drive strobe signal.
  The bidirectional shift register is shifted at STB's rising edge.

- **FRMB (input)**
  Refers to the input pin of the frame signal.
  The shift register data is read at STB's rising edge.

- **DIR (input)**
  Refers to the input pin of the drive output's shift direction selection signal.
  When the shift direction selection signal (DIR) is "L", the shift data (selection signal) is shifted from the drive output X_1 to the X_{240} direction. When "H", it is shifted from the X_{240} to the X_1 direction.

- **DOFFB' (input)**
  Refers to the input pin of the display OFF signal.
  It is placed in the display OFF status (all outputs at V1) at the "L" level. In the mean time, it reads the frame signal and returns to the normal display status at the "H" level.

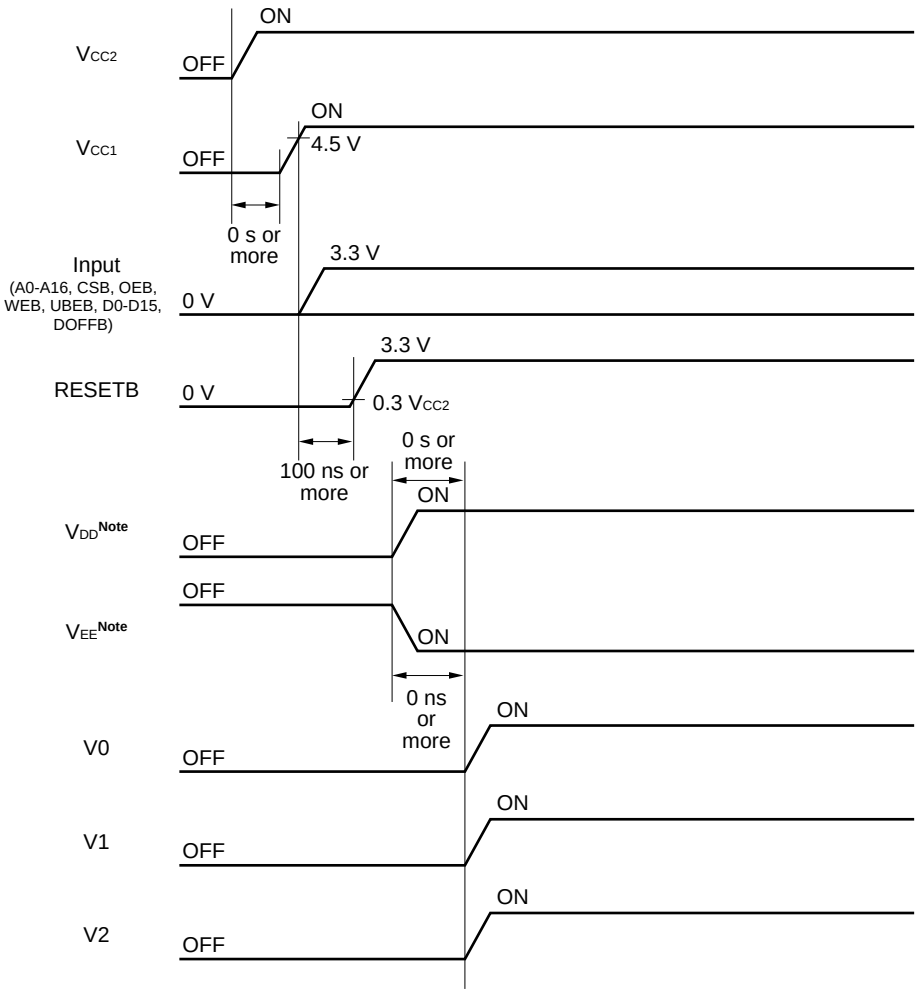
- **L1 & L2 (input)**
  Refer to the input pins of the drive level power selection signal.
  In the case of the liquid-crystal drive output, the two lines are selected simultaneously by the shift register. L1 selects the first line, and L2 the second line. Both lines select V_{DD} at "H", and V_{EE} at "L".

POWER SUPPLY SEQUENCE OF CHIP SET

It is recommended to apply power in the following sequence.

$V_{CC2} \rightarrow V_{CC1} \rightarrow$ input $\rightarrow V_{DD}, V_{EE} \rightarrow$ V0, V1, V2

Be sure to apply LCD drive voltages V0, V1, and V2 last.

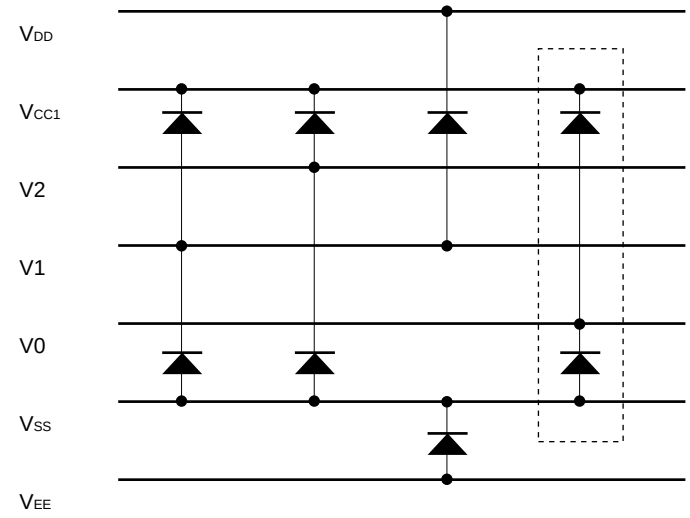


Note V_{DD} and V_{EE} do not need to be turned ON at the same time.

Caution Turn off power to the chip set in the reverse sequence to the power application sequence.

EXAMPLE OF CONNECTING INTERNAL SCHOTTKY BARRIER DIODE OF MODULE TO REINFORCE POWER SUPPLY PROTECTION

(Use a Schottky barrier diode with Vf = 0.5 V or less.)



Connect the diodes enclosed in the dotted line when V_0 is not 0 V (GND)

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage	V_{CC1}		–0.5 to +6.5	V
	$V_{DD} – V_{EE}$	$V_{CC1} \le V_{DD}$, $V_{EE} \le V_{SS}$	40	
	V1		V_{EE} – 0.5 to V_{DD} + 0.5	
Input Voltage	V_{I1}	Other than the DIR pin	–0.5 to V_{CC1} + 0.5	
	V_{I2}	DIR pin	V_{EE} – 0.5 to V_{DD} + 0.5	
Output Voltage	V_O		V_{EE} – 0.5 to +V_{DD} + 0.5	
Operating Temperature	T_A		–20 to +70	°C
Storage Temperature	T_{stg}		–40 to +125	

Recommended Operating Range (T_A = –20 to +70 °C, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC1}		4.75		5.25	V
	$V_{DD} – V_{EE}$	$V_{CC1} \le V_{DD}$, $V_{EE} \le V_{SS}$	20		36	
	V1		0		3	
Input Voltage	V_{I1}	Other than DIR pin	0		V_{CC1}	
	V_{I2}	DIR pin	V_{EE}		V_{DD}	

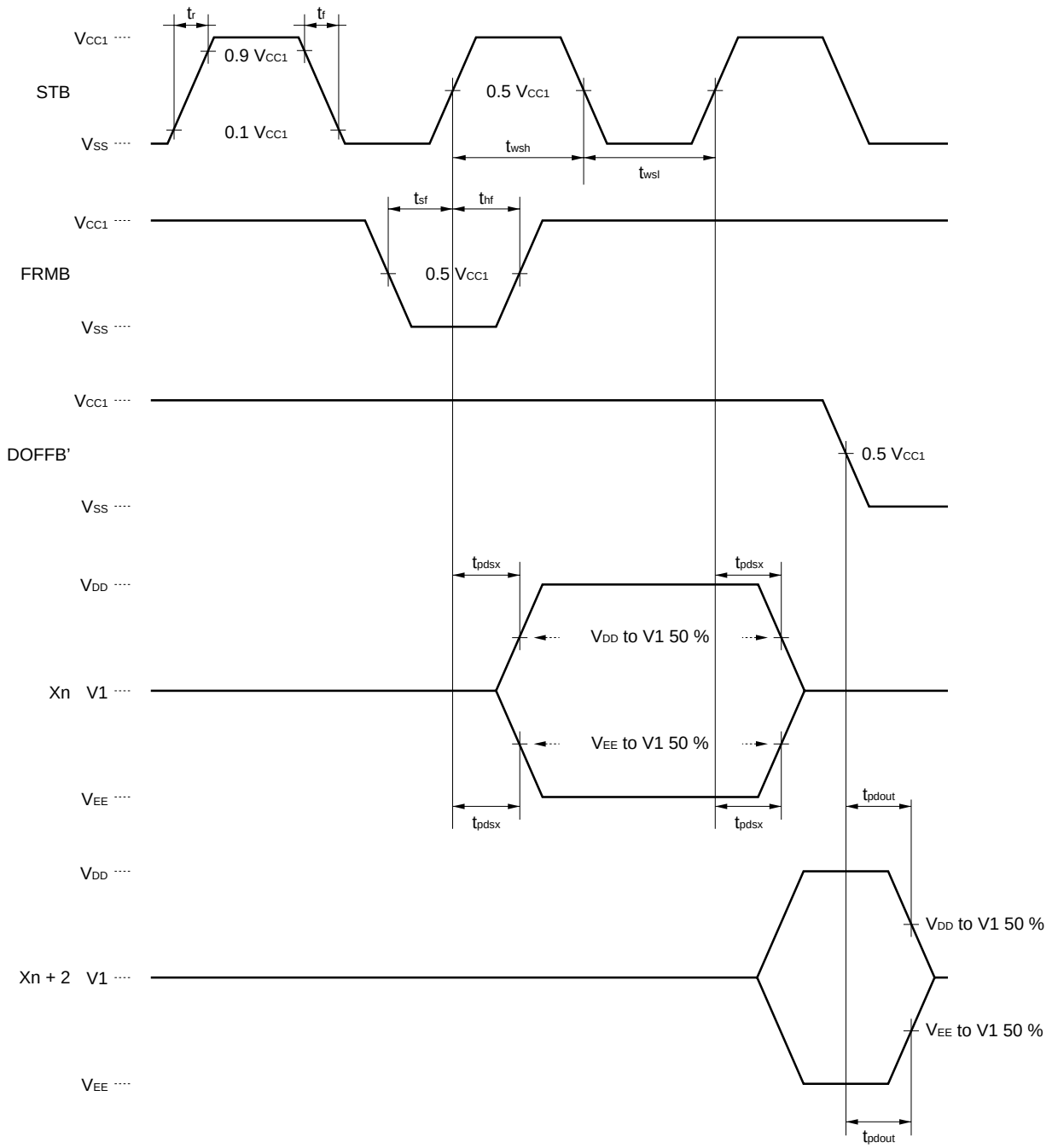
DC Characteristics (unless otherwise specified, V_{CC1} = 4.75 to 5.25 V, V_{DD} – (V_{EE}) = 20 to 31 V, $V_{CC1} \le V_{DD}$, $V_{EE} \le V_{SS}$, V1 = 0 to 3 V, V_{SS} = 0 V, T_A = – 20 to +70 °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Other than the DIR pin	0.8 V_{CC1}			V
	V_{IH2}	DIR pin	V_{DD}–0.3 (V_{DD}–V_{EE})			
Low-Level Input Voltage	V_{IL1}	Other than the DIR pin			0.2 V_{CC1}	
	V_{IL2}	DIR pin			V_{EE}+0.3 (V_{DD}–V_{EE})	
Driver ON Resistance	R_{ON}	Load current = 100 μA		1.0	2.0	kΩ
Input Leakage Current	I_{IH1}	V_{IN} = V_{CC}, other than the DIR pin			1.0	μA
	I_{IH2}	V_{IN} = V_{DD}, DIR pin			25	
	I_{IL1}	V_{IN} = 0 V, other than the DIR pin			–1.0	
	I_{IL2}	V_{IN} = V_{EE}, DIR pin			–25	
Current Consumption	I_{CC1}	Frame frequency 70 Hz at operation		200	320	μA
	I_{DD}			120	210	

AC Characteristics

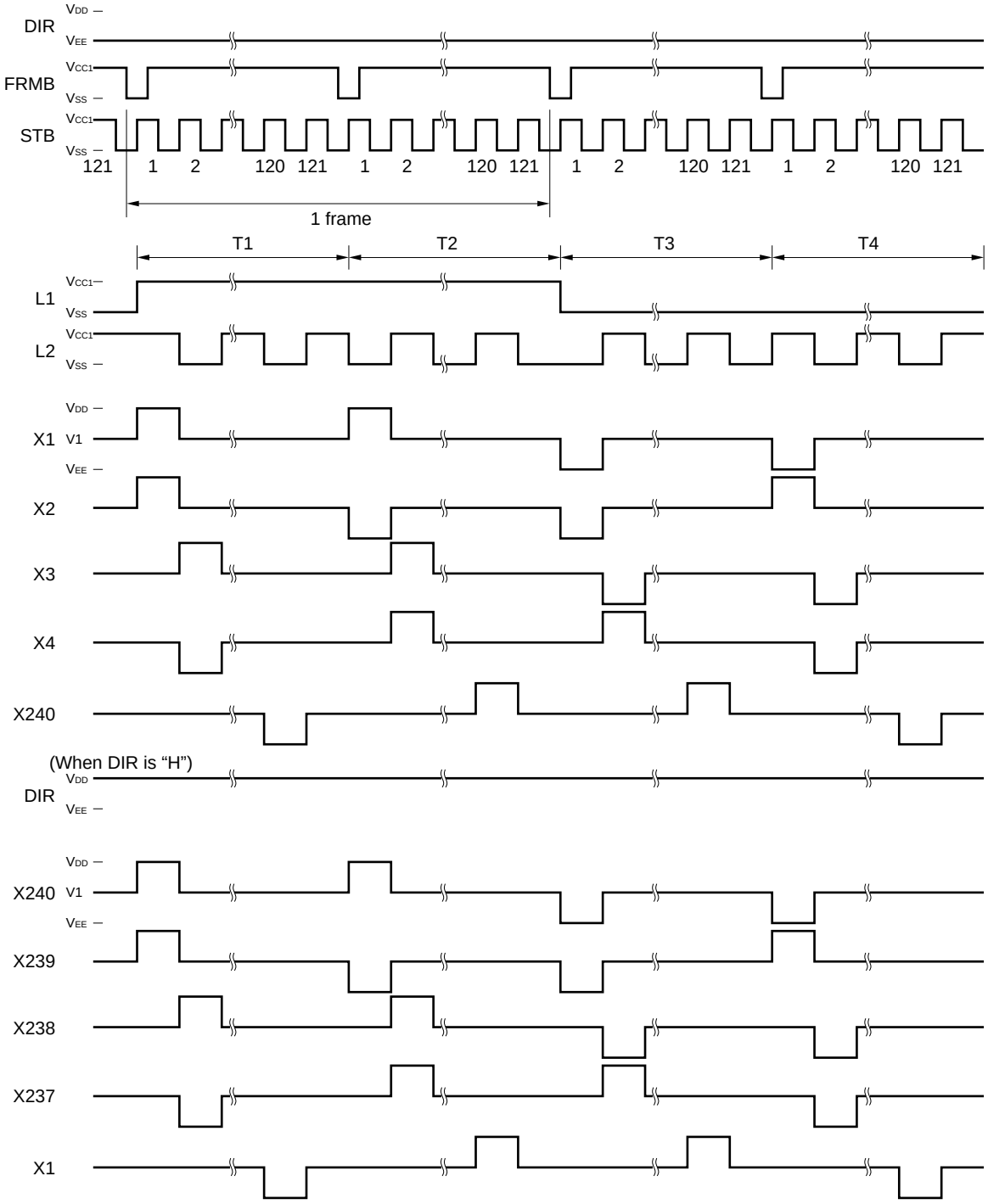
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
STB High-Level Width	t_{wsh}		500			ns
STB Low-Level Width	t_{wsl}		500			
FRMB Setup Time	t_{sf}		100			
FRMB Hold Time	t_{hf}		100			
STB Rise Time	t_r				150	
STB Fall Time	t_f				150	
Output Delay Time	t_{pdsx}	Output no-load			300	
	t_{pdout}				200	

AC CHARACTERISTICS WAVEFORM DIAGRAMS



LEVEL SELECTION TIMING OF LIQUID-CRYSTAL DRIVE OUTPUT

The FRMB is input in one frame twice. The STB is input into half a frame 121 times, and into one frame 242 times.



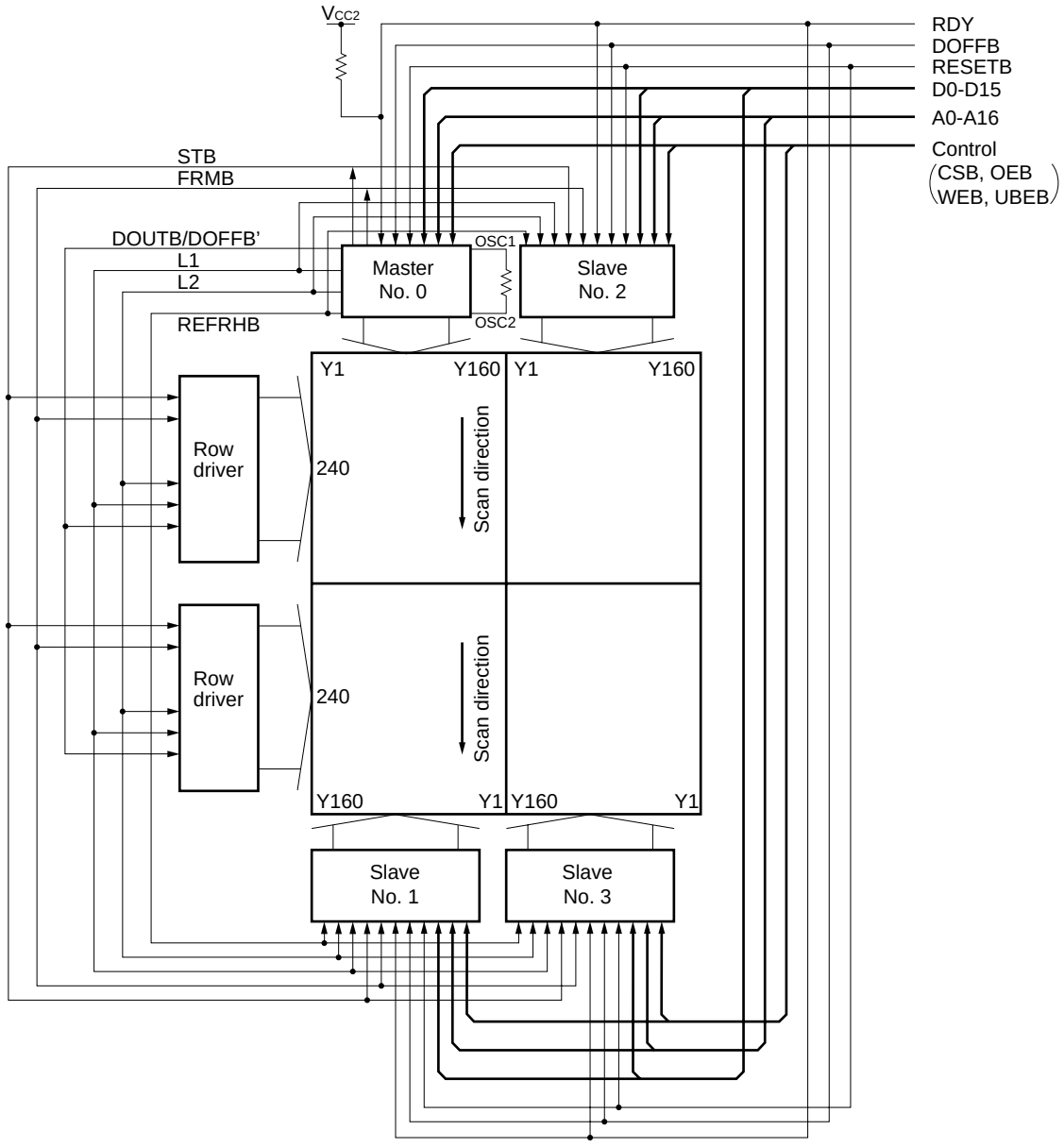
Remark While the DOFFB' is "L", the X output remains at the V1 level. Afterward, if it becomes "H", the level of the X output is output timed with the above timing.

Note When the time lag between STB signal and the L1, L2 signals is large, hazard may occur in output.

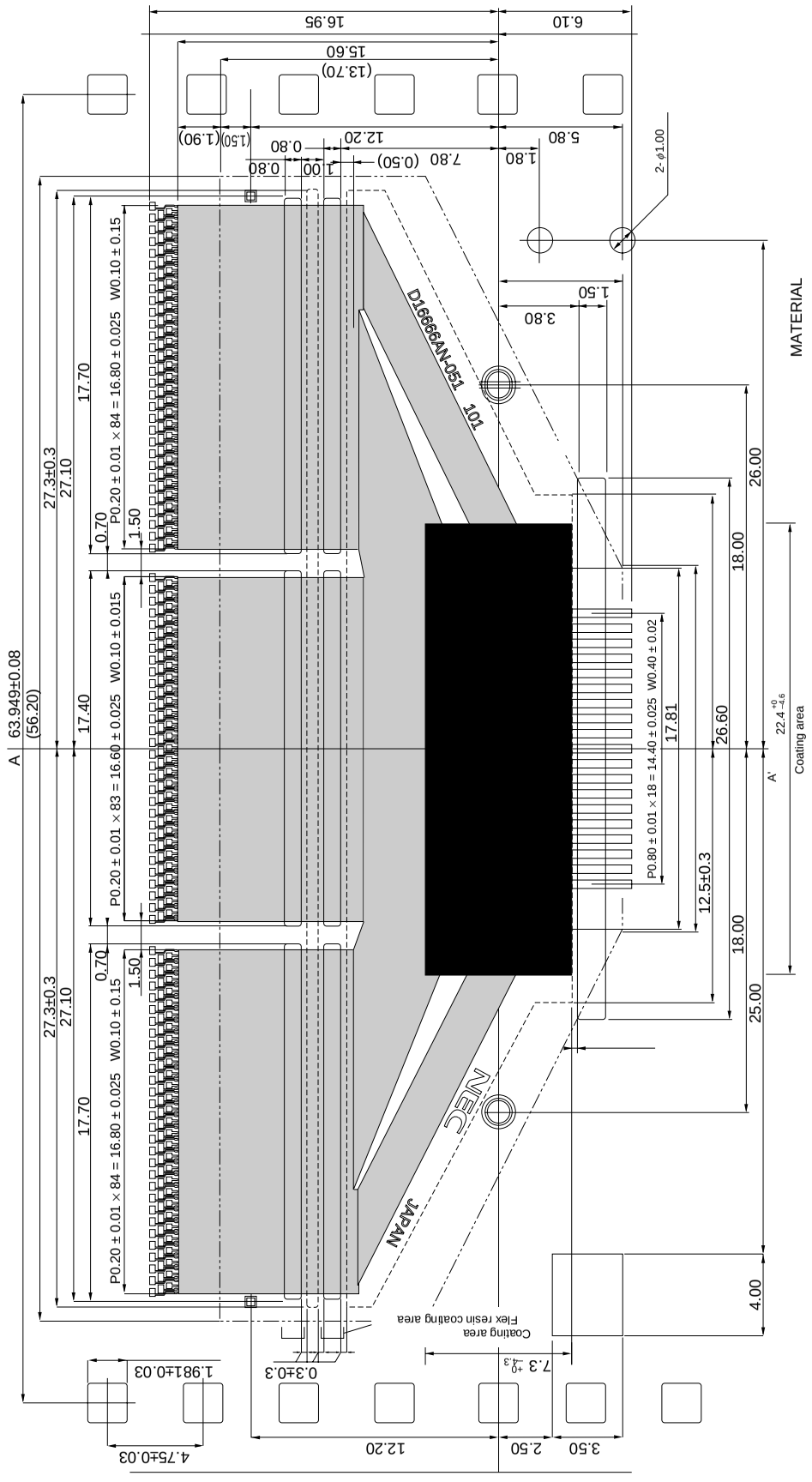
SYSTEM CONFIGURATION EXAMPLE

An example of configuring a liquid-crystal panel of half-VGA size (480 across by 320) by using four column drivers and two row drivers.

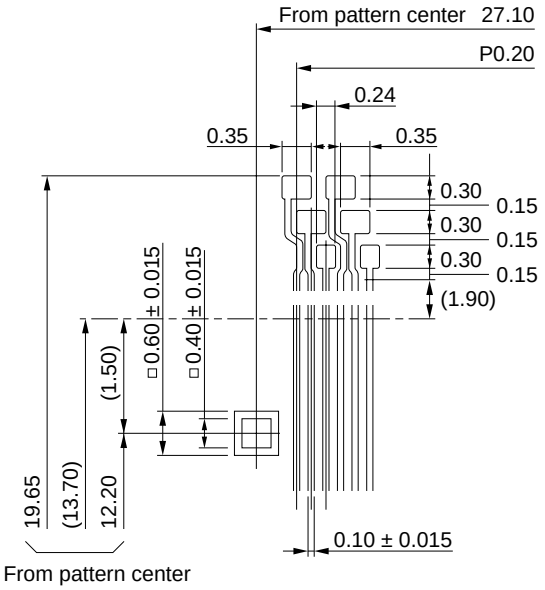
- Each column driver sets the LSI No. with PL0, 1, and 2 pins.
- The DIR pins of each column driver are all set to low level.
- Only one of the column drivers is set to the master; all the others are set to the slave. Signals are supplied from the master column driver to the slave column driver and to the row driver.
- Connect an oscillator resistor to the OSC1 and OSC2 pins on the master, and leave these pins open on the slave.
- All the signals from the system (D0 to D15, A0 to A16, CSB, OEB, WEB, UBEB, RDY, RESETB, and DOFFB) are connected in parallel to the column driver. Connect a pull-up resistor to the RDY signal.
- The TEST pin is used to test the LSI, and is open or grounded when the system is configured.



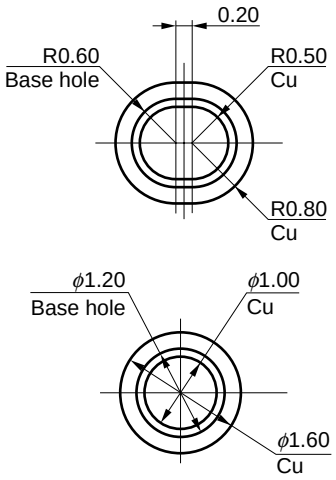
STANDARD TCP PACKAGE (μPD16666AN-051)



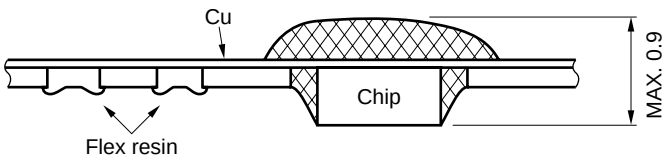
Detail of output side test pad and alignment mark (× 20)



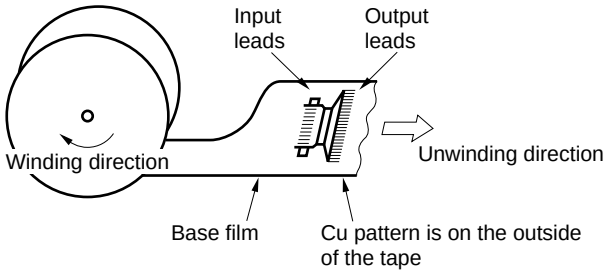
Detail of alignment hole (× 20)

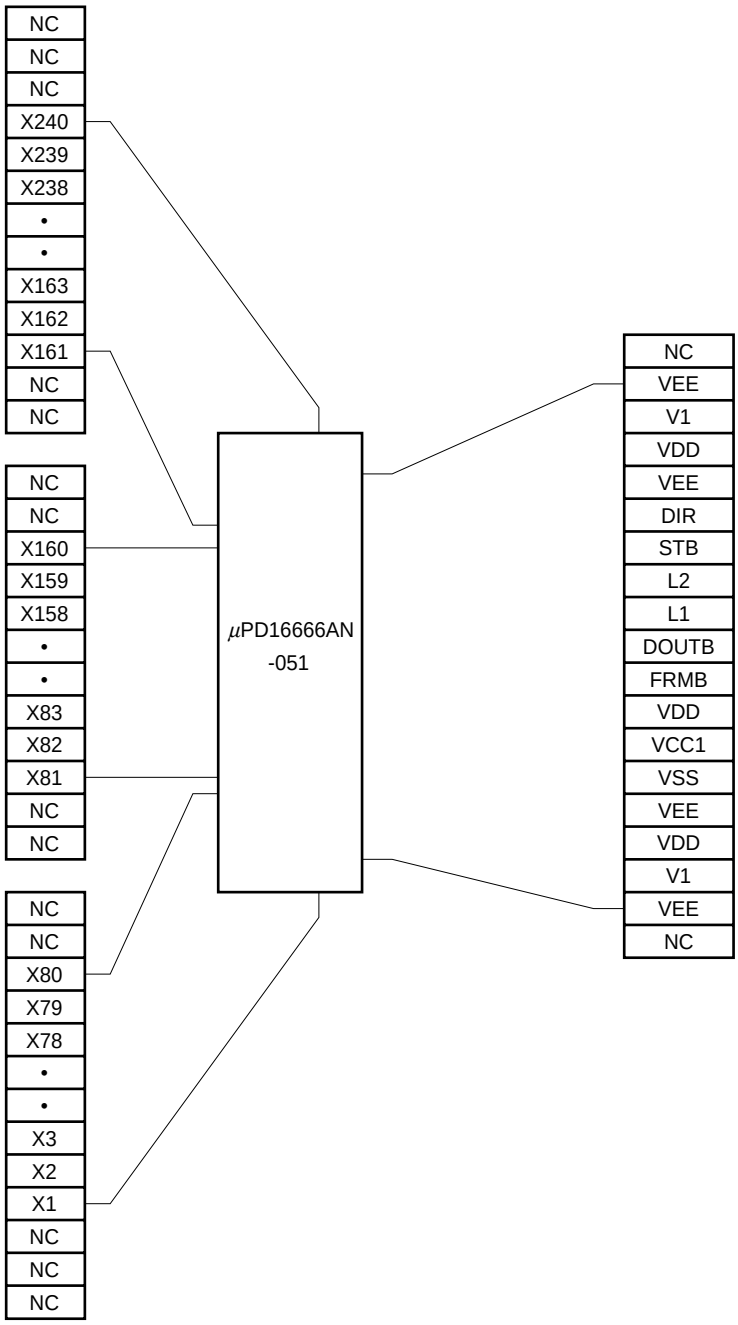


A - A' sectional view



TCP tape winding direction




NC
NC
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X160
X159
X158
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X81
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X80
X79
X78
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X3
X2
X1
NC
NC
NC
μPD16666AN
-051
NC
VEE
V1
VDD
VEE
DIR
STB
L2
L1
DOUTB
FRMB
VDD
VCC1
VSS
VEE
VDD
V1
VEE
NC

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