OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM65355

8-Bit Microcontroller with A/D Converter (with LCD Driver)

GENERAL DESCRIPTION

The MSM65355 is a high-performance 8-bit microcontroller that employs OKI original nX-8/50 CPU core. The MSM65355 includes 16K bytes of program memory, 384 bytes of data memory, an LCD driver, an A/D converter and shift registers. Also available is the MSM65P355, which replace the on-chip program memory with one-time PROM.

FEATURES

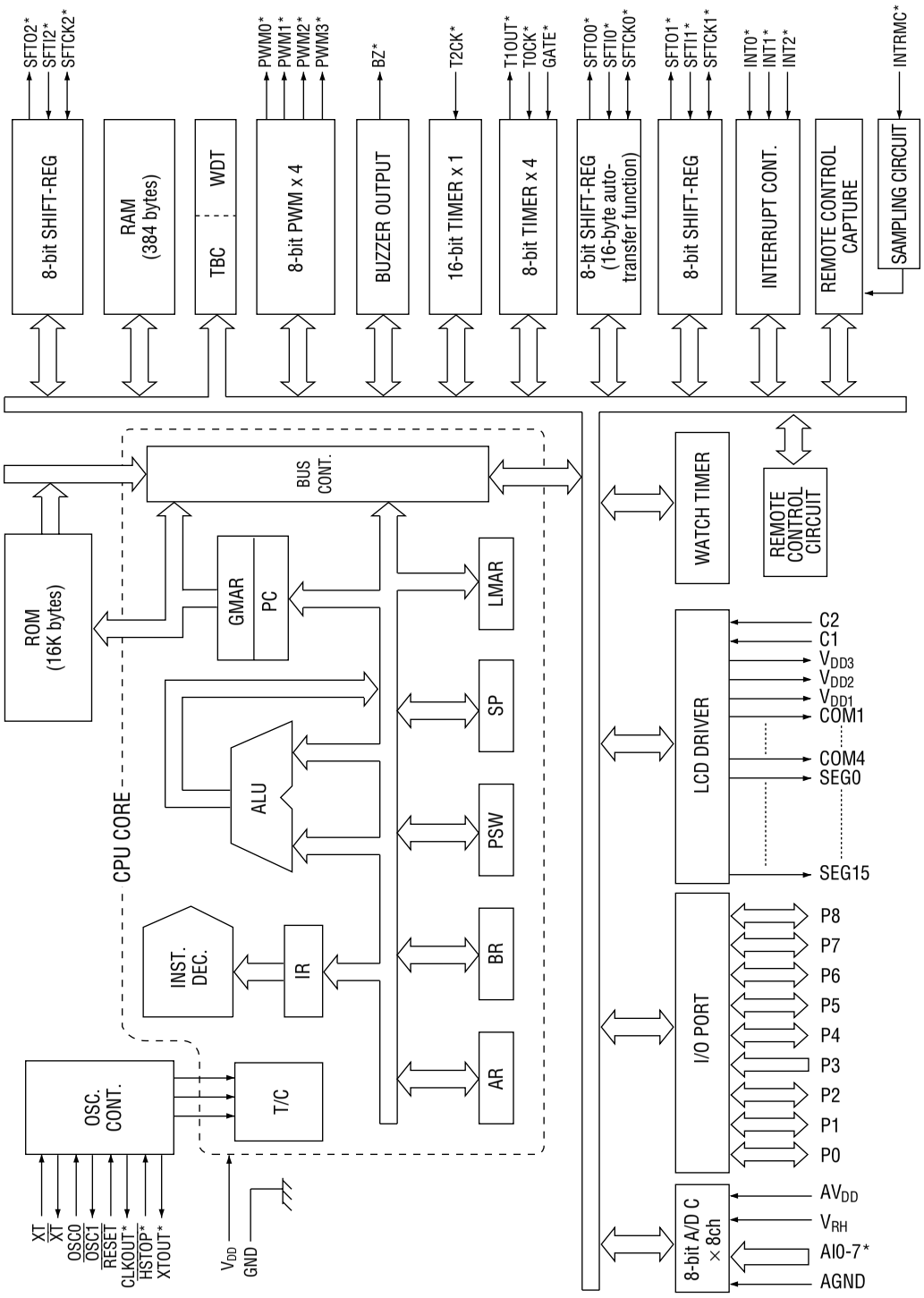
- Operating range
  - Operating voltage : 2.7 to 5.5V
  - Operating temperature : –20 to +70 °C
  - Operating frequency (dual clock)
    - High speed side : 0 to 10MHz (@ V_{DD} = 5V ± 10%)
      0 to 10MHz (@ V_{DD} = 2.7 to 5.5V)
    - Low speed side : 75kHz/32.768kHz (@ V_{DD} = 2.7 to 5.5V)
  - Current consumption (Typ.)
    - High speed side : 5mA (@ 5MHz, V_{DD} = 3V),
      20mA (@ 10MHz, V_{DD}=5V)
    - Low speed side : 45µA (@ 32.768kHz, V_{DD} = 3V)
      4µA (@ V_{DD} = 3V, stop mode)
- Minimum instruction execution time : 400ns (@ 10MHz), 800ns (@ 5MHz)
- CPU core : 8-bit CPU core nX-8/50
- General memory space : Internal 16K-byte program memory
- Local memory space : Internal 384-byte data memory + SFR
- LCD driver : 16 × 4 (1/4, 1/3, and 1/2 duties are selectable with software.)
- I/O port
  - Input-output port : 5 ports × 8 bits, 1 port × 6 bits, 1 port × 5 bits, 1 port × 4 bits
  - Input port : 1 port × 8 bits, 1 port × 1 bit
  - Output port : 1 port × 1 bit
- Timers : 8-bit auto-reload timer × 4 (clock for PWM frequency setting, shift clock for shift register)
  16-bit auto-reload timer × 1
  Watchdog timer × 1
  Watch timer counter × 1
- Counters : Time base counter × 1 (14-bit)
- PWM : 4ch 8-bit duty, frequency 1Hz to 80kHz (@ 10MHz)
- Buzzer output : 1, selectable at 1600Hz, 3200Hz and 6400Hz (@ 10MHz)
- Serial port : Synchronous with auto-transfer function × 1
  Synchronous × 2

- A/D converter : 8 ch, 8 bits
- External interrupts : 3, selectable for rising edge/falling edge/both edges.
- External interrupt for a remote control input (with 8-bit capture)
  : 1, selectable for rising edge/falling edge/both edges, with a sampling circuit for noise prevention.
  With rising edge operating capture and falling edge capture.
- Remote control circuit : Can receive at 75/32.768kHz.
- Interrupt sources : 22
- Package:
  100-pin plastic QFP (QFP100-P-1420-0.65-BK4) (Product name: MSM65355-×××GS-BK4)
  ××× indicates the code number.

- Others

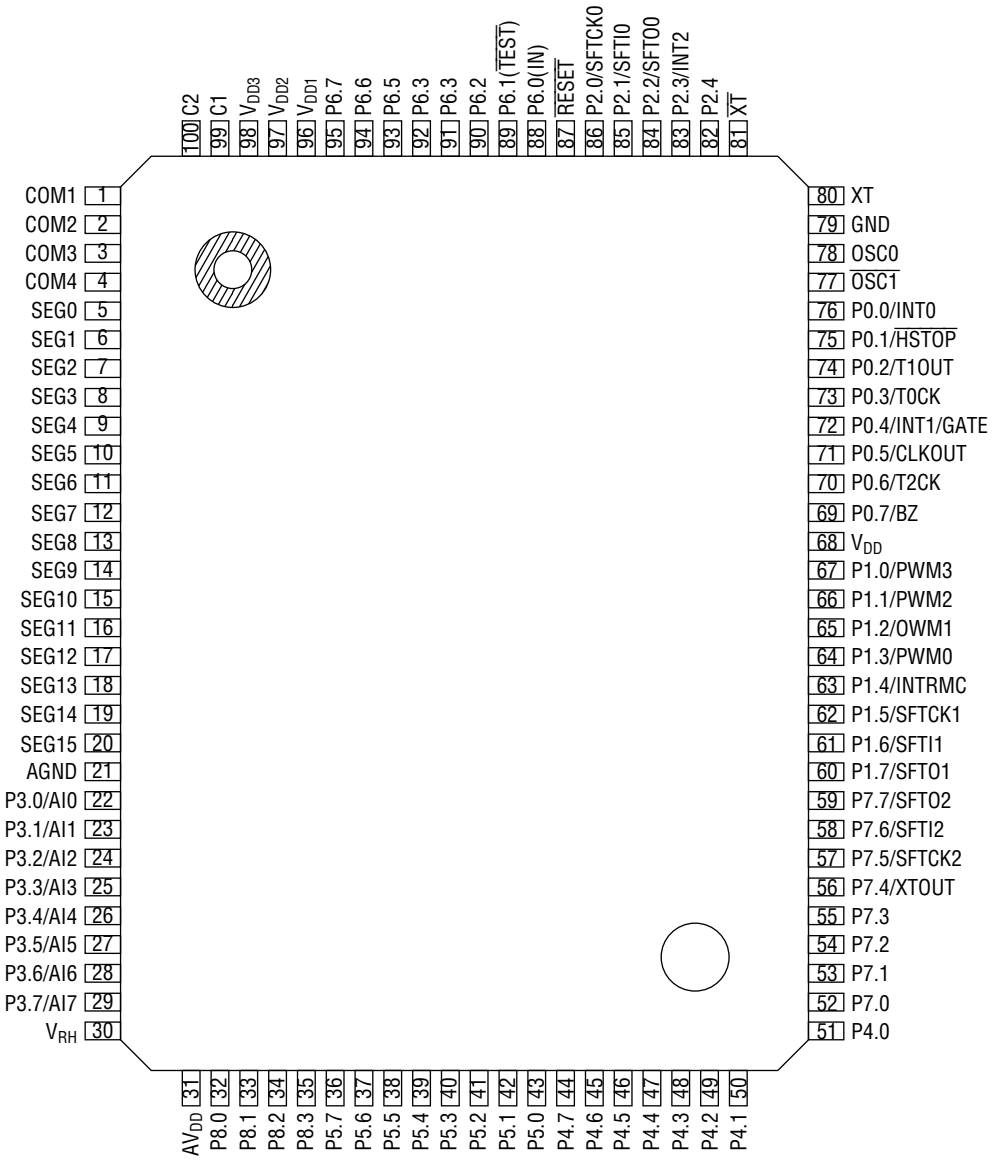
– A 1/2 OSC clock, XT clock or a 4-times XT clock can be selected as the CPU clock.
– The time base counter can be selected to be 1/4n of the CPU clock (n=1 to 8).
– On-chip power-on reset circuit.
– The state during STOP (maintaining of either high impedance or previous state) can be set for each port. (The current consumption of a port in the high impedance setting is less than 1µA.)
– All input-output ports can be set to be pull-up or open. (Ports 0, 1, 2, and 6 can be set to be pull-up or open for each bit.)
– A/D accuracy (±1.5LSB @V_{DD}=4.5 to 5.5V)

BLOCK DIAGRAM



*Secondary functions of each port.

PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic QFP

PIN DESCRIPTIONS

Basic Function

Function	Pin	Symbol	Type	Description
Power	68	V_{DD}	–	Digital power supply (5V)
	79	GND	–	Digital ground
	31	AV_{DD}	–	Analog power supply (5V)
	21	AGND	–	Analog ground
	30	V_{RH}	–	Analog reference voltage
	96	V_{DD1}	–	LCD drive bias output
	97	V_{DD2}	–	LCD drive bias output
	98	V_{DD3}	–	LCD drive bias output
	99	C1	–	Capacitor connecting pins for LCD drive bias generation
	100	C2	–	
Oscillator	78	OSC0	I	Oscillator input pin: connects to a crystal oscillator (or ceramic resonator) or external clock.
	77	$\overline{OSC1}$	O	Oscillator output pin: connects to a crystal oscillator (or ceramic resonator). When an external clock is input to OSC0, leave $\overline{OSC1}$ open.
	80	XT	I	XT-side oscillator input pin: connects a crystal oscillator of 32.768kHz or 75kHz.
	81	$\overline{XT}$	O	XT-side oscillator output pin: connects a crystal oscillator of 32.768kHz or 75kHz.
Control	87	$\overline{RESET}$	I	System reset input: when this pin goes low, the internal state of the chip is initialized and program execution restarts from address 0040H. The input is pulled up to V_{DD} with an internal pull-up resistor.
Ports	76 to 69	P0.0 to P0.7	I/O	8-bit input-output port (port 0): input or output can be selected for each bit by the port 0 direction register (P0DIR). In addition to their input-output port functions, the pins of port 0 have secondary functions: see Secondary Function.
	67 to 60	P1.0 to P1.7	I/O	8-bit input-output port (port 1): input or output can be selected for each bit by the port 1 direction register (P1DIR). In addition to their input or output port functions, the pins of port 1 have secondary functions: see Secondary Function.
	86 to 82	P2.0 to P2.4	I/O	5-bit input-output port (port 2): input or output can be selected for each bit by the port 2 direction register (P2DIR). In addition to their input or output port functions, P2.0 and P2.1 have secondary functions: see Secondary Function.
	22 to 29	P3.0 to P3.7	I	8-bit input port (port3): during A/D conversion, the pins of port 3 function as analog input channels.
	51 to 44	P4.0 to P4.7	I/O	8-bit input-output port (port 4).
	43 to 36	P5.0 to P5.7	I/O	8-bit input-output port (port 5): input or output can be selected for each bit by the port 5 direction register (P5DIR).

Basic Function (Continued)

Function	Pin	Symbol	Type	Description
Ports	88	P6.0	I	1-bit input port (port 6.0)
	89	P6.1 ($\overline{\text{TEST}}$)	O	1-bit output port (port 6.1). After reset, this port is pulled up to 1. During reset, if this port is forcibly cleared to 0, this IC goes into test mode, disabling execution of the use program.
	90 to 95	P6.2 to P6.7	I/O	6-bit input-output port (port6)
	52 to 59	P7.0 to P7.7	I/O	8-bit input-output port (port7): input or output can be selected for each bit by the port 7 direction register (P7DIR). In addition to their input or output port functions, P7.4 to P7.7 pins have secondary functions: see Secondary Function.
	32 to 35	P8.0 to P8.3	I/O	8-bit input-output port (port8): Input or output can be selected for each bit by the port 8 direction register (P8DIR).
LCD Driver	1 to 4	COM1 to COM4	O	LCD common signal output pin
	5 to 20	SEG0 to SEG15	O	LCD segment signal output pin

Secondary Function

Function	Pin	Symbol	Type	Description
External interrupt	76	INT0	I	Secondary function of P0.0: input pin for external interrupt 0. The interrupt can be triggered by the rising edge, falling edge, or both edges.
	72	INT1	I	Secondary function of P0.4: input pin for external interrupt 1. The interrupt can be triggered by the rising edge, falling edge, or both rising and falling edges. Also used as a gate signal input pin for gating the counter of timer 0.
	83	INT2	I	Secondary function of P2.3: input pin for external interrupt 2. The interrupt can be triggered by the rising edge, falling edge, or both rising and falling edges.
Control	75	$\overline{\text{HSTOP}}$	I	Secondary function of P0.1: input pin for hard stop mode. If this pin goes low while the HSTP bit in SBYCON is set to "1", the chip enters hard stop mode. In hard stop mode the clock stops and the CPU and on-chip peripheral functions shut down to conserve power.
Timer 0	73	T0CK	I	Secondary function of P0.3: external clock input pin for timer 0.
Timer 1	74	T1OUT	O	Secondary function of P0.2: This pin outputs a waveform with twice the cycle of the overflow interval of timer 1.
Timer 2	70	T2CK	I	Secondary function of P0.6: external clock input pin for timer 2.
A/D Converter	22 to 29	AI0 to AI7	I	Secondary function of P3.0 to P3.7: These pins function as analog input channel in A/D conversion.
PWM	64	PWM0	O	Secondary function of P1.3: PWM channel 0 output pin.
	65	PWM1	O	Secondary function of P1.2: PWM channel 1 output pin.
	66	PWM2	O	Secondary function of P1.1: PWM channel 2 output pin.
	67	PWM3	O	Secondary function of P1.0: PWM channel 3 output pin.
Clock Output	71	CLKOUT	O	Secondary function of P0.5: clock output pin for 1/2 dividing or 1/4 dividing of OSCCLK or XTCLK.
	56	XTOUT	O	Secondary function of P7.4: XTCLK output pin.
Buzzer Output	69	BZ	O	Secondary function of P0.7: buzzer output pin
Remote Control Input	63	INTRMC	I	Secondary function of P1.4: remote control input pin.

Secondary Function (Continued)

Function	Pin	Symbol	Type	Description
Shift Register	84	SFTO0	O	Secondary function of P2.2: shift register 0 data output pin.
	85	SFTI0	I	Secondary function of P2.1: shift register 0 data input pin.
	86	SFTCK0	I/O	Secondary function of P2.0: shift register 0 synchronizing clock input-output pin. In master mode: clock output In slave mode: clock input
	60	SFTO1	O	Secondary function of P1.7: shift register 1 data output pin.
	61	SFTI1	I	Secondary function of P1.6: shift register 1 data input pin.
	62	SFTCK1	I/O	Secondary function of P1.5: shift register 1 synchronizing clock input-output pin. In master mode: clock output In slave mode: clock input
	59	SFTO2	O	Secondary function of P7.7: shift register 2 data output pin.
	58	SFTI2	I	Secondary function of P7.6: shift register 2 data input pin.
	57	SFTCK2	I/O	Secondary function of P7.5: shift register 2 synchronizing clock input-output pin. In master mode: clock output In slave mode: clock input

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Input Voltage	V_I		–0.3 to V_{DD}+0.3	
Output Voltage	V_O		–0.3 to V_{DD}+0.3	
Power Dissipation	P_D	Ta=25°C, per package	400	mW
		Ta=25°C, per output	50	
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	—	2.7 to 5.5	V
Memory Hold Voltage	V_{DDMH}	f_{OSC}=0 Hz	2.0 to 5.5	
Oscillation Operating Frequency*1	f_{OSC}	—	1 to 10	MHz
	f_{XT}	V_{DD}=2.7 to 5.5	32.768/75	kHz
External Clock Operating Frequency *2	f_{EXTCLK}	—	0 to 10	MHz
Operating Temperature	T_{op}	—	–20 to +70	°C

*1 Depends on specifications for a crystal or ceramic resonator.
*2 External clock cannot be used for XT pin.

ELECTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD}=4.5 to 5.5V)

(GND=0V, Ta=–20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage *1	V_{IH1}	CPUCLK=1MHz	2.4	—	—	V
"H" Input Voltage *2	V_{IH2}	CPUCLK=1MHz	0.75V_{DD}	—	—	
"L" Input Voltage	V_{IL}	CPUCLK=1MHz	—	—	0.8	
"H" Output Voltage 1 *3	V_{OH1}	I_{OH}=–200µA	0.75V_{DD}	—	—	
"H" Output Voltage 2 *4	V_{OH2}	I_{OH}=–400µA	0.75V_{DD}	—	—	
"L" Output Voltage 1 *3	V_{OL1}	I_{OL}=1.6mA	—	—	0.4	
"L" Output Voltage 2 *4	V_{OL2}	I_{OL}=3.2mA	—	—	0.4	
LCD Driving Bias Output Voltage	V_{DD1}	V_{DD}=5V, C_1, C_2, C_3=0.1µF, VSEL=0 (5V mode)	1.2	1.4	—	
	V_{DD2}		2.6	2.8	—	
	V_{DD3}		4.0	4.2	—	
Segment/Common Driving Output Voltage	V_0	I=+10µA	—	—	0.4	
	V_1	V_{DD1}=1.4V, I=±10µA	V_{DD1}–0.4	—	V_{DD1}+0.4	
	V_2	V_{DD2}=2.8V, I=±10µA	V_{DD2}–0.4	—	V_{DD2}+0.4	
	V_3	V_{DD3}=4.2V, I=–10µA	V_{DD3}–0.4	—	—	
Input Leakage Current *5	I_{LI2}	V_I=V_{DD}/0V	—	—	±10	µA
"L" Input Current *6	I_{IL}	V_I=0V, V_{DD}=5V	–40	–200	–400	
Input Capacitance	C_I	f=1MHz, Ta=25°C	—	5	—	pF
Operating Current Consumption V_{DD} = 5V, XT = 32kHz, OSC = 10MHz	I_{DD1}	Stop mode *7	—	15	30	µA
	I_{DD2}	CPUCLK=32kHz, halt mode *8	—	30	60	µA
	I_{DD3}	CPUCLK=32kHz, no load *9	—	80	160	µA
	I_{DD4}	CPUCLK=10MHz, halt mode	—	8	16	mA
	I_{DD5}	CPUCLK=10MHz, no load	—	20	50	mA

*1 Excluding OSC0 and $\overline{RESET}$
*2 OSC0 and $\overline{RESET}$
*3 Excluding P4
*4 P4
*5 Excluding $\overline{RESET}$
*6 $\overline{RESET}$
*7 No load, including hard stop mode
*8 When OSC clock is stopped and LCD is operating
*9 When OSC clock is stopped

DC Characteristics 2 ($2.7V \leq V_{DD} < 4.5V$)

(GND=0V, Ta=–20 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage *1	V_{IH1}	CPUCLK=1MHz	$0.3V_{DD}+0.9$	—	—	V
"H" Input Voltage *2	V_{IH2}	CPUCLK=1MHz	$0.6V_{DD}+0.6$ *10	—	—	
"L" Input Voltage	V_{IL}	CPUCLK=1MHz	—	—	$0.3V_{DD}-0.1$ *11	
"H" Output Voltage 1 *3	V_{OH1}	I_{OH}=–10µA	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 *4	V_{OH2}	I_{OH}=–20µA	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 *3	V_{OL1}	I_{OL}=10µA	—	—	0.1	
"L" Output Voltage 2 *4	V_{OL2}	I_{OL}=20µA	—	—	0.1	
LCD Driving Bias Output Voltage	V_{DD1}	V_{DD}=3V, C_1, C_2, C_3=0.1µF, VSEL=0 (3V mode)	1.2	1.4	—	
	V_{DD2}		2.6	2.8	—	
	V_{DD3}		4.0	4.2	—	
Segment/Common Driving Output Voltage	V_0	I=+10µA	—	—	0.4	
	V_1	V_{DD1}=1.4V, I=±10µA	V_{DD1}–0.4	—	V_{DD1}+0.4	
	V_2	V_{DD2}=2.8V, I=±10µA	V_{DD2}–0.4	—	V_{DD2}+0.4	
	V_3	V_{DD3}=4.2V, I=–10µA	V_{DD3}–0.4	—	—	
Input Leakage Current 1 *5	I_{LI2}	$V_I=V_{DD}$/0V	—	—	±10	µA
"L" Input Current *6	I_{IL}	V_I=0V, V_{DD}=3V	–40	–125	–250	
Input Capacitance	C_I	f=1MHz, Ta=25°C	—	5	—	pF
Operating Current Consumption V_{DD} = 3V, XT = 32kHz, OSC = 5MHz	I_{DD1}	Stop mode *7	—	4	8	µA
	I_{DD2}	CPUCLK=32kHz, halt mode *8	—	15	30	µA
	I_{DD3}	CPUCLK=32kHz, no load *9	—	45	90	µA
	I_{DD4}	CPUCLK=5MHz, halt mode	—	1.5	3	mA
	I_{DD5}	CPUCLK=5MHz, no load	—	5	16	mA

*1 Excluding OSC0 and $\overline{\text{RESET}}$
*2 OSC0 and $\overline{\text{RESET}}$
*3 Excluding P4
*4 P4
*5 Excluding $\overline{\text{RESET}}$
*6 $\overline{\text{RESET}}$
*7 No load, including hard stop mode
*8 When OSC clock is stopped and LCD is operated
*9 When OSC clock is stopped
*10 More than 3.375V
*11 Less than 0.8V

AC Characteristics

• CPU control

(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–20 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{RESET}}$ Pulse Width	t_{RESW}	—	20	—	ns

• Peripheral control 1

(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–20 to +70°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			2.7V ≤ V_{DD} < 4.5V	200	—	
	Clock "L" Pulse Wedth	t_{CLW}	—	0.45t_C	0.55t_C	
EXI	External Interrupt Pulse Width	t_{EXIW}	—	4CPUCLK *1	—	
T0	External Clock Pulse Width	t_{T0CW}		4CPUCLK *1	—	
	GATE Pulse Width	t_{T0GW}		1 t_{T0CLK} *2	—	
T2	External Clock Pulse Width	t_{T2CW}		4CPUCLK *1	—	

*1 CPUCLK : Supply clock for CPU selected by SBYCON
*2 t_{T0CLK} : Timer 0 count clock cycle selected by T0CON

• Peripheral control 2

(V_{DD}=2.7 to 5.5V, GND=0V, Ta=–20 to +70°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t_C	V_{DD}=4.5 to 5.5V	100	—	ns
			2.7V ≤ V_{DD} < 4.5V	200	—	
SFT0-2	SFTCK Cycle	t_{SFC0-2}	C_L=100pF	8CPUCLK*	—	
	SFTCK "L" Pulse Width	$t_{SFCLW0-2}$		4CPUCLK–20*	—	
	SFTCK "H" Pulse Width	$t_{SFCHW0-2}$		4CPUCLK–20*	—	
	SFTO Setup Time	$t_{SFOS0-2}$		$t_{SFCLW0-2}$–100	—	
	SFTO Hold Time	$t_{SFOH0-2}$		$t_{SFCHW0-2}$–100	—	
	SFTI Setup Time	$t_{SFIS0-2}$		100	—	
	SFTI Hold Time	$t_{SFIH0-2}$		100	—	

* CPUCLK : Supply clock for CPU selected by SBYCON

- **A/D Converter Characteristics 1**

(V_{DD}=AV_{DD}=V_{RH}=4.5 to 5.5V, GND=AGND=0V, Ta=–20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	See the recommended circuit. Analog input source impedance $R_I \leq 5k\Omega$	—	8	—	bit
Linearity Error	E_L		—	—	+1.5 –1.5	LSB
Differential Linearity Error	E_D		—	—	±0.5	LSB
Zero Scale Error	E_{ZS}		—	—	+1.5	LSB
Full Scale Error	E_{FS}		—	—	–1.5	LSB
Crosstalk	E_{CT}	See the measuring circuit.	—	—	±0.5	LSB
Conversion Time *	t_{CONV}	f_{OSC}=10 MHz	—	16	—	µs/CH

* The conversion just after setting GO bit to "1" : 14.8µs/CH

- **A/D Converter Characteristics 2**

(V_{DD}=AV_{DD}=V_{RH}, 2.7V ≤ V_{DD} < 4.5V, GND=AGND=V_{RL}=0V, Ta=–20 to +75°C)

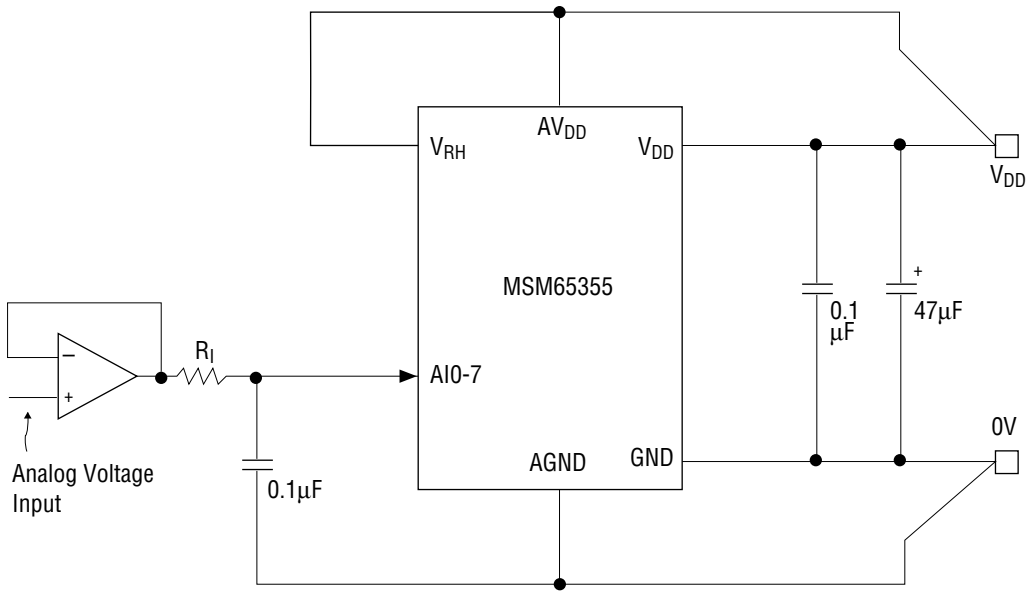
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	See the recommended circuit. Analog input source impedance $R_I \leq 5k\Omega$	—	8	—	bit
Linearity	E_L		—	—	+2 –2	LSB
Differential Linearity Error	E_D		—	—	±1	LSB
Zero Scale Error	E_{ZS}		—	—	+2	LSB
Full Scale Error	E_{FS}		—	—	–2	LSB
Crosstalk	E_{CT}	See the measuring circuit.	—	—	±1	LSB
Conversion Time *	t_{CONV}	f_{OSC}=5 MHz	—	32	—	µs/CH

* The conversion just after setting GO bit to "1" : 29.6µs/CH

Definition of Terms

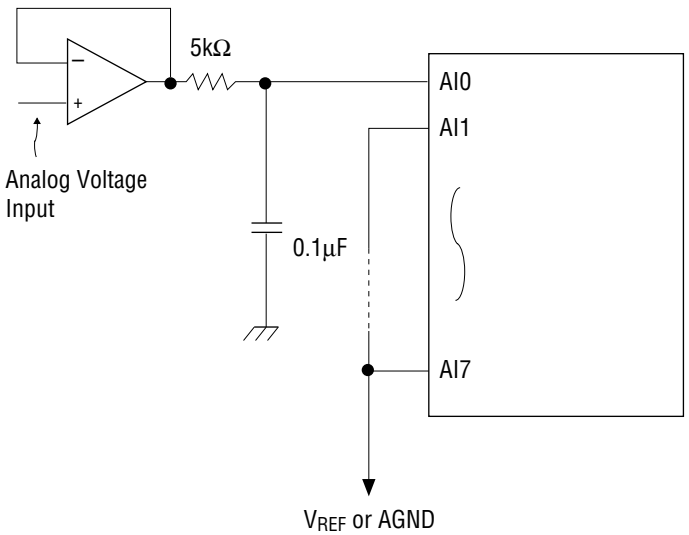
Resolution	Recognizable minimum input analog value. This can be resolved into 2^8=256, that is, $V_{RH} \div 256$ in 8 bits.
Linearity Error	Deviation between ideal conversion characteristics as an 8-bit A/D converter and actual conversion characteristics. (Quantization error not included.) Ideal conversion characteristics means a step, where voltage is divided between V_{RH} and AGND into 256.
Differential Linearity Error	Shows the smoothness of conversion characteristics. 1LSB= $V_{RH} \div 256$ is ideal for analog input voltage width corresponding to change per 1 bit of digital output. The differential linearity error is the deviation between this ideal bit size and a bit size at arbitrary point in conversion range.
Zero Scale Error	Deviation between ideal conversion characteristics of transfer point for digital outputs "000H" to "001H" and actual conversion characteristics.
Full Scale Error	Deviation between ideal conversion characteristics of transfer point for digital outputs "0FEH" to "0FFH" and actual conversion characteristics.

Recommended circuit



R_I (Analog input source impedance) ≤ 5kΩ

Crosstalk measuring circuit

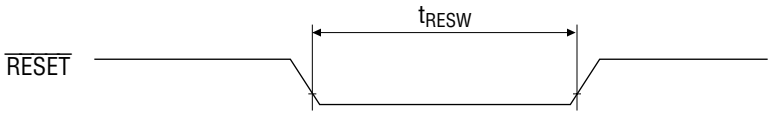


Crosstalk is defined as the difference of A/D conversion result between supplying the same voltage to AI0 to AI7 and supplying voltage shown in this left diagram.

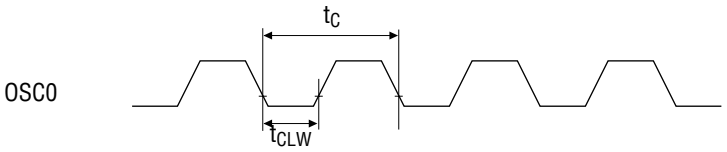
- **Timing diagram**

CPU control

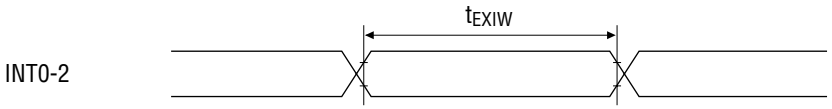
1) $\overline{\text{RESET}}$ pulse width



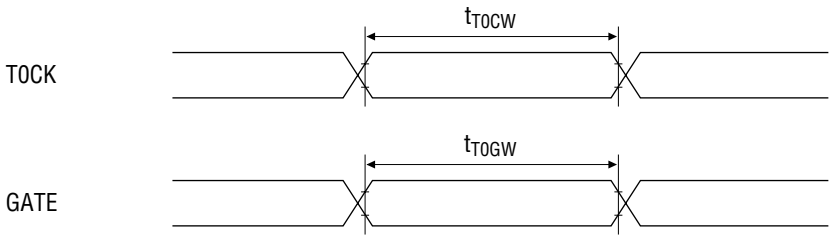
Peripheral control 1



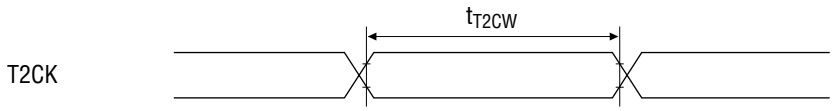
1) EXI pulse width



2) T0

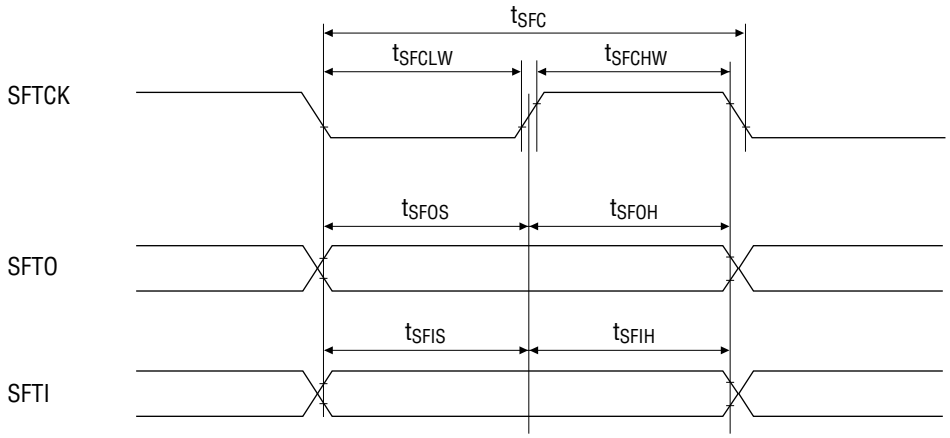


3) T2



Peripheral control 2

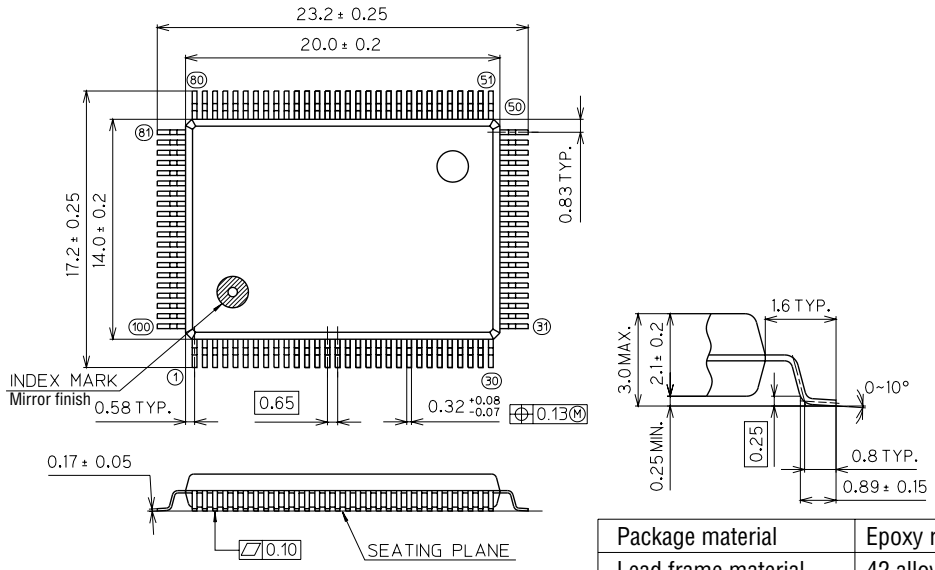
1) SFT0-2



PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-BK4



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.54 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).