



# Microprocessor Supervisory Circuits

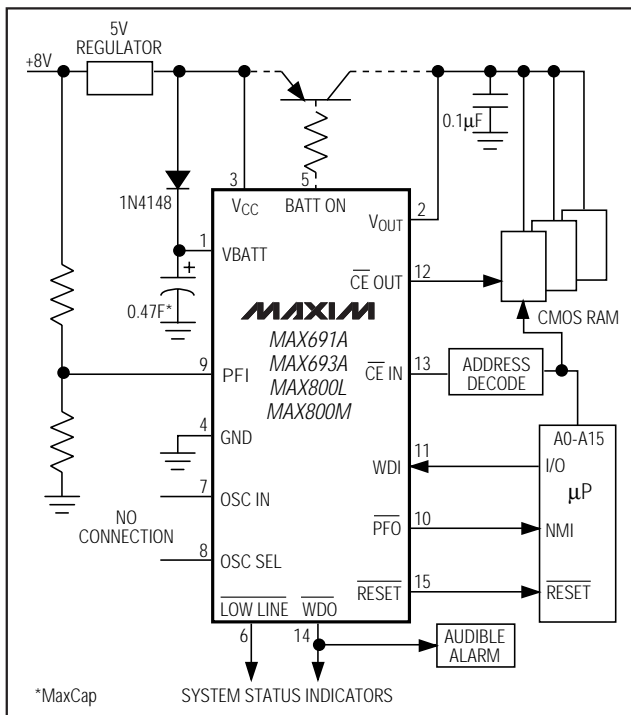
## General Description

The MAX691A/MAX693A/MAX800L/MAX800M microprocessor ( $\mu$ P) supervisory circuits are pin-compatible upgrades to the MAX691, MAX693, and MAX695. They improve performance with 30 $\mu$ A supply current, 200ms typ reset active delay on power-up, and 6ns chip-enable propagation delay. Features include write protection of CMOS RAM or EEPROM, separate watchdog outputs, backup-battery switchover, and a  $\overline{\text{RESET}}$  output that is valid with  $V_{CC}$  down to 1V. The MAX691A/MAX800L have a 4.65V typical reset-threshold voltage, and the MAX693A/MAX800M's reset threshold is 4.4V typical. The MAX800L/MAX800M guarantee power-fail accuracies to  $\pm 2\%$ .

## Applications

- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical  $\mu$ P Power Monitoring

## Typical Operating Circuit



SuperCap is a registered trademark of Baknor Industries. MaxCap is a registered trademark of The Carborundum Corp.

## Features

- ◆ 200ms Power-OK/Reset Timeout Period
- ◆ 1 $\mu$ A Standby Current, 30 $\mu$ A Operating Current
- ◆ On-Board Gating of Chip-Enable Signals, 10ns Max Delay
- ◆ MaxCap™ or SuperCap™ Compatible
- ◆ Guaranteed  $\overline{\text{RESET}}$  Assertion to  $V_{CC} = +1V$
- ◆ Voltage Monitor for Power-Fail or Low-Battery Warning
- ◆ Power-Fail Accuracy Guaranteed to  $\pm 2\%$  (MAX800L/M)
- ◆ Available in 16-Pin Narrow SO and Plastic DIP Packages

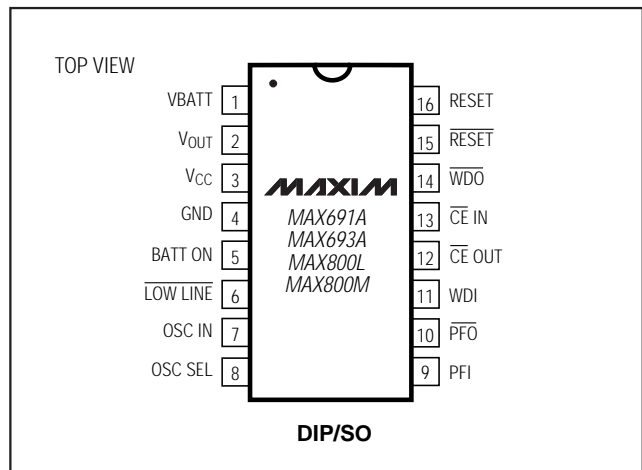
## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX691ACPE	0°C to +70°C	16 Plastic DIP
MAX691ACSE	0°C to +70°C	16 Narrow SO
MAX691ACWE	0°C to +70°C	16 Wide SO
MAX691AC/D	0°C to +70°C	Dice*
MAX691AEPE	-40°C to +85°C	16 Plastic DIP
MAX691AESE	-40°C to +85°C	16 Narrow SO
MAX691AEWE	-40°C to +85°C	16 Wide SO
MAX691AEJE	-40°C to +85°C	16 CERDIP
MAX691AMJE	-55°C to +125°C	16 CERDIP

Ordering Information continued on last page.

\* Dice are specified at  $T_A = +25^\circ\text{C}$ , DC parameters only.

## Pin Configuration



MAX691A/MAX693A/MAX800L/MAX800M



# Microprocessor Supervisory Circuits

## ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

V <sub>CC</sub> .....	-0.3V to +6V
VBATT .....	-0.3V to +6V
All Other Inputs .....	-0.3V to (V <sub>OUT</sub> + 0.3V)

Input Current

V <sub>CC</sub> Peak .....	1.0A
V <sub>CC</sub> Continuous .....	250mA
VBATT Peak .....	250mA
VBATT Continuous .....	25mA
GND, BATT ON .....	100mA
All Other Outputs .....	25mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

Plastic DIP (derate 10.53mW/°C above +70°C) .....	842mW
Narrow SO (derate 8.70mW/°C above +70°C) .....	696mW
Wide SO (derate 9.52mW/°C above +70°C) .....	762mW
CERDIP (derate 10.00mW/°C above +70°C) .....	800mW

Operating Temperature Ranges

MAX69_AC_/MAX800_C_ .....	0°C to +70°C
MAX69_AE_/MAX800_E_ .....	-40°C to +85°C
MAX69_AMJE .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +160°C
Lead Temperature (soldering, 10sec) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(MAX691A, MAX800L: V<sub>CC</sub> = +4.75V to +5.5V, MAX693A, MAX800M: V<sub>CC</sub> = +4.5V to +5.5V, VBATT = 2.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V <sub>CC</sub> , VBATT (Note 1)			0		5.5	V
V <sub>OUT</sub> Output	V <sub>CC</sub> = 4.5V	I <sub>OUT</sub> = 25mA		V <sub>CC</sub> - 0.02	V <sub>CC</sub> - 0.05	V
		I <sub>OUT</sub> = 250mA	MAX69_AC	V <sub>CC</sub> - 0.2	V <sub>CC</sub> - 0.3	
			MAX69_AE, MAX800_C/E	V <sub>CC</sub> - 0.2	V <sub>CC</sub> - 0.35	
			MAX69_A/M		V <sub>CC</sub> - 0.40	
I <sub>OUT</sub> = 210mA	MAX69_AC/AE, MAX800_C/E	V <sub>CC</sub> - 0.17	V <sub>CC</sub> - 0.3V			
V <sub>CC</sub> -to-V <sub>OUT</sub> On-Resistance	V <sub>CC</sub> = 4.5V	MAX69_AC, MAX800_C		0.8	1.2	Ω
		MAX69_AE, MAX800_E		0.8	1.4	
		MAX69_A/M		0.8	1.6	
V <sub>OUT</sub> in Battery-Backup Mode	VBATT = 4.5V, I <sub>OUT</sub> = 20mA		VBATT - 0.3		V	
	VBATT = 2.8V, I <sub>OUT</sub> = 10mA		VBATT - 0.25			
	VBATT = 2.0V, I <sub>OUT</sub> = 5mA		VBATT - 0.15			
VBATT-to-V <sub>OUT</sub> On-Resistance	VBATT = 4.5V				15	Ω
	VBATT = 2.8V				25	
	VBATT = 2.0V				30	
Supply Current in Normal Operating Mode (Excludes I <sub>OUT</sub> )	V <sub>CC</sub> > VBATT - 1V			30	100	μA
Supply Current in Battery-Backup Mode (Excludes I <sub>OUT</sub> ) (Note 2)	V <sub>CC</sub> < VBATT - 1.2V VBATT = 2.8V	T <sub>A</sub> = +25°C		0.04	1	μA
		T <sub>A</sub> = T <sub>MIN</sub> + T <sub>MIN</sub>			5	
VBATT Standby Current (Note 3)	VBATT + 0.2V ≤ V <sub>CC</sub>	T <sub>A</sub> = +25°C	-0.1		0.02	μA
		T <sub>A</sub> = T <sub>MIN</sub> + T <sub>MIN</sub>	-1.0		0.02	
Battery Switchover Threshold	Power-up				VBATT + 0.3	V
	Power-down				VBATT - 0.3	

# Microprocessor Supervisory Circuits

## ELECTRICAL CHARACTERISTICS (continued)

(MAX691A, MAX800L:  $V_{CC} = +4.75V$  to  $+5.5V$ , MAX693A, MAX800M:  $V_{CC} = +4.5V$  to  $+5.5V$ ,  $V_{BATT} = 2.8V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Switchover Hysteresis			60		mV
BATT ON Output Low Voltage	$I_{SINK} = 3.2mA$		0.1	0.4	V
	$I_{SINK} = 25mA$		0.7	1.5	
BATT ON Output Short-Circuit Current	Sink current		60		mA
	Source current	1	15	100	$\mu A$
<b>RESET AND WATCHDOG TIMER</b>					
Reset Threshold Voltage	MAX691A, MAX800L	4.50	4.65	4.75	V
	MAX693A, MAX800M	4.25	4.40	4.50	
	MAX800L, $T_A = +25^\circ C$ , $V_{CC}$ falling	4.55		4.70	
	MAX800M, $T_A = +25^\circ C$ , $V_{CC}$ falling	4.30		4.45	
Reset Threshold Hysteresis			15		mV
$V_{CC}$ to RESET Delay	Power-down		80		$\mu s$
$\overline{LOW\ LINE}$ -to- $\overline{RESET}$ Delay			800		ns
Reset Active Timeout Period, Internal Oscillator	Power-up	140	200	280	ms
Reset Active Timeout Period, External Clock (Note 4)	Power-up		2048		Clock Cycles
Watchdog Timeout Period, Internal Oscillator	Long period	1.0	1.6	2.25	sec
	Short period	70	100	140	ms
Watchdog Timeout Period, External Clock (Note 4)	Long period		4096		Clock Cycles
	Short period		1024		
Minimum Watchdog Input Pulse Width	$V_{IL} = 0.8V$ , $V_{IH} = 0.75 \times V_{CC}$	100			ns
$\overline{RESET}$ Output Voltage	$I_{SINK} = 50\mu A$ , $V_{CC} = 1V$ , $V_{BATT} = 0V$ , $V_{CC}$ falling		0.004	0.3	V
	$I_{SINK} = 3.2mA$ , $V_{CC} = 4.25V$		0.1	0.4	
	$I_{SOURCE} = 1.6mA$ , $V_{CC} = 5V$	3.5			
$\overline{RESET}$ Output Short-Circuit Current	Output source current		7	20	mA
RESET Output Voltage Low (Note 5)	$I_{SINK} = 3.2mA$	0.1	0.4		V
$\overline{LOW\ LINE}$ Output Voltage	$I_{SINK} = 3.2mA$ , $V_{CC} = 4.25V$			0.4	V
	$I_{SOURCE} = 1\mu A$ , $V_{CC} = 5V$	3.5			
$\overline{LOW\ LINE}$ Output Short-Circuit Current	Output source current	1	15	100	$\mu A$
$\overline{WDO}$ Output Voltage	$I_{SINK} = 3.2mA$			0.4	V
	$I_{SOURCE} = 500\mu A$ , $V_{CC} = 5V$	3.5			
$\overline{WDO}$ Output Short-Circuit Current	Output source current		3	10	mA
WDI Threshold Voltage (Note 6)	$V_{IH}$	$0.75 \times V_{CC}$			V
	$V_{IL}$			0.8	
WDI Input Current	WDI = 0V	-50	-10		$\mu A$
	WDI = $V_{OUT}$		20	50	

MAX691A/MAX693A/MAX800L/MAX800M

# Microprocessor Supervisory Circuits

MAX691A/MAX693A/MAX800L/MAX800M

## ELECTRICAL CHARACTERISTICS (continued)

(MAX691A, MAX800L:  $V_{CC} = +4.75V$  to  $+5.5V$ , MAX693A, MAX800M:  $V_{CC} = +4.5V$  to  $+5.5V$ ,  $V_{BATT} = 2.8V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER-FAIL COMPARATOR</b>					
PFI Input Threshold	MAX69_AC/AE/AM, $V_{CC} = 5V$	1.2	1.25	1.3	V
	MAX800_C/E, $V_{CC} = 5V$	1.225	1.25	1.275	
PFI Leakage Current			$\pm 0.01$	$\pm 25$	nA
$\overline{PFO}$ Output Voltage	$I_{SINK} = 3.2mA$			0.4	V
	$I_{SOURCE} = 1\mu A$ , $V_{CC} = 5V$	3.5			
$\overline{PFO}$ Output Short-Circuit Current	Output source current	1	15	100	$\mu A$
PFI-to-PFO Delay	$V_{IN} = -20mV$ , $V_{OD} = 15mV$		25		$\mu s$
	$V_{IN} = 20mV$ , $V_{OD} = 15mV$		60		
<b>CHIP-ENABLE GATING</b>					
$\overline{CE}$ IN Leakage Current	Disable mode		$\pm 0.005$	$\pm 1$	$\mu A$
$\overline{CE}$ IN-to- $\overline{CE}$ OUT Resistance (Note 7)	Enable mode		75	150	$\Omega$
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)	Disable mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN-to- $\overline{CE}$ OUT Propagation Delay (Note 8)	50 $\Omega$ source impedance driver, $C_{LOAD} = 50pF$		6	10	ns
$\overline{CE}$ OUT Output Voltage High (Reset Active)	$V_{CC} = 5V$ , $I_{OUT} = -100\mu A$	3.5			V
	$V_{CC} = 0V$ , $V_{BATT} = 2.8V$ , $I_{OUT} = 1\mu A$	2.7			
RESET-to- $\overline{CE}$ OUT Delay	Power-down		12		$\mu s$
<b>INTERNAL OSCILLATOR</b>					
OSC IN Leakage Current	OSC SEL = 0V		0.10	$\pm 5$	$\mu A$
OSC IN Input Pull-Up Current	OSC SEL = $V_{OUT}$ or floating, OSC IN = 0V		10	100	$\mu A$
OSC SEL Input Pull-Up Current	OSC SEL = 0V		10	100	$\mu A$
OSC IN Frequency Range	OSC SEL = 0V		50		kHz
OSC IN External Oscillator Threshold Voltage	$V_{IH}$	$V_{OUT} - 0.3$	$V_{OUT} - 0.6$		V
	$V_{IL}$		3.65	2.00	
OSC IN Frequency with External Capacitor	OSC SEL = 0V, $C_{OSC} = 47pF$		100		kHz

**Note 1:** Either  $V_{CC}$  or  $V_{BATT}$  can go to 0V, if the other is greater than 2.0V.

**Note 2:** The supply current drawn by the MAX691A/MAX800L/MAX800M from the battery excluding  $I_{OUT}$  typically goes to 10 $\mu A$  when  $(V_{BATT} - 1V) < V_{CC} < V_{BATT}$ . In most applications, this is a brief period as  $V_{CC}$  falls through this region.

**Note 3:** "+" = battery-discharging current, "-" = battery-charging current.

**Note 4:** Although presented as typical values, the number of clock cycles for the reset and watchdog timeout periods are fixed and do not vary with process or temperature.

**Note 5:** RESET is an open-drain output and sinks current only.

**Note 6:** WDI is internally connected to a voltage divider between  $V_{OUT}$  and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

**Note 7:** The chip-enable resistance is tested with  $V_{CC} = +4.75V$  for the MAX691A/MAX800L and  $V_{CC} = +4.5V$  for the MAX693A/MAX800M.  $\overline{CE}$  IN =  $\overline{CE}$  OUT =  $V_{CC} / 2$ .

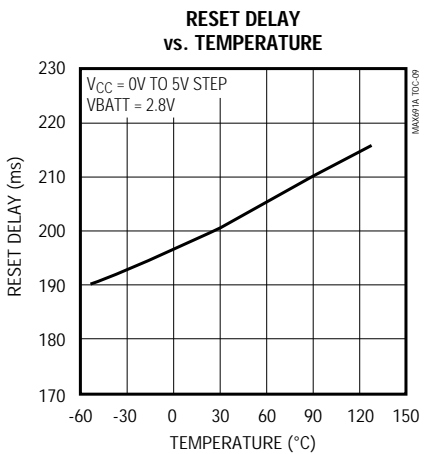
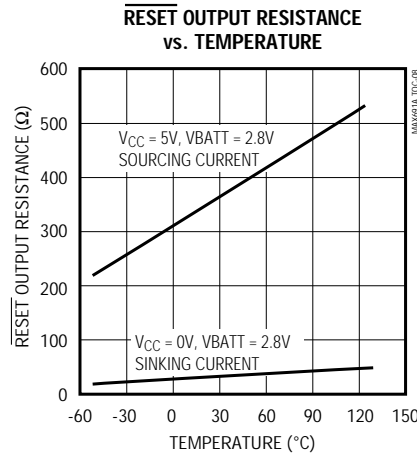
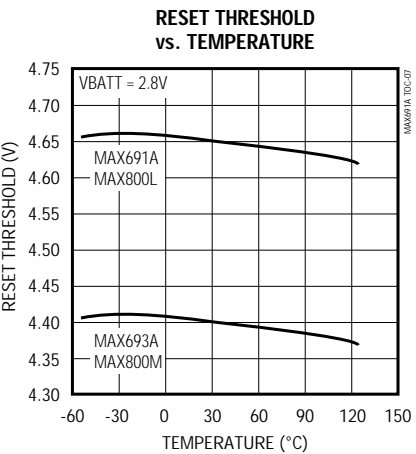
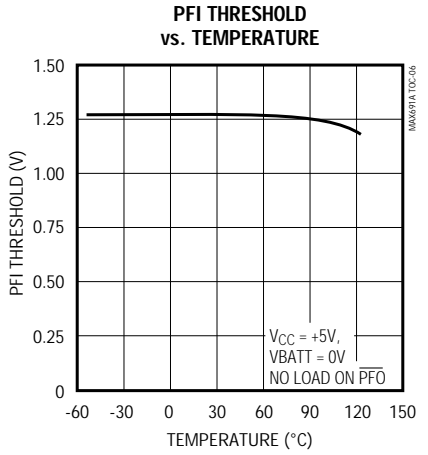
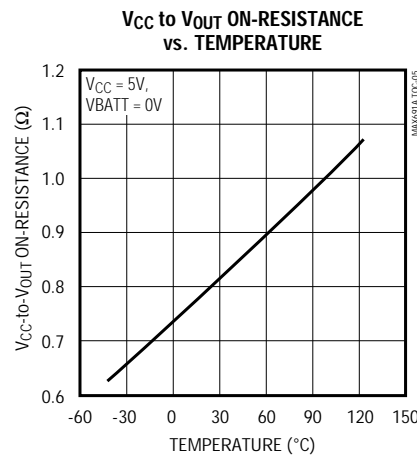
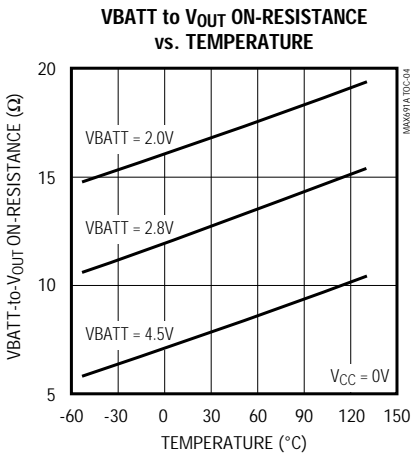
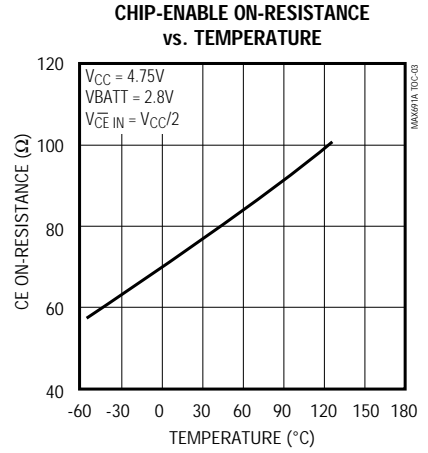
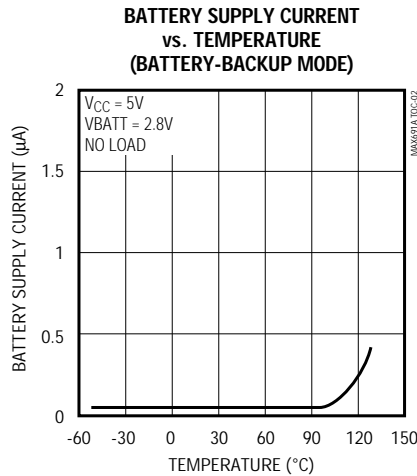
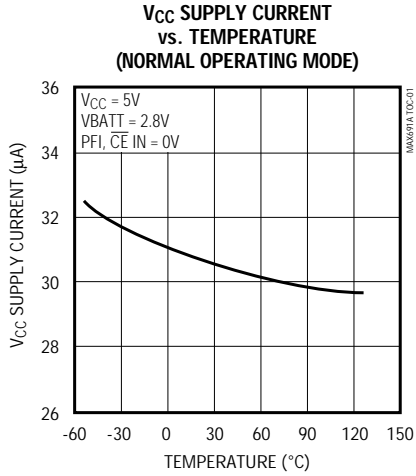
**Note 8:** The chip-enable propagation delay is measured from the 50% point at  $\overline{CE}$  IN to the 50% point at  $\overline{CE}$  OUT.

# Microprocessor Supervisory Circuits

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

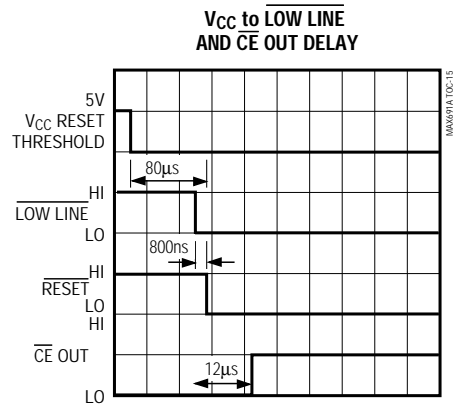
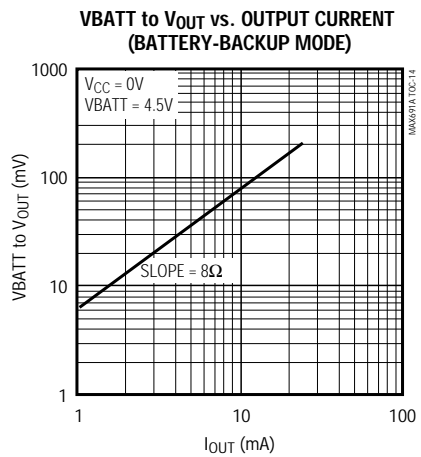
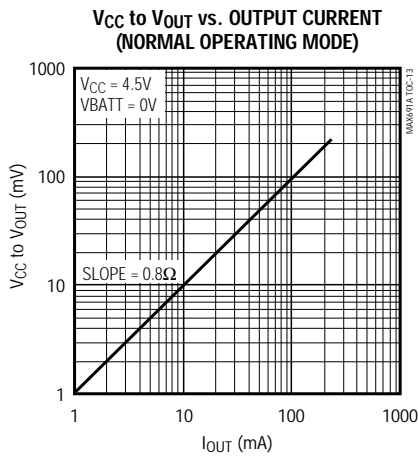
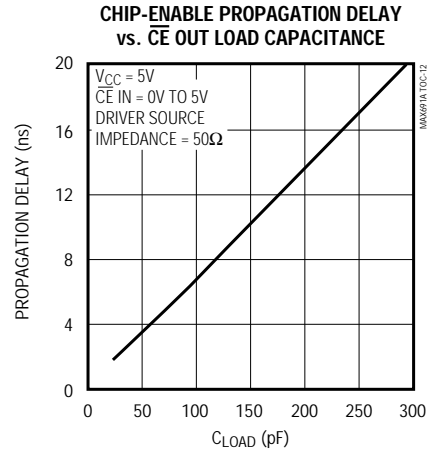
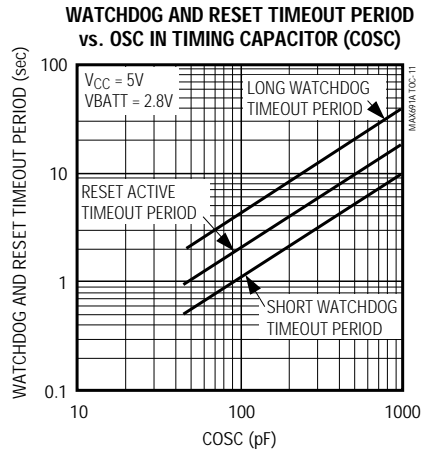
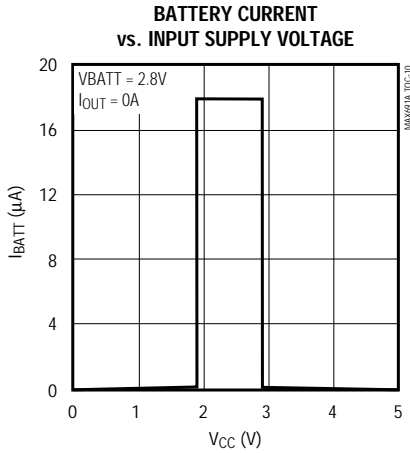
MAX6911A/MAX693A/MAX693A/MAX800L/MAX800M



# Microprocessor Supervisory Circuits

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# Microprocessor Supervisory Circuits

## Pin Description

PIN	NAME	FUNCTION
1	VBATT	Battery-Backup Input. Connect to external battery or capacitor and charging circuit. If backup battery is not used, connect to GND.
2	V <sub>OUT</sub>	Output Supply Voltage. When V <sub>CC</sub> is greater than VBATT and above the reset threshold, V <sub>OUT</sub> connects to V <sub>CC</sub> . When V <sub>CC</sub> falls below VBATT and is below the reset threshold, V <sub>OUT</sub> connects to VBATT. Connect a 0.1μF capacitor from V <sub>OUT</sub> to GND. Connect V <sub>OUT</sub> to V <sub>CC</sub> if no backup battery is used.
3	V <sub>CC</sub>	Input Supply Voltage, 5V input.
4	GND	Ground. 0V reference for all signals.
5	BATT ON	Battery On Output. When V <sub>OUT</sub> switches to VBATT, BATT ON goes high. When V <sub>OUT</sub> switches to V <sub>CC</sub> , BATT ON goes low. Connect the base of a PNP through a current-limiting resistor to BATT ON for V <sub>OUT</sub> current requirements greater than 250mA.
6	LOW LINE	LOW LINE output goes low when V <sub>CC</sub> falls below the reset threshold. It returns high as soon as V <sub>CC</sub> rises above the reset threshold.
7	OSC IN	External Oscillator Input. When OSC SEL is unconnected or driven high, a 10μA pull-up connects from V <sub>OUT</sub> to OSC IN, the internal oscillator sets the reset and watchdog timeout periods, and OSC IN selects between fast and slow watchdog timeout periods. When OSC SEL is driven low, the reset and watchdog timeout periods may be set either by a capacitor from OSC IN to ground or by an external clock at OSC IN (Figure 3).
8	OSC SEL	Oscillator Select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. When OSC SEL is low, the external oscillator input (OSC IN) is enabled (Table 1). OSC SEL has a 10μA internal pull-up.
9	PFI	Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, PFO goes low. When PFI is not used, connect PFI to GND or V <sub>OUT</sub> .
10	PFO	Power-Fail Output. This is the output of the power-fail comparator. PFO goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.
11	WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, WDO goes low and reset is asserted for the reset timeout period. WDO remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V <sub>OUT</sub> and GND, which sets it to mid-supply when left unconnected.
12	CE OUT	Chip-Enable Output. CE OUT goes low only when CE IN is low and V <sub>CC</sub> is above the reset threshold. If CE IN is low when reset is asserted, CE OUT will stay low for 15μs or until CE IN goes high, whichever occurs first.
13	CE IN	Chip-Enable Input. The input to chip-enable gating circuit. If CE IN is not used, connect CE IN to GND or V <sub>OUT</sub> .
14	WDO	Watchdog Output. If WDI remains high or low longer than the watchdog timeout period, WDO goes low and reset is asserted for the reset timeout period. WDO returns high on the next transition at WDI. WDO remains high if WDI is unconnected.
15	RESET	RESET Output goes low whenever V <sub>CC</sub> falls below the reset threshold. RESET will remain low typically for 200ms after V <sub>CC</sub> crosses the reset threshold on power-up.
16	RESET	RESET is an active-high output. It is open drain, and the inverse of RESET.

## Detailed Description

### RESET and RESET Outputs

The MAX691A/MAX693A/MAX800L/MAX800M's RESET and RESET outputs ensure that the μP (with reset inputs asserted either high or low) powers up in a known state, and prevents code-execution errors during power-down or brownout conditions.

The RESET output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deasserted, RESET sources 1.6mA at typically V<sub>OUT</sub> - 0.5V. RESET output is open drain, active high, and typically sinks 3.2mA with a saturation voltage of 0.1V. When no backup battery is used, RESET output is

guaranteed to be valid down to V<sub>CC</sub> = 1V, and an external 10kΩ pull-down resistor on RESET insures that it will be valid with V<sub>CC</sub> down to GND (Figure 1). As V<sub>CC</sub> goes below 1V, the gate drive to the RESET output switch reduces accordingly, increasing the R<sub>DS(ON)</sub> and the saturation voltage. The 10kΩ pull-down resistor insures the parallel combination of switch plus resistor is around 10kΩ and the output saturation voltage is below 0.4V while sinking 40μA. When using a 10kΩ external pull-down resistor, the high state for RESET output with V<sub>CC</sub> = 4.75V will be 4.5V typical. For battery voltages ≥ 2V connected to VBATT, RESET and RESET remain valid for V<sub>CC</sub> from 0V to 5.5V.

MAX691A/MAX693A/MAX800L/MAX800M

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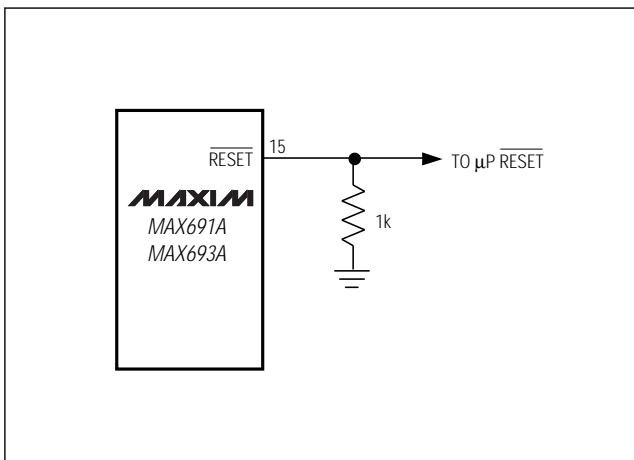


Figure 1. Adding an external pull-down resistor ensures  $\overline{\text{RESET}}$  is valid with  $V_{\text{CC}}$  down to GND.

$\overline{\text{RESET}}$  and  $\overline{\text{RESET}}$  are asserted when  $V_{\text{CC}}$  falls below the reset threshold (4.65V for the MAX691A/MAX800L, 4.4V for the MAX693A/MAX800M) and remain asserted for 200ms typ after  $V_{\text{CC}}$  rises above the reset threshold on power-up (Figure 5). The devices' battery-switchover comparator does not affect reset assertion. However, both reset outputs are asserted in battery-backup mode since  $V_{\text{CC}}$  must be below the reset threshold to enter this mode.

### Watchdog Function

The watchdog monitors  $\mu\text{P}$  activity via the Watchdog Input (WDI). If the  $\mu\text{P}$  becomes inactive,  $\overline{\text{RESET}}$  and  $\overline{\text{RESET}}$  are asserted. To use the watchdog function, connect WDI to a bus line or  $\mu\text{P}$  I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6sec nominal),  $\overline{\text{WDO}}$ ,  $\overline{\text{RESET}}$ , and  $\overline{\text{RESET}}$  are asserted (see *RESET and RESET Outputs* section, and the *Watchdog Output* discussion on this page).

### Watchdog Input

A change of state (high to low, low to high, or a minimum 100ns pulse) at the WDI during the watchdog period resets the watchdog timer. The watchdog default timeout is 1.6sec.

To disable the watchdog function, leave WDI floating. An internal resistor network (100k $\Omega$  equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When  $V_{\text{CC}}$  is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

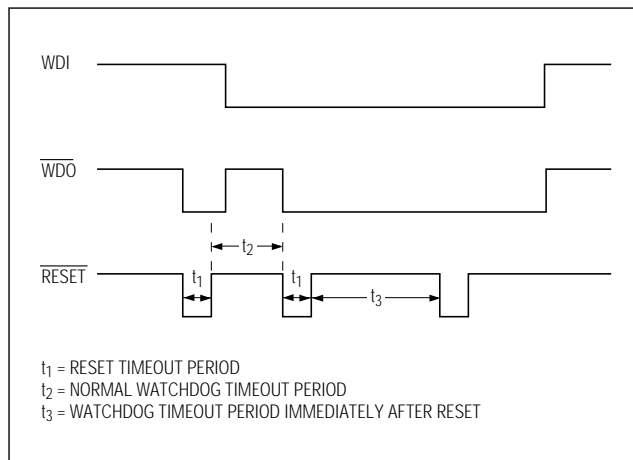


Figure 2. Watchdog Timeout Period and Reset Active Time

### Watchdog Output

The Watchdog Output ( $\overline{\text{WDO}}$ ) remains high if there is a transition or pulse at WDI during the watchdog timeout period. The watchdog function is disabled and  $\overline{\text{WDO}}$  is a logic high when  $V_{\text{CC}}$  is below the reset threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog timeout period,  $\overline{\text{RESET}}$  and  $\overline{\text{RESET}}$  are asserted for the reset timeout period (200ms typical).  $\overline{\text{WDO}}$  goes low and remains low until the next transition at WDI (Figure 2). If WDI is held high or low indefinitely,  $\overline{\text{RESET}}$  and  $\overline{\text{RESET}}$  will generate 200ms pulses every 1.6sec.  $\overline{\text{WDO}}$  has a 2 x TTL output characteristic.

### Selecting an Alternative Watchdog and Reset Timeout Period

The OSC SEL and OSC IN inputs control the watchdog and reset timeout periods. Floating OSC SEL and OSC IN or tying them both to  $V_{\text{OUT}}$  selects the nominal 1.6sec watchdog timeout period and 200ms reset timeout period. Connecting OSC IN to GND and floating or connecting OSC SEL to  $V_{\text{OUT}}$  selects the 100ms normal watchdog timeout delay and 1.6sec delay immediately after reset. The reset timeout delay remains 200ms (Figure 2). Select alternative timeout periods by connecting OSC SEL to GND and connecting a capacitor between OSC IN and GND, or by externally driving OSC IN (Table 1 and Figure 3). OSC IN is internally connected to a  $\pm 100\text{nA}$  (typ) current source that charges and discharges the timing capacitor to create the oscillator frequency, which sets the reset and watchdog timeout periods (see *Connecting a Timing Capacitor at OSC IN* in the *Applications Information* section).



# Microprocessor Supervisory Circuits

**Table 1. Reset Pulse Width and Watchdog Timeout Selections**

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period
		Normal	Immediately After Reset	
Low	External Clock Input	1024 clks	4096 clks	2048 clks
Low	External Capacitor	(600/47pF x C)ms	(2.4/47pF x C)sec	(1200/47pF x C)ms
Floating	Low	100ms	1.6sec	200ms
Floating	Floating	1.6sec	1.6sec	200ms

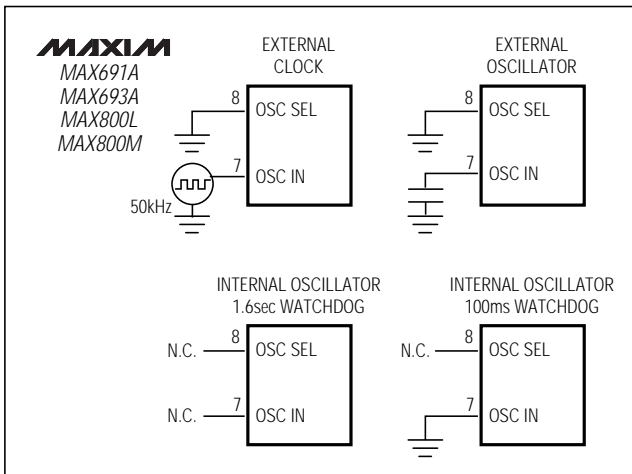


Figure 3. Oscillator Circuits

### Chip-Enable Signal Gating

The MAX691A/MAX693A/MAX800L/MAX800M provide internal gating of chip-enable (CE) signals to prevent erroneous data from being written to CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. All these parts use a series transmission gate from  $\overline{\text{CE}} \text{ IN}$  to  $\overline{\text{CE}} \text{ OUT}$  (Figure 4).

The 10ns max CE propagation delay from  $\overline{\text{CE}} \text{ IN}$  to  $\overline{\text{CE}} \text{ OUT}$  enables the parts to be used with most  $\mu\text{Ps}$ .

### Chip-Enable Input

The Chip-Enable Input ( $\overline{\text{CE}} \text{ IN}$ ) is high impedance (disabled mode) while RESET and  $\overline{\text{RESET}}$  are asserted.

During a power-down sequence where  $V_{\text{CC}}$  falls below the reset threshold or a watchdog fault,  $\overline{\text{CE}} \text{ IN}$  assumes a high-impedance state when the voltage at  $\overline{\text{CE}} \text{ IN}$  goes high or 15 $\mu\text{s}$  after reset is asserted, whichever occurs first (Figure 5).

During a power-up sequence,  $\overline{\text{CE}} \text{ IN}$  remains high impedance, regardless of  $\overline{\text{CE}} \text{ IN}$  activity, until reset is deasserted following the reset timeout period.

In the high-impedance mode, the leakage currents into this terminal are  $\pm 1\mu\text{A}$  max over temperature. In the low-impedance mode, the impedance of  $\overline{\text{CE}} \text{ IN}$  appears as a 75 $\Omega$  resistor in series with the load at  $\overline{\text{CE}} \text{ OUT}$ .

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to  $\overline{\text{CE}} \text{ IN}$  and the capacitive loading on the Chip-Enable Output ( $\overline{\text{CE}} \text{ OUT}$ ) (see Chip-Enable Propagation Delay vs.  $\overline{\text{CE}} \text{ OUT}$  Load Capacitance in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point of  $\overline{\text{CE}} \text{ IN}$  to the 50% point of  $\overline{\text{CE}} \text{ OUT}$  using a 50 $\Omega$  driver and 50pF of load capacitance (Figure 6). For minimum propagation delay, minimize the capacitive load at  $\overline{\text{CE}} \text{ OUT}$ , and use a low output-impedance driver.

### Chip-Enable Output

In the enabled mode, the impedance of  $\overline{\text{CE}} \text{ OUT}$  is equivalent to 75 $\Omega$  in series with the source driving  $\overline{\text{CE}} \text{ IN}$ . In the disabled mode, the 75 $\Omega$  transmission gate is off and  $\overline{\text{CE}} \text{ OUT}$  is actively pulled to  $V_{\text{OUT}}$ . This source turns off when the transmission gate is enabled.

### LOW LINE Output

$\overline{\text{LOW LINE}}$  is the buffered output of the reset threshold comparator.  $\overline{\text{LOW LINE}}$  typically sinks 3.2mA at 0.1V. For normal operation ( $V_{\text{CC}}$  above the  $\overline{\text{LOW LINE}}$  threshold),  $\overline{\text{LOW LINE}}$  is pulled to  $V_{\text{OUT}}$ .

### Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the IC. Common uses include low-battery indication (Figure 7), and early power-fail warning (see *Typical Operating Circuit*).

### Power-Fail Input

Power Fail Input (PFI) is the input to the power-fail comparator. It has a guaranteed input leakage of  $\pm 25\text{nA}$  max over temperature. The typical comparator delay is 25 $\mu\text{s}$  from  $V_{\text{IL}}$  to  $V_{\text{OL}}$  (power failing), and 60 $\mu\text{s}$  from  $V_{\text{IH}}$  to  $V_{\text{OH}}$  (power being restored). If PFI is not used, connect it to ground.

# Microprocessor Supervisory Circuits

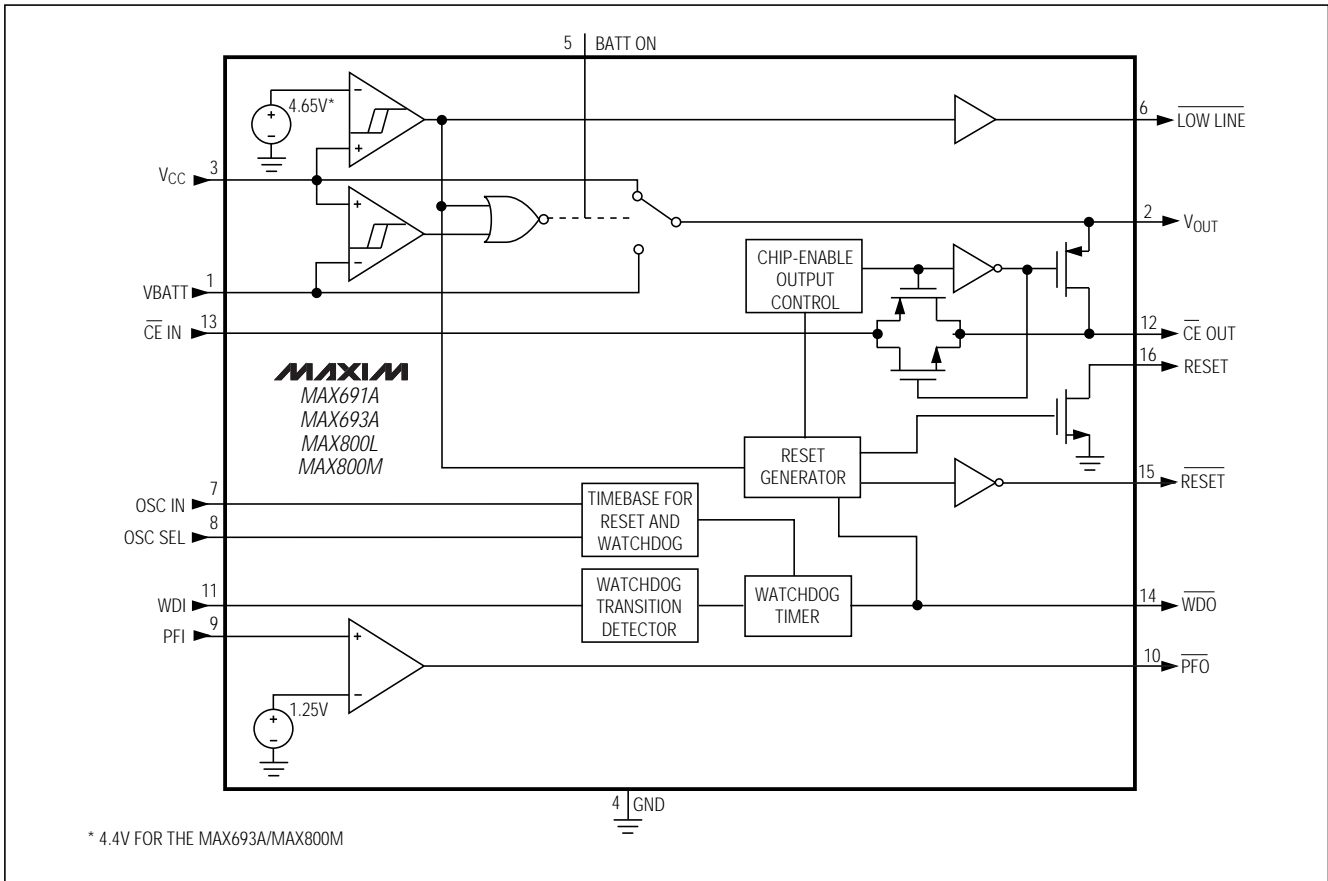


Figure 4. MAX691A/MAX693A/MAX800L/MAX800M Block Diagram

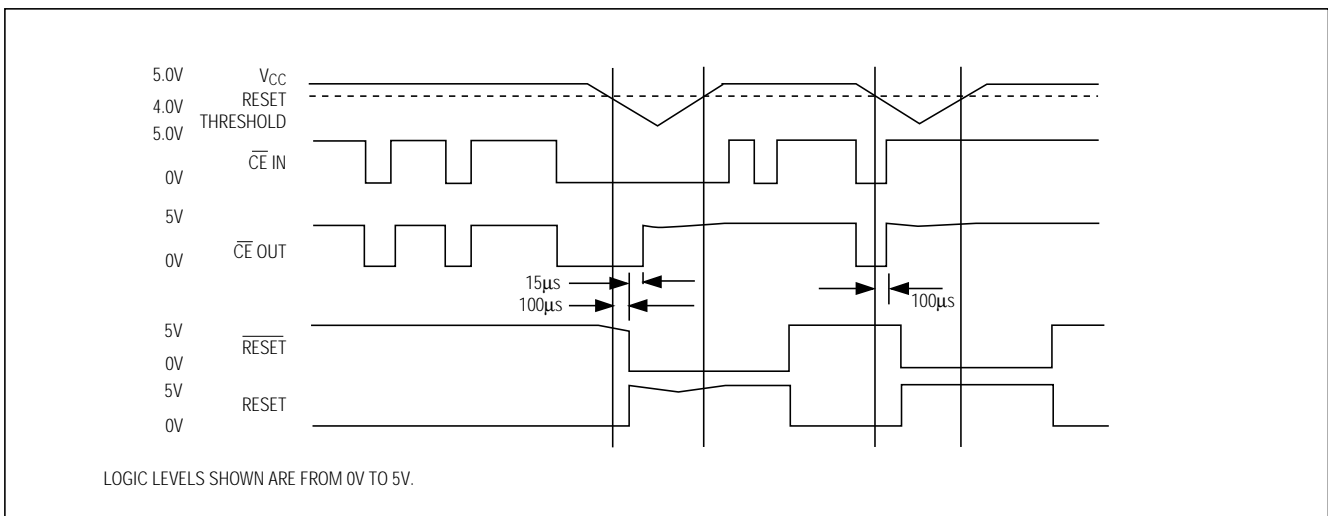


Figure 5. Reset and Chip-Enable Timing

# Microprocessor Supervisory Circuits

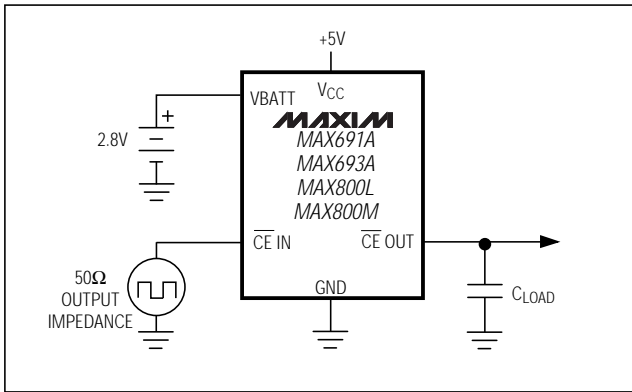


Figure 6. CE Propagation Delay Test Circuit

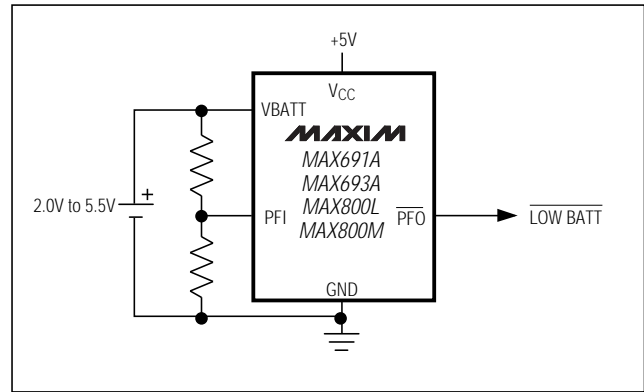


Figure 7. Low-Battery Indicator

**Table 2. Input and Output Status in Battery-Backup Mode**

PIN	NAME	STATUS
1	VBATT	Supply current is 1μA max.
2	V <sub>OUT</sub>	V <sub>OUT</sub> is connected to VBATT through an internal PMOS switch.
3	V <sub>CC</sub>	Battery switchover comparator monitors V <sub>CC</sub> for active switchover.
4	GND	GND 0V, 0V reference for all signals.
5	BATT ON	Logic high. The open-circuit output is equal to V <sub>OUT</sub> .
6	LOWLINE	Logic low*
7	OSC IN	OSC IN is ignored.
8	OSC SEL	OSC SEL is ignored.
9	PFI	The power-fail comparator remains active in the battery-backup mode for V <sub>CC</sub> ≥ VBATT - 1.2V typ.
10	PFO	The power-fail comparator remains active in the battery-backup mode for V <sub>CC</sub> ≥ VBATT - 1.2V typ. Below this voltage, PFO is forced low.
11	WDI	Watchdog is ignored.
12	CE OUT	Logic high. The open-circuit voltage is equal to V <sub>OUT</sub> .
13	CE IN	High impedance
14	WDO	Logic high. The open-circuit voltage is equal to V <sub>OUT</sub> .
15	RESET	Logic low*
16	RESET	High impedance*

\* V<sub>CC</sub> must be below the reset threshold to enter battery-backup mode.

## Power-Fail Output

The Power-Fail Output ( $\overline{\text{PFO}}$ ) goes low when PFI goes below 1.25V. It typically sinks 3.2mA with a saturation voltage of 0.1V. With PFI above 1.25V,  $\overline{\text{PFO}}$  is actively pulled to V<sub>OUT</sub>.

## Battery-Backup Mode

Two conditions are required to switch to battery-backup mode: 1) V<sub>CC</sub> must be below the reset threshold, and 2) V<sub>CC</sub> must be below VBATT. Table 2 lists the status of the inputs and outputs in battery-backup mode.

## Battery On Output

The Battery On (BATT ON) output indicates the status of the internal V<sub>CC</sub>/battery-switchover comparator, which controls the internal V<sub>CC</sub> and VBATT switches. For V<sub>CC</sub> greater than VBATT (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10μA from V<sub>OUT</sub>. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications (see *Typical Operating Circuit*).

## Input Supply Voltage

The Input Supply Voltage (V<sub>CC</sub>) should be a regulated 5V. V<sub>CC</sub> connects to V<sub>OUT</sub> via a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω each. The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

# Microprocessor Supervisory Circuits

## Battery-Backup Input

The Battery-Backup Input (VBATT) is similar to the  $V_{CC}$  input except the PMOS switch and parallel diode are much smaller. Accordingly, the on-resistances of the diode and the switch are each approximately  $10\Omega$ . Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of this input is less than  $1\mu\text{A}$  over temperature and supply voltage (Figure 8).

## Output Supply Voltage

The Output Supply Voltage ( $V_{OUT}$ ) pin is internally connected to the substrate of the IC and supplies current to the external system and internal circuitry. All open-circuit outputs will, for example, assume the  $V_{OUT}$  voltage in their high states rather than the  $V_{CC}$  voltage. At the maximum source current of 250mA,  $V_{OUT}$  will typically be 200mV below  $V_{CC}$ . Decouple this terminal with a  $0.1\mu\text{F}$  capacitor.

## Applications Information

The MAX691A/MAX693A/MAX800L/MAX800M are not short-circuit protected. Shorting  $V_{OUT}$  to ground, other than power-up transients such as charging a decoupling capacitor, destroys the device.

All open-circuit outputs swing between  $V_{OUT}$  and GND rather than  $V_{CC}$  and GND.

If long leads connect to the chip inputs, insure that these leads are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

- 1) Normal operating mode with all circuitry powered up. Typical supply current from  $V_{CC}$  is  $35\mu\text{A}$  while only leakage currents flow from the battery.
- 2) Battery-backup mode where  $V_{CC}$  is typically within 0.7V below VBATT. All circuitry is powered up and the supply current from the battery is typically less than  $60\mu\text{A}$ .
- 3) Battery-backup mode where  $V_{CC}$  is less than VBATT by at least 0.7V. VBATT supply current is  $1\mu\text{A}$  max.

## Using SuperCap™ or MaxCap™ with the MAX691A/MAX693A/MAX800L/MAX800M

VBATT has the same operating voltage range as  $V_{CC}$ , and the battery switchover threshold voltages are typically  $\pm 30\text{mV}$  centered at VBATT, allowing use of a SuperCap and a simple charging circuit as a backup source (Figure 9).

If  $V_{CC}$  is above the reset threshold and VBATT is 0.5V above  $V_{CC}$ , current flows to  $V_{OUT}$  and  $V_{CC}$  from VBATT until the voltage at VBATT is less than 0.5V above  $V_{CC}$ . For example, with a SuperCap connected to VBATT and through a diode to  $V_{CC}$ , if  $V_{CC}$  quickly changes from 5.4V to 4.9V, the capacitor discharges through  $V_{OUT}$  and  $V_{CC}$  until VBATT reaches 5.1V typ. Leakage current through the SuperCap charging diode and the internal power diode eventually discharges the SuperCap to  $V_{CC}$ . Also, if  $V_{CC}$  and VBATT start from 0.1V above the reset threshold and power is lost at  $V_{CC}$ , the SuperCap on VBATT discharges through  $V_{CC}$  until VBATT reaches the reset threshold; then the battery-backup mode is initiated and the current through  $V_{CC}$  goes to zero.

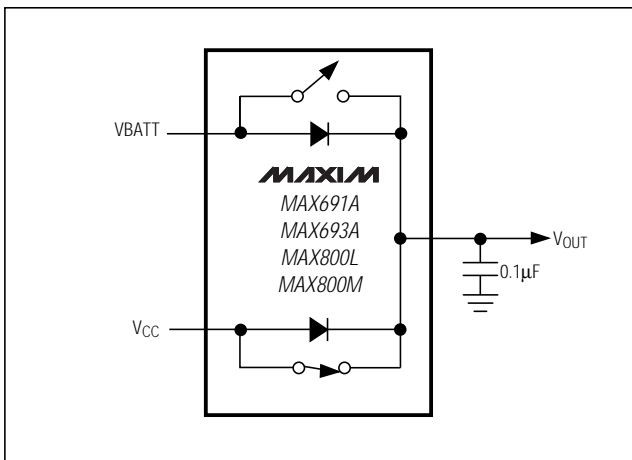


Figure 8.  $V_{CC}$  and VBATT to  $V_{OUT}$  Switch

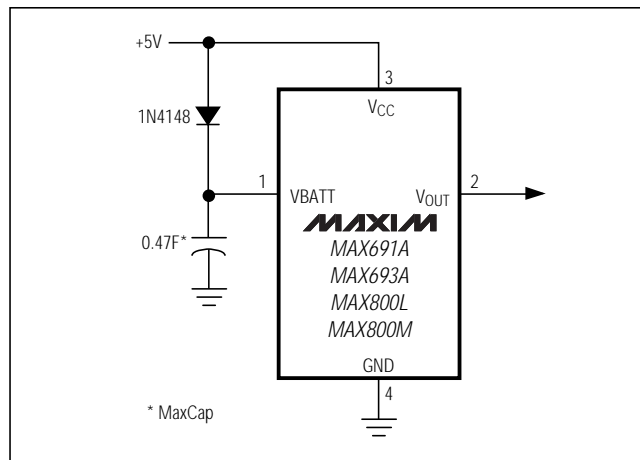


Figure 9. SuperCap or MaxCap on VBATT

# Microprocessor Supervisory Circuits

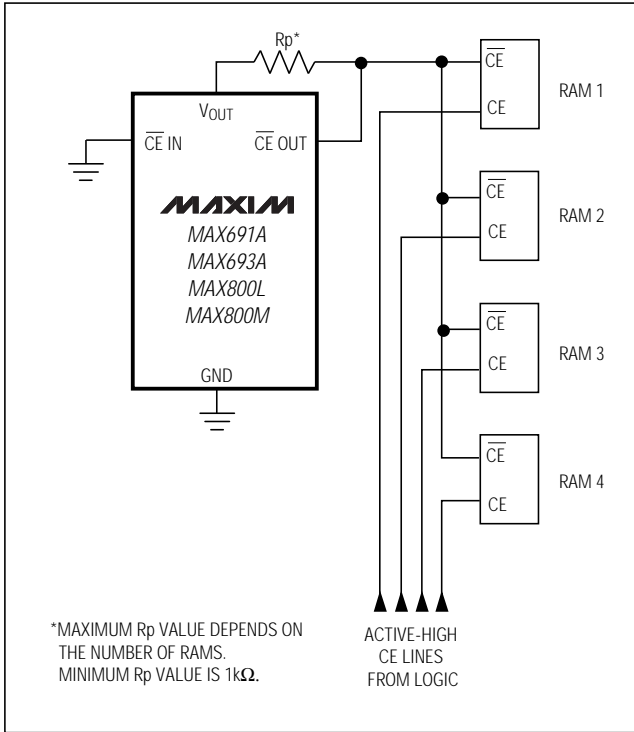


Figure 10. Alternate CE Gating

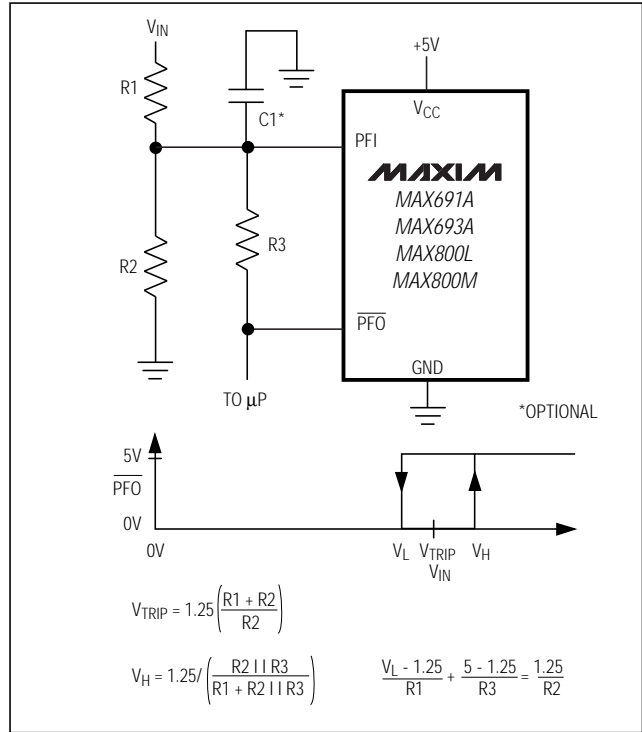


Figure 11. Adding Hysteresis to the Power-Fail Comparator

## Using Separate Power Supplies for VBATT and VCC

If using separate power supplies for VCC and VBATT, VBATT must be less than 0.3V above VCC when VCC is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at VCC, current flows continuously from VBATT to VCC via the VBATT-to-VOUT diode and the VOUT-to-VCC switch until the circuit is broken (Figure 8).

## Alternate Chip-Enable Gating

Using memory devices with both CE and CE inputs allows the CE loop to be bypassed. To do this, connect CE IN to ground, pull up CE OUT to VOUT, and connect CE OUT to the CE input of each memory device (Figure 10). The CE input of each part then connects directly to the chip-select logic, which does not have to be gated.

## Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when VIN is near the power-fail comparator trip point. Figure 11 shows how to add hysteresis to the power-fail com-

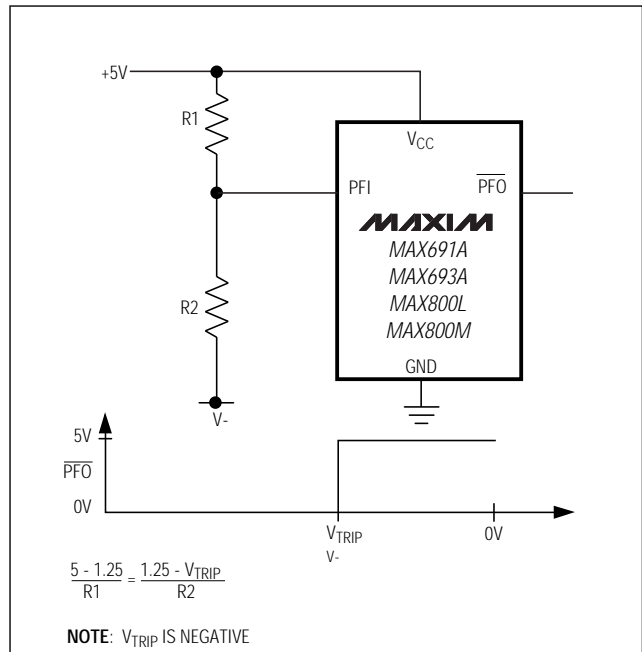


Figure 12. Monitoring a Negative Voltage

# Microprocessor Supervisory Circuits

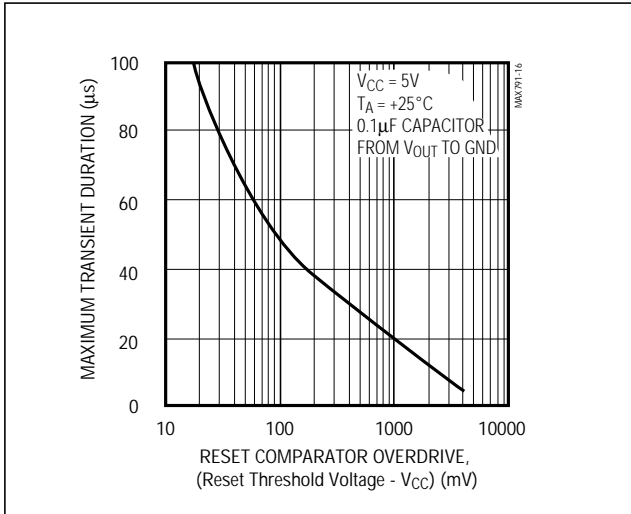


Figure 13. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

parator. Select the ratio of R1 and R2 such that PFI sees 1.25V when  $V_{IN}$  falls to the desired trip point ( $V_{TRIP}$ ). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1 $\mu$ A to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10k $\Omega$  to prevent it from loading down the PFO pin. Capacitor C1 adds noise rejection.

### Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 12's circuit. When the negative supply is valid,  $\overline{PFO}$  is low. When the negative supply voltage drops,  $\overline{PFO}$  goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the  $V_{CC}$  voltage, and resistors R1 and R2.

### Backup-Battery Replacement

The backup battery may be disconnected while  $V_{CC}$  is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

### Negative-Going $V_{CC}$ Transients

While issuing resets to the  $\mu$ P during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration, negative-going  $V_{CC}$  transients (glitches). It is usually undesirable to reset the  $\mu$ P when  $V_{CC}$  experiences only small glitches.

Figure 13 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going  $V_{CC}$  pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset-comparator overdrive). The graph shows the maximum pulse width a negative-going  $V_{CC}$  transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a  $V_{CC}$  transient that goes 100mV below the reset threshold and lasts for 40 $\mu$ s or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the  $V_{CC}$  pin provides additional transient immunity.

### Connecting a Timing Capacitor at OSC IN

When OSC SEL is connected to ground, OSC IN disconnects from its internal 10 $\mu$ A (typ) pull-up and is internally connected to a  $\pm$ 100nA current source. When a capacitor is connected from OSC IN to ground (to select alternative reset and watchdog timeout periods), the current source charges and discharges the timing capacitor to create the oscillator that controls the reset and watchdog timeout period. To prevent timing errors or oscillator start-up problems, minimize external current leakage sources at this pin, and locate the capacitor as close to OSC IN as possible. The sum of PC-board leakage plus OSC capacitor leakage must be small compared to  $\pm$ 100nA.

# Microprocessor Supervisory Circuits

## Maximum $V_{CC}$ Fall Time

The  $V_{CC}$  fall time is limited by the propagation delay of the battery switchover comparator and should not exceed  $0.03V/\mu s$ . A standard rule of thumb for filter capacitance on most regulators is on the order of  $100\mu F$  per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial  $V_{CC}$  fall rate is just the inverse or  $1A/100\mu F = 0.01V/\mu s$ . The  $V_{CC}$  fall rate decreases with time as  $V_{CC}$  falls exponentially, which more than satisfies the maximum fall-time requirement.

## Watchdog Software Considerations

A way to help the watchdog timer keep a closer watch on software execution involves setting and resetting the watchdog input at different points in the program, rather than “pulsing” the watchdog input high-low-high or low-high-low. This technique avoids a “stuck” loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 14 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should “hang” in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

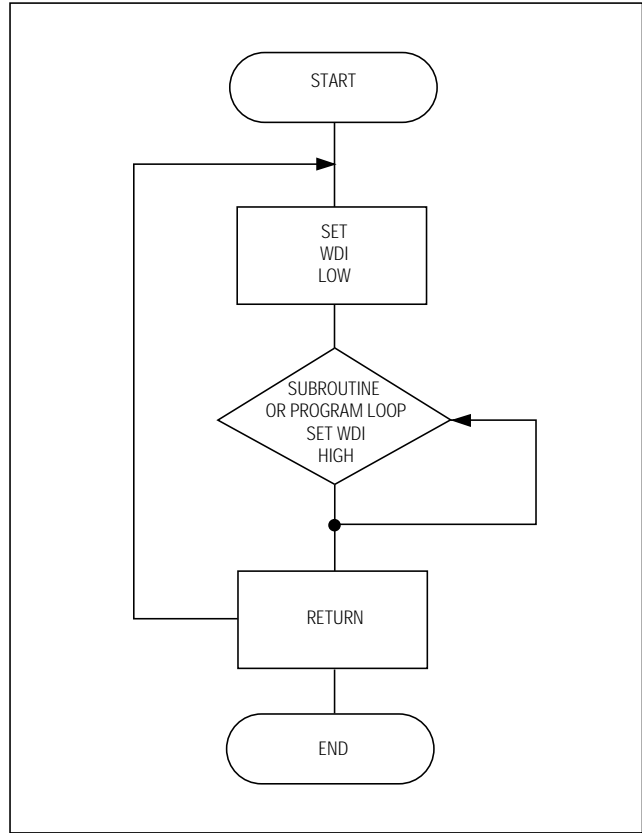


Figure 14. Watchdog Flow Diagram

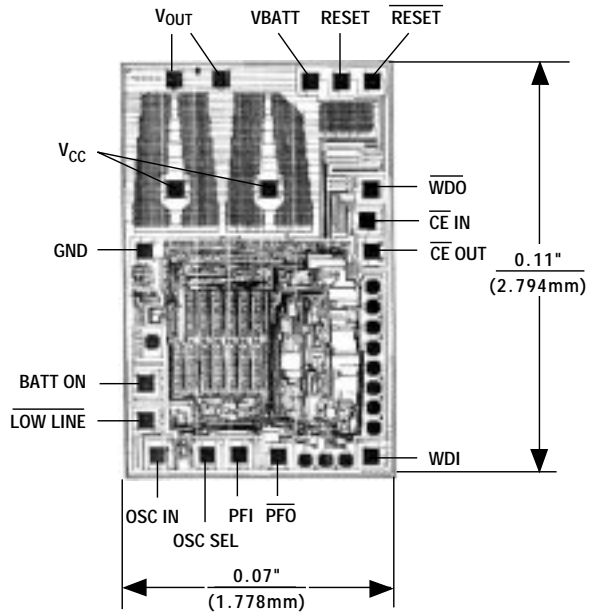
# Microprocessor Supervisory Circuits

## Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
<b>MAX693ACPE</b>	0°C to +70°C	16 Plastic DIP
MAX693ACSE	0°C to +70°C	16 Narrow SO
MAX693ACWE	0°C to +70°C	16 Wide SO
MAX693AC/D	0°C to +70°C	Dice*
MAX693AEPE	-40°C to +85°C	16 Plastic SO
MAX693AESE	-40°C to +85°C	16 Narrow SO
MAX693AEWE	-40°C to +85°C	16 Wide SO
MAX693AEJE	-40°C to +85°C	16 CERDIP
MAX693AMJE	-55°C to +125°C	16 CERDIP
<b>MAX800LCPE</b>	0°C to +70°C	16 Plastic DIP
MAX800LCSE	0°C to +70°C	16 Narrow SO
MAX800LEPE	-40°C to +85°C	16 Plastic DIP
MAX800LESE	-40°C to +85°C	16 Narrow SO
<b>MAX800MCPE</b>	0°C to +70°C	16 Plastic DIP
MAX800MCSE	0°C to +70°C	16 Narrow SO
MAX800MEPE	-40°C to +85°C	16 Plastic DIP
MAX800MESE	-40°C to +85°C	16 Narrow SO

\* Dice are specified at  $T_A = +25^\circ\text{C}$ , DC parameters only.

## Chip Topography



TRANSISTOR COUNT: 729  
SUBSTRATE CONNECTED TO V<sub>OUT</sub>

## Package Information

INCHES		MILLIMETERS		
MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050			1.27
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

INCHES		MILLIMETERS		N	MS012
MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	B A
D	0.337	0.344	8.55	8.75	14 B
D	0.386	0.394	9.80	10.00	16 C

NOTES:  
 1. DAE DO NOT INCLUDE MOLD FLASH  
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")  
 3. LEADS TO BE COPPLANAR WITHIN .102mm (.004")  
 4. CONTROLLING DIMENSION MILLIMETER  
 5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE  
 6. N = NUMBER OF PINS

**MAXIM** INTEGRATED PRODUCTS  
 PACKAGE FAMILY OUTLINE: SOIC .150"  $\frac{1}{4}$  21-0041 A

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