

M62359P,FP

8-BIT 8CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62359 is a 8-channel 8-bit voltage output digital to analog converter.
 The M62359 includes data latch circuit and gain change circuit of output amplifiers.
 Input data is a easy-to-use three-wires serial interface.
 It is able to cascading serial use with Do terminal.
 Gain set up data change a case the each channel's output voltage range is change ,and each channel's output voltage range is able to change severally make use of gain set up data.

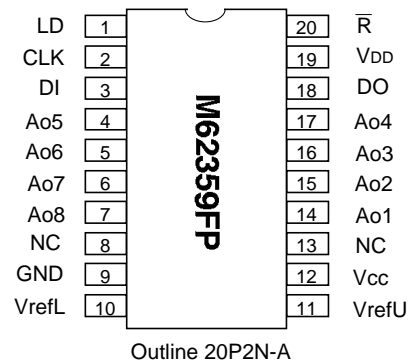
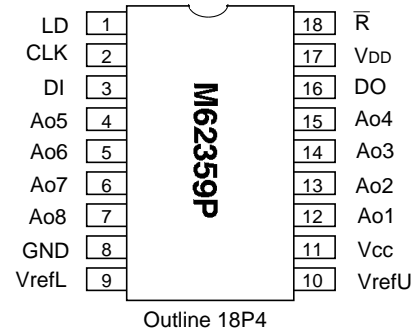
FEATURES

- All channel includes gain change latch circuit with output amplifiers.
- 14-bit serial data input
- Built-in reset circuit

APPLICATION

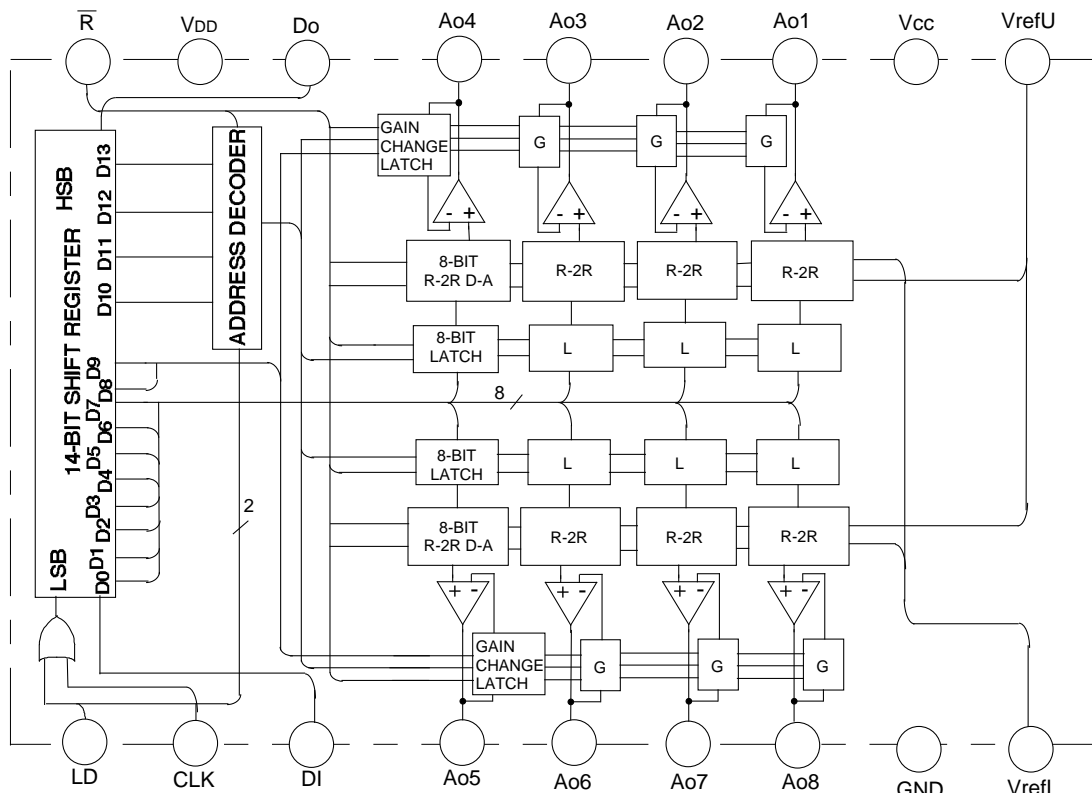
Conversion from digital control data to analog control data for home-use and industrial equipment.
 Automatic adjustment by combination with EEPROM and microcomputer(replacement of conventional half-fixed resistor).
 Signal gain control of DISPLAY-MONITOR or CTV.

PIN CONFIGURATION (TOP VIEW)



NC:NO CONNECTION

BLOCK DIAGRAM



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EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
③	DI	Serial data input terminal
⑬	DO	Serial data output terminal
②	CLK	Serial clock input terminal
①	LD	LD terminal input high level than latch circuit data load *1
⑰	V _{DD}	Digital power supply terminal
⑪	V _{CC}	Analog power supply terminal
⑧	GND	Digital and Analog common GND
⑩	V _{refU}	D-A converter high level reference voltage input terminal
⑨	V _{refL}	D-A converter low level reference voltage input terminal
⑱	\bar{R}	Reset terminal
⑫	Ao1	8-bit D-A converter output terminal
⑬	Ao2	
⑭	Ao3	
⑮	Ao4	
④	Ao5	
⑤	Ao6	
⑥	Ao7	
⑦	Ao8	

*1 When the LD terminal is "H" input data has load.

ABSOLUTE MAXIMUM RATINGS(T_a=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~13.5	V
V _{DD}	Supply voltage		-0.3~7	V
V _{refU}	D-A converter high level reference voltage		V _{DD}	V
V _{IN}	Input voltage		-0.3~V _{DD} +0.3	V
I _{DO}	Output current		-5~+5	mA
I _{AO}	Buffer amplifier output current range		-5~+5	mA
T _{opr}	Operating temperature		-20~+85	°C
T _{stg}	Storage temperature		-40~+125	°C

RECOMMENDED OPERATING CONDITIONS

- Digital supply voltage V_{DD} 5V±10%
- Analog supply voltage V_{CC} V_{DD}~13V

ELECTRICAL CHARACTERISTICS

Digital part(V_{CC}=13V,V_{DD}=V_{refU}=5V, T_a=-25 to +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{DD}	Supply voltage		4.5		5.5	V
I _{DD}	Circuit current	CLK=1MHz in action			1	mA
V _{IL}	Input low voltage				0.2V _{DD}	V
V _{IH}	Input high voltage		0.8V _{DD}			V
V _{OL}	Output low voltage	I _{OL} =1.0mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-400μA	V _{DD} -0.4			V

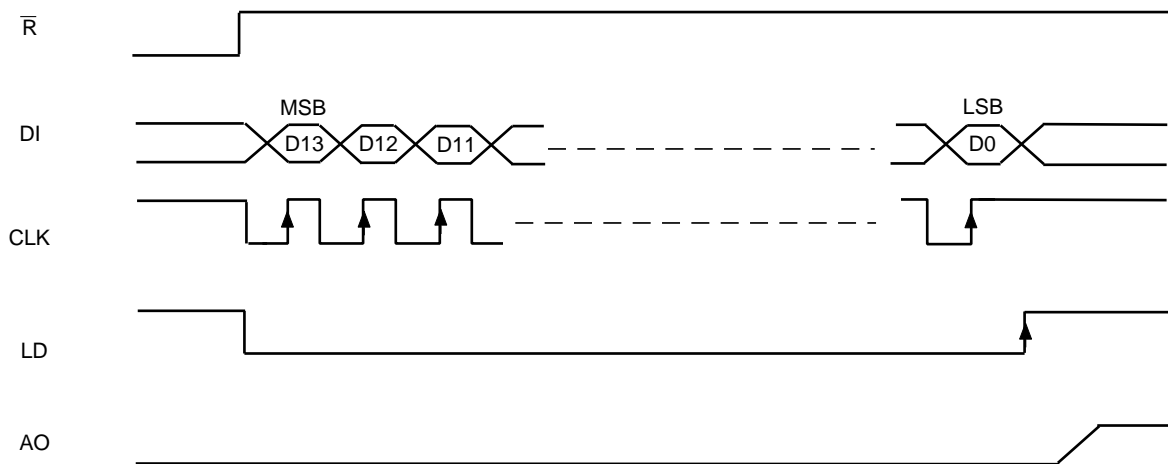
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Analog part ($V_{CC}=13V, V_{DD}=V_{refU}=5V, T_a=-20^{\circ}C \sim +85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		V_{DD}		13	V
I_{CC}	Circuit current			2	4	mA
I_{refU}	D-A converter high level reference input current	All ch's set up at 107/256		1.2	2.5	mA
V_{refU}	D-A converter high level reference voltage range		3.5		V_{DD}	V
V_{refL}	D-A converter low level reference voltage range		0		1.5	V
V_{AO}	D-A converter output voltage range	$I_{AO} = \pm 500\mu A$	0.1		$V_{CC}-0.1$	V
		$I_{AO} = \pm 1mA$	0.2		$V_{CC}-0.2$	
I_{AO}	Buffer amplifier output current range				± 2.5	mA
DNL	Differential nonlinearity	Guaranteed monotonic	-1.0		1.0	LSB
NL	Nonrinality		-1.5		1.5	LSB
EZ	Zero code error	$V_{refU}=4.79V$	-2		2	LSB
EF	Full scale error	$V_{refL}=0.95V$ without load	-2		2	LSB
E_o	Gain error		-3		3	%
SR	Output slew rate			0.2		V/ μs

TIMING CHART (MODEL)



Input data is carried out LD signal Low besides CLK signal positive edge.
CLK,LD is keep generally High level.

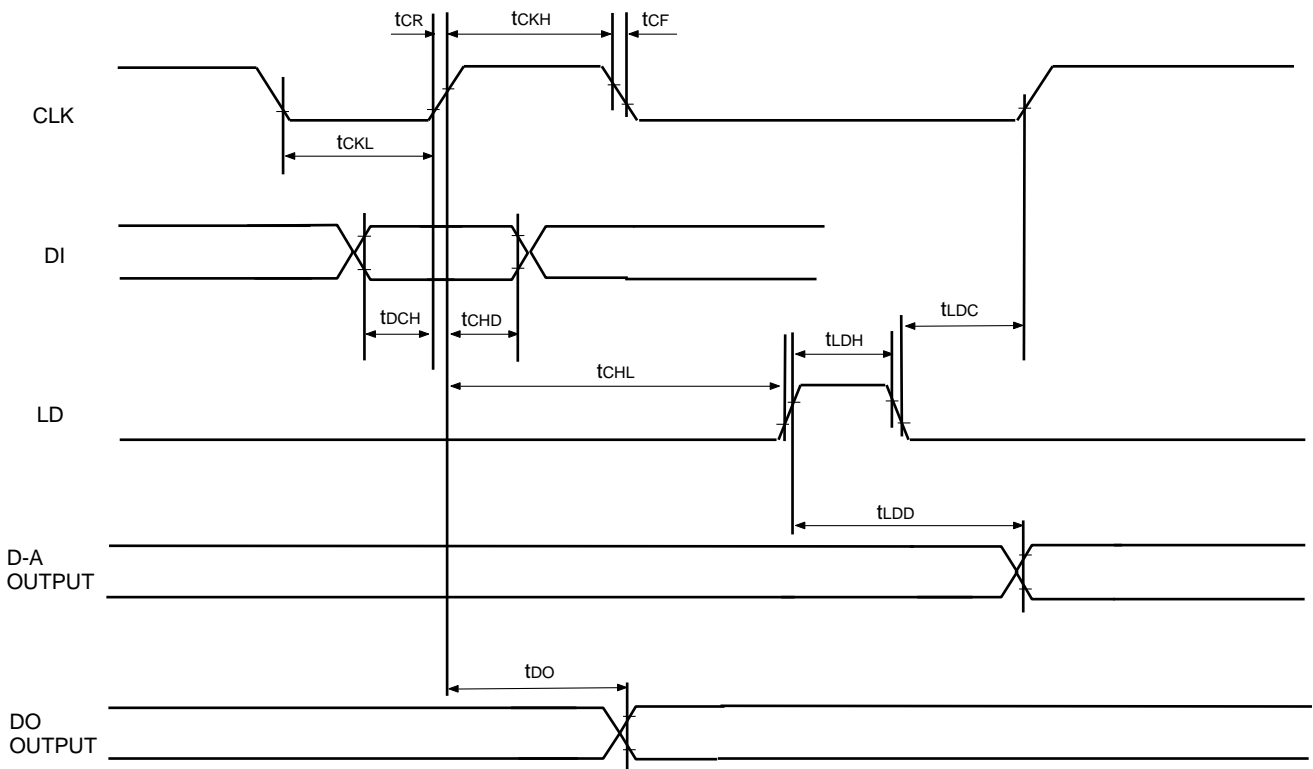
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AC CHARACTERISTICS (Ta=25°C, Vcc=13V, VDD=VrefU=5V, VrefL=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tCKL	Clock "L" pulse width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR	Clock rise time				200	ns
tCF	Clock fall time				200	ns
tDCH	Data set up time		60			ns
tCHD	Data hold time		100			ns
tCHL	LD setup time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" pulse width		100			ns
tDO	Data output delay time	CL=100pF	70		350	ns
tLDD	Data output setting time	Without load			300	μs

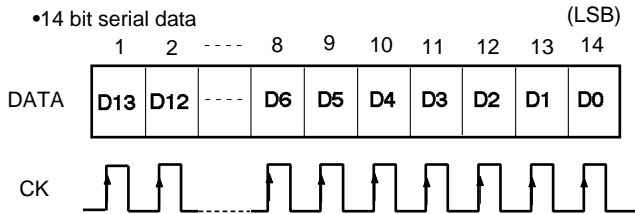
TIMING CHART



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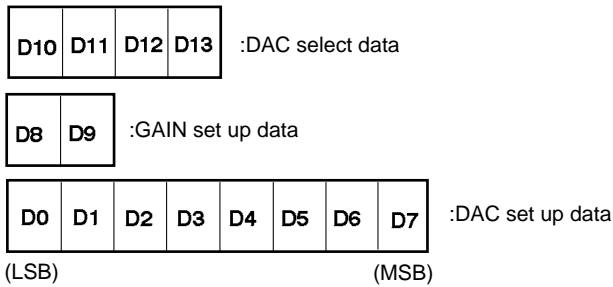
DIGITAL FORMAT



•DAC select data

D10	D11	D12	D13	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2 selection
0	0	1	1	Ao3 selection
0	1	0	0	Ao4 selection
0	1	0	1	Ao5 selection
0	1	1	0	Ao6 selection
0	1	1	1	Ao7 selection
1	0	0	0	Ao8 selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

•Data assignment



•GAIN set up data

D8	D9	K	DAC output range (VrefU=5V,VrefL=0V)
0	0	1	0~5V
1	0	1.6	0~8V
0	1	1.8	0~9V
1	1	2.4	0~12V

•DAC set up data

(LSB)							(MSB)	DAC voltage
D0	D2	D3	D4	D5	D6	D7		
0	0	0	0	0	0	0	$1/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
1	0	0	0	0	0	0	$2/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
0	0	0	0	0	0	0	$3/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
1	0	0	0	0	0	0	$4/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0	1	1	1	1	1	1	$255/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	
1	1	1	1	1	1	1	$256/256 \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$	

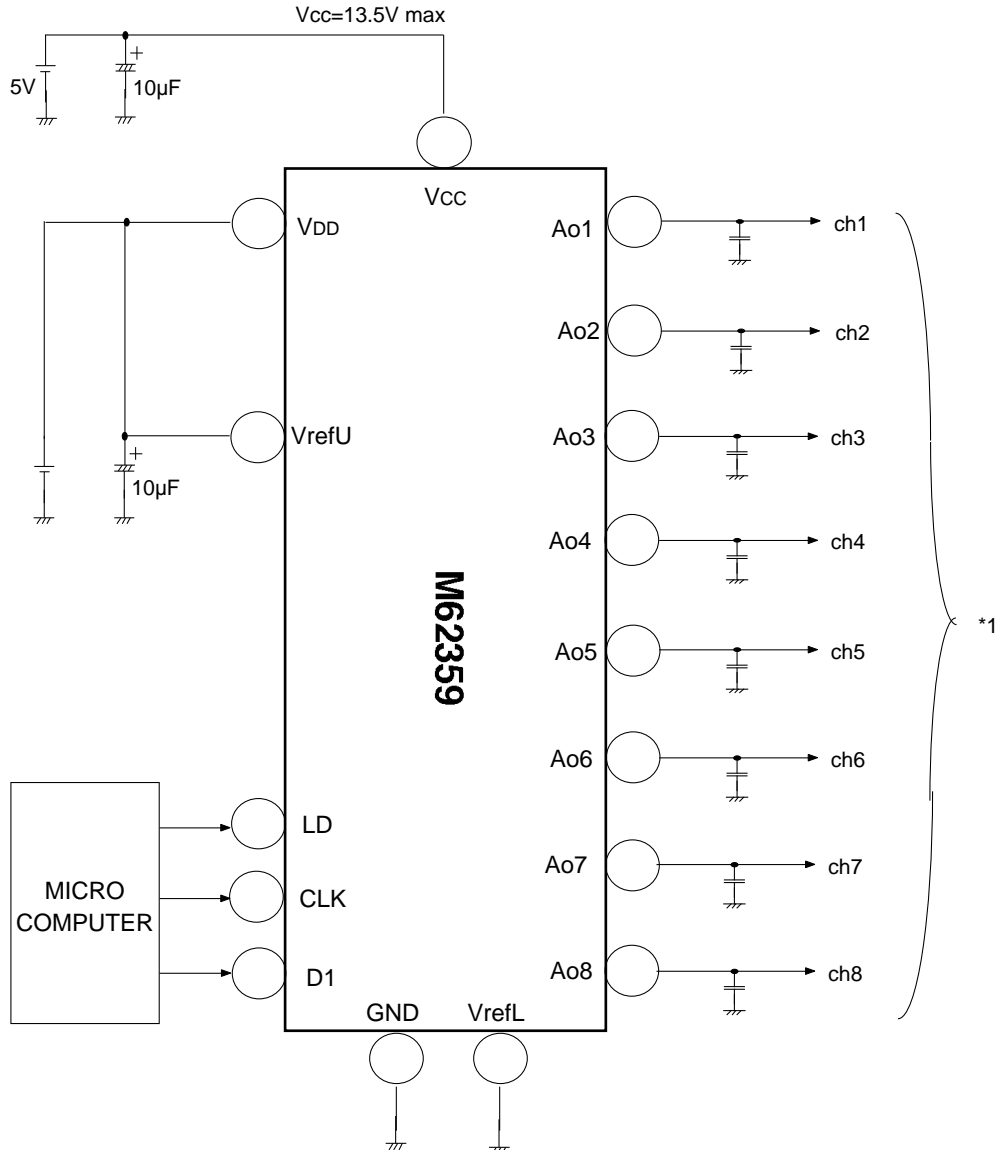
$$A_o = \frac{2^0 \times D_0 + 2^1 \times D_1 + 2^2 \times D_2 + \dots + 2^6 \times D_6 + 2^7 \times D_7 + 1}{256} \cdot (V_{refU} - V_{refL}) \cdot K + V_{refL}$$

K: Amplifiers gain

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APPLICATION CIRCUIT



This IC's output amplifier has an advantage to capacitive load. So it's no problem at device action when connect capacitor among output to GND for every noise eliminate.

*1 If be used in a cathode-ray tube sets and high voltage sets, please connect capacitor among output to GND, about 0.1µF~1µF, because keep off effect of spark and electric discharge etc.