
HM6264BI Series

64k SRAM (8-kword × 8-bit)
Wide Temperature Range version

HITACHI

ADE-203-492C (Z)
Rev. 3.0
May. 8, 2000

Description

The Hitachi HM6264BI is 64k-bit static RAM organized 8-kword × 8-bit. It realizes higher performance and low power consumption by 1.5 μm CMOS process technology. The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, is available for high density mounting.

Features

- Single 5 V supply: 5 V ± 10%
- Access time: 100/120 ns (max)
- Power dissipation:
 - Standby: 10 μW (typ)
 - Operation: 15 mW (typ) (f = 1 MHz)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation capability
- Operating temperature range: -40°C to +85°C

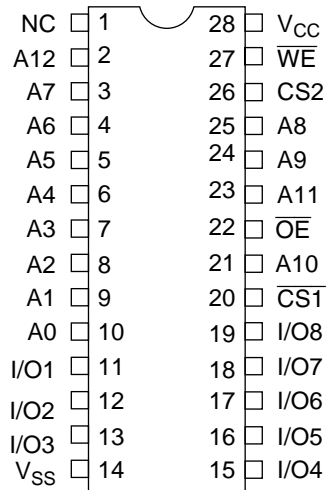
HM6264BI Series

Ordering Information

Type No.	Access time	Package
HM6264BLPI-10	100 ns	600-mil, 28-pin plastic DIP (DP-28)
HM6264BLPI-12	120 ns	
HM6264BLFPI-10T	100 ns	450-mil, 28-pin plastic SOP(FP-28DA)
HM6264BLFPI-12T	120 ns	

Pin Arrangement

HM6264BLPI/BLFPI Series

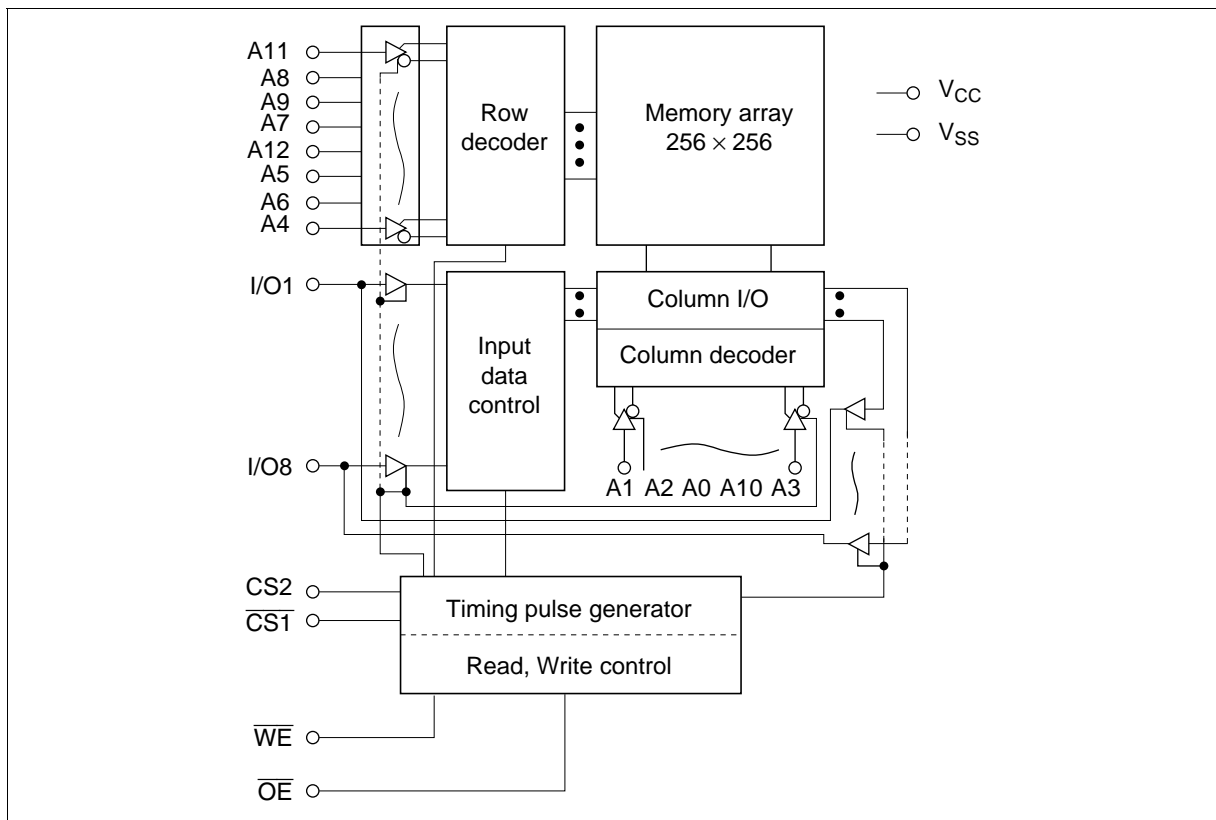


(Top view)

Pin Description

Pin name	Function
A0 to A12	Address input
I/O1 to I/O8	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
\overline{WE}	Write enable
\overline{OE}	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

\overline{WE}	$\overline{CS1}$	$CS2$	\overline{OE}	Mode	V_{CC} current	I/O pin	Ref. cycle
×	H	×	×	Not selected (power down)	I_{SB}, I_{SB1}	High-Z	—
×	×	L	×	Not selected (power down)	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage*1	V_{CC}	−0.5 to +7.0	V
Terminal voltage*1	V_T	−0.5*2 to $V_{CC} + 0.3$ *3	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−40 to +85	°C

- Notes: 1. Relative to V_{SS}
 2. V_T min: −3.0 V for pulse half-width ≤ 50 ns
 3. Maximum voltage is 7.0 V

Recommended DC Operating Conditions ($T_a = -40$ to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	−0.3*1	—	0.6	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 50 ns

DC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	2	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}
Operating power supply current	I_{CCDC}	—	7	20	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{ mA}$ others = V_{IH}/V_{IL}
Average operating power supply current	I_{CC1}	—	30	50	mA	Min cycle, duty = 100%, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{ mA}$ others = V_{IH}/V_{IL}
	I_{CC2}	—	3	8	mA	Cycle time = $1\ \mu\text{s}$, duty = 100%, $I_{I/O} = 0\text{ mA}$ $\overline{CS1} \leq 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$, $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $V_{IL} \leq 0.2\text{ V}$
Standby power supply current	I_{SB}	—	1	3	mA	$\overline{CS1} = V_{IH}$, $CS2 = V_{IL}$
	I_{SB1}^{*2}	—	2	200	μA	$\overline{CS1} \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq CS2 \leq 0.2\text{ V}$, $0\text{ V} \leq V_{in}$
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1.0\text{ mA}$

Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. V_{IL} min = -0.3V

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C_{in}	—	—	5	pF	$V_{in} = 0\text{ V}$
Input/output capacitance* ¹	$C_{I/O}$	—	—	7	pF	$V_{I/O} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

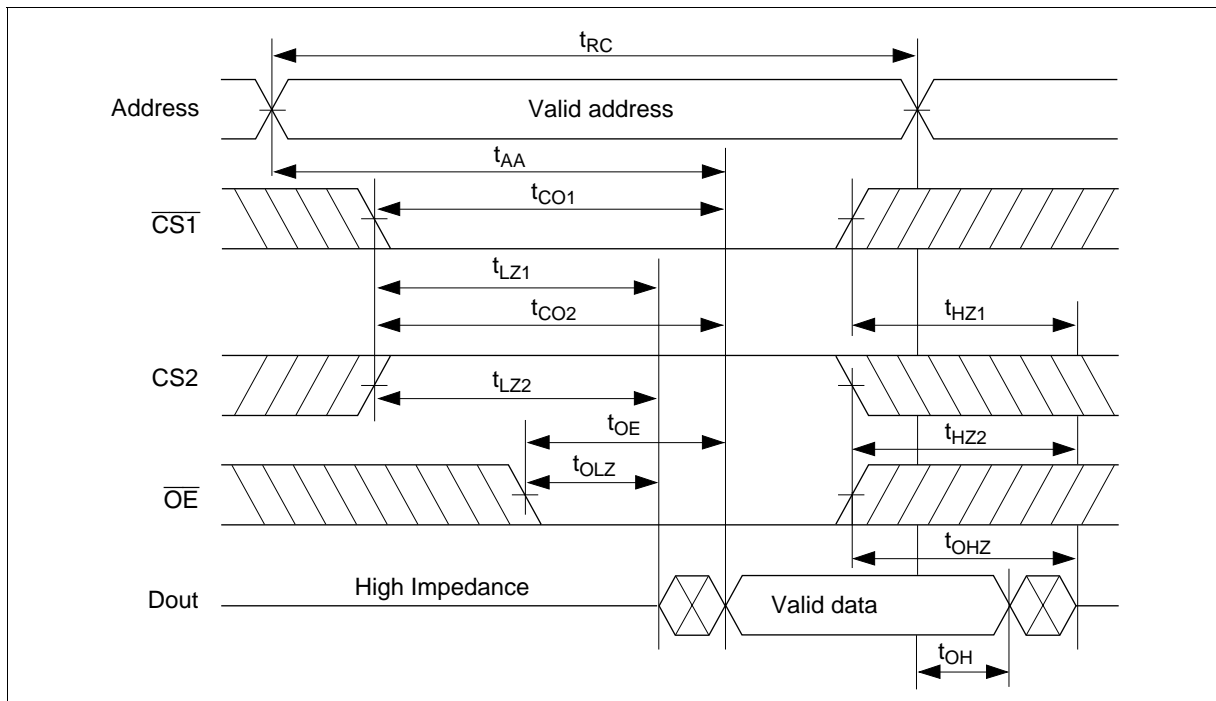
- Input pulse levels: 0.6 V to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

Read Cycle

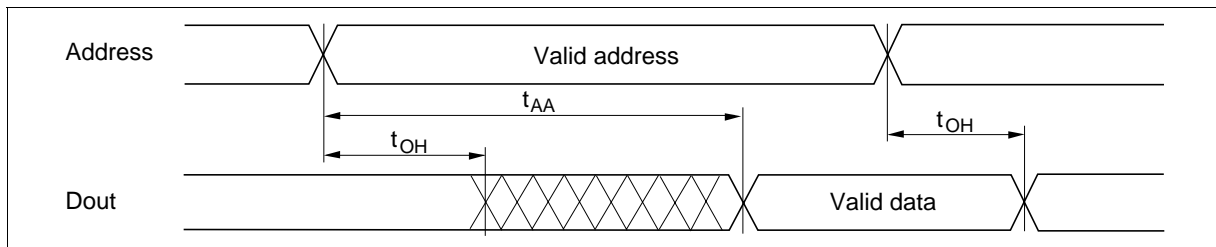
Parameter	Symbol	HM6264BI-10		HM6264BI-12		Unit	Notes
		Min	Max	Min	Max		
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
Chip select access time	$\overline{CS1}$ t_{CO1}	—	100	—	120	ns	
	CS2 t_{CO2}	—	100	—	120	ns	
Output enable to output valid	t_{OE}	—	50	—	60	ns	
Chip selection to output in low-Z	$\overline{CS1}$ t_{LZ1}	10	—	10	—	ns	2
	CS2 t_{LZ2}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselection in to output in high-Z	$\overline{CS1}$ t_{HZ1}	0	35	0	40	ns	1, 2
	CS2 t_{HZ2}	0	35	0	40	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	35	0	40	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

- Notes: 1. t_{HZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.
3. Address must be valid prior to or simultaneously with $\overline{CS1}$ going low or CS2 going high.

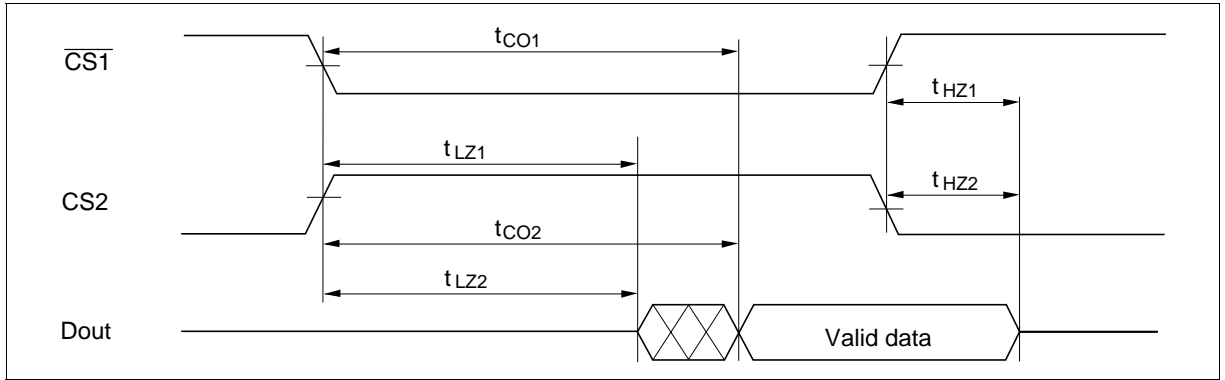
Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)



Read Timing Waveform (2) ($\overline{WE} = V_{IH}, \overline{OE} = V_{IL}$)



Read Timing Waveform (3) ($\overline{WE} = V_{IH}, \overline{OE} = V_{IL}$)*3



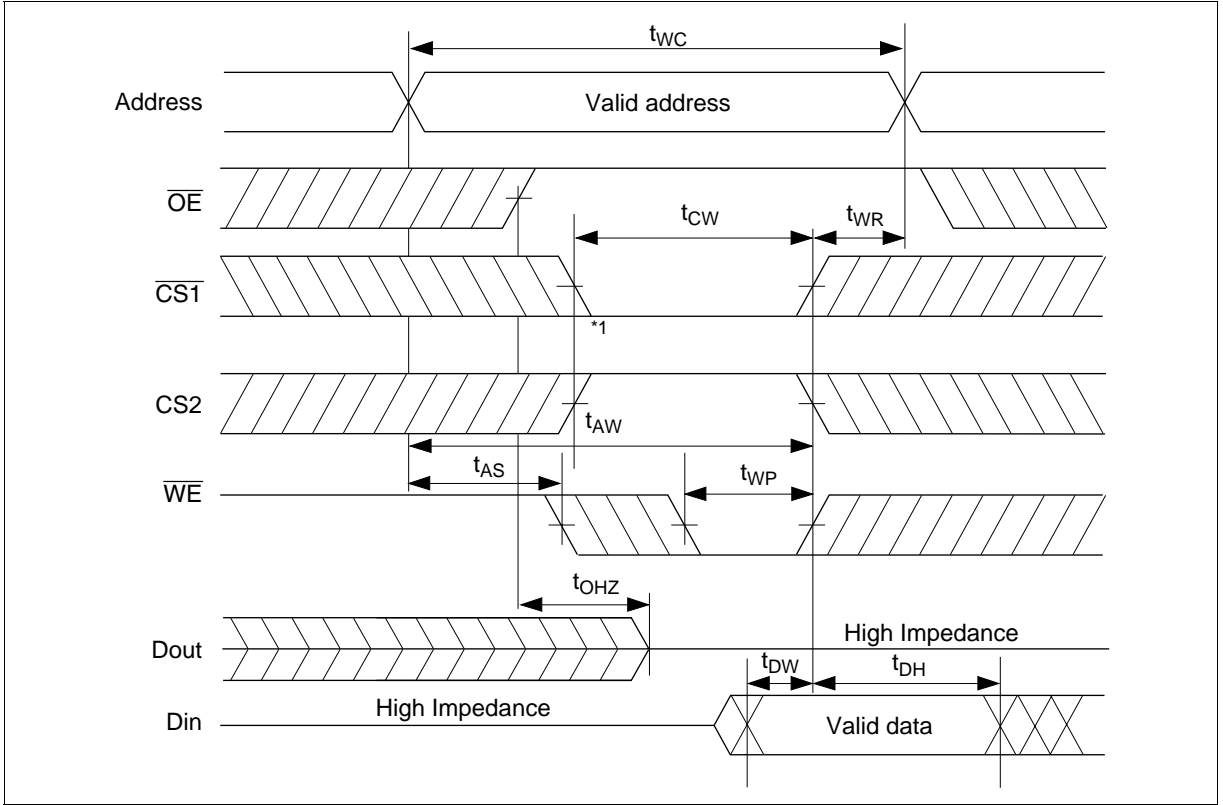
Write Cycle

Parameter	Symbol	HM6264BI-10		HM6264BI-12		Unit	Notes
		Min	Max	Min	Max		
Write cycle time	t_{WC}	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	80	—	85	—	ns	2
Address setup time	t_{AS}	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	80	—	85	—	ns	
Write pulse width	t_{WP}	60	—	70	—	ns	1, 9
Write recovery time	t_{WR}	0	—	0	—	ns	4
\overline{WE} to output in high-Z	t_{WHZ}	0	35	0	40	ns	5
Data to write time overlap	t_{DW}	40	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	
Output disable to output in high-Z	t_{OHZ}	0	35	0	40	ns	5

- Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, and high CS2, and a high \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high CS2 going low and \overline{WE} going high. Time t_{WP} is measured from the beginning of write to the end of write.
 2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
 3. t_{AS} is measured from the address valid to the beginning of write.
 4. t_{WR} is measured from the earliest of $\overline{CS1}$ or \overline{WE} going high or CS2 going low to the end of write cycle.
 5. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.
 6. If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low after \overline{WE} goes low, the outputs remain in high impedance state.
 7. Dout is the same phase of the written data in this write cycle.
 8. Dout is the read data of the next address
 9. In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention

$$t_{WP} \geq t_{WHZ} \max + t_{DW} \min.$$

Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



Low V_{CC} Data Retention Characteristics ($T_a = -40$ to $+85^\circ\text{C}$)

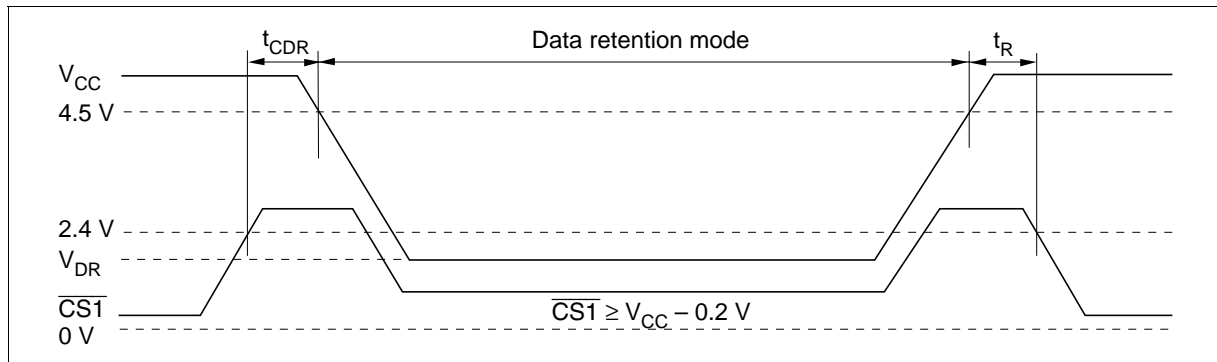
Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions* ³
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$ or $CS2 \leq 0.2 \text{ V}$ $V_{in} \geq 0 \text{ V}$
Data retention current	I_{CCDR}	—	1* ¹	100* ²	μA	$V_{CC} = 3.0 \text{ V}$, $0 \text{ V} \leq V_{in} \leq V_{CC}$ $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$ or $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Notes: 1. Reference data at $T_a = 25^\circ\text{C}$.

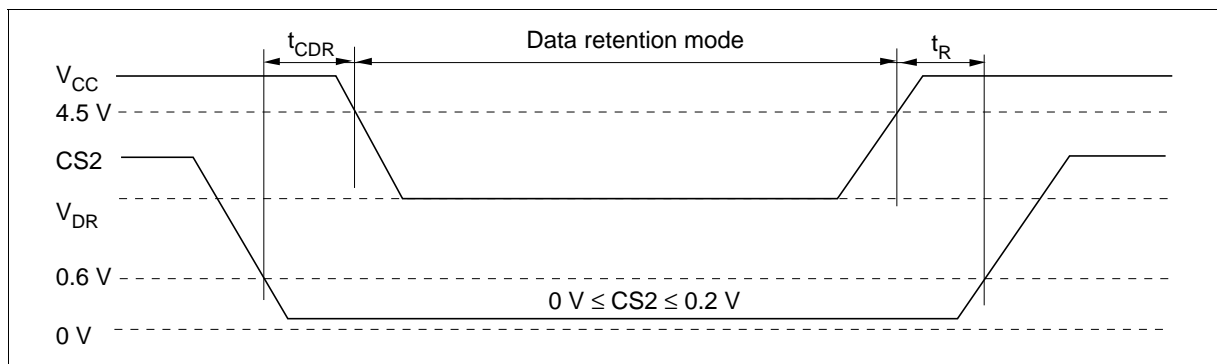
2. $10 \mu\text{A}$ max at $T_a = -40$ to $+40^\circ\text{C}$.

3. CS2 controls address buffer, \overline{WE} buffer, $\overline{CS1}$ buffer, \overline{OE} buffer, and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, \overline{WE} , \overline{OE} , $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2 \text{ V}$ or $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)

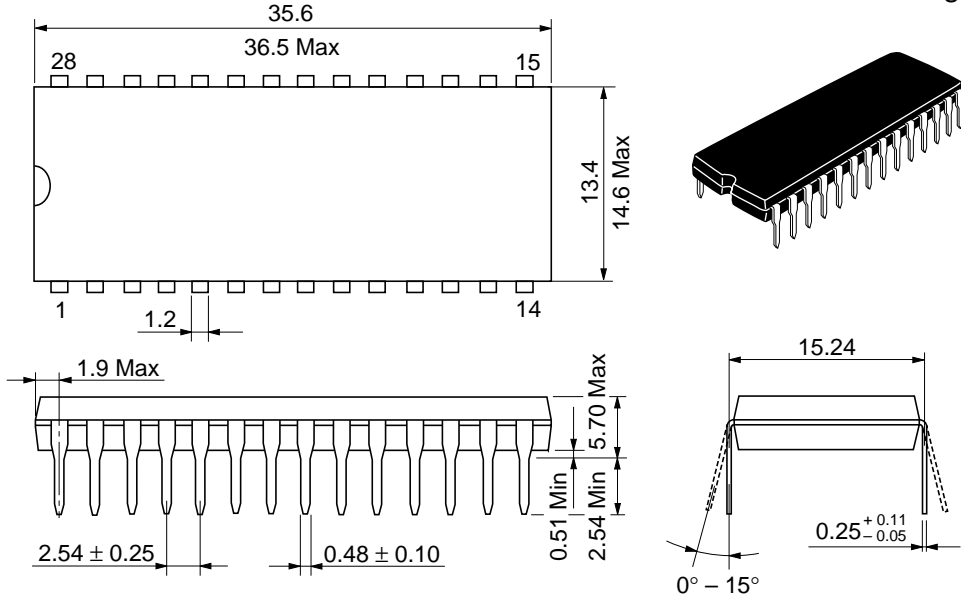


HM6264BI Series

Package Dimensions

HM6264BLPI Series (DP-28)

Unit: mm

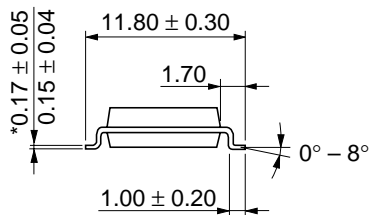
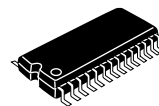
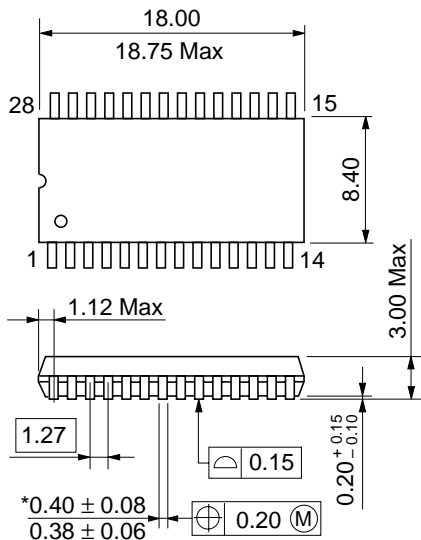


Hitachi Code	DP-28
JEDEC	—
EIAJ	Conforms
Weight (reference value)	4.6 g

Package Dimensions (cont.)

HM6264BLFPI Series (FP-28DA)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-28DA
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.82 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica : <http://semiconductor.hitachi.com/>
 Europe : <http://www.hitachi-eu.com/hel/ecg>
 Asia (Singapore) : <http://www.has.hitachi.com.sg/grp3/sicd/index.htm>
 Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
 Asia (HongKong) : <http://www.hitachi.com.hk/eng/bo/grp3/index.htm>
 Japan : <http://www.hitachi.co.jp/Sicd/index.htm>

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Copyright © Hitachi, Ltd., 1998. All rights reserved. Printed in Japan.

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Dec. 1, 1995	Initial issue	I. Ogiwara	K. Yoshizaki
1.0	Sep. 5, 1996	Deletion of Preliminary	I. Ogiwara	K. Imato
2.0	Feb. 9, 1998	Change of subtitle Change of FP-28DA	I. Ogiwara	K. Imato
3.0	May. 8, 2000	Low V_{CC} Data Retention Characteristics Note 2: V_{IL} min = -0.3 V to 10 μ A max at $T_a = -40$ to $+40^\circ\text{C}$		
