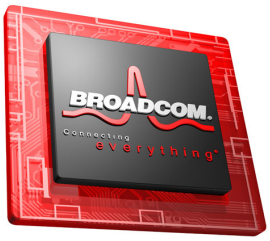
BROADCOM®
Connecting everything®

BCM8152 PRODUCT Brief



10 GBPS TRANSCEIVER WITH 10G CLOCK, BUS SKEW, AND LIMITING AMPLIFIER

FEATURES

- 10-Gigabit MSA (Multi-Source Agreement) compatible
- Fully integrated multi-rate CDR, DEMUX, CMU, and MUX
- 16-bit LVDS interface
- 10-gigabit serial transmitter clock output
- Limiting amplifier
- On-chip PLL-based clock generator
- Line and system loopback modes
- Receiver and transmitter serial data polarity invert
- Bit order reversal
- Analog loss-of-signal output (ALOSB) and input (LOSIB)
- Tx and Rx lock detect
- 10-word FIFO with overflow alarm absorbs system clock jitter
- Reference clock: 1/16 or 1/64 of the selectable data rate
- Selectable Rx clock and Rx data squelch upon ALOSB
- Selectable loop timing mode
- Internal phase detector and charge pump for cleanup PLL, external VCXO required
- Power supplies: core, LVPECL, LVDS output, and CML at 1.8V, LVDS input and CMOS I/O at 1.8 or 3.3V
- Power dissipation: 1.2W typical

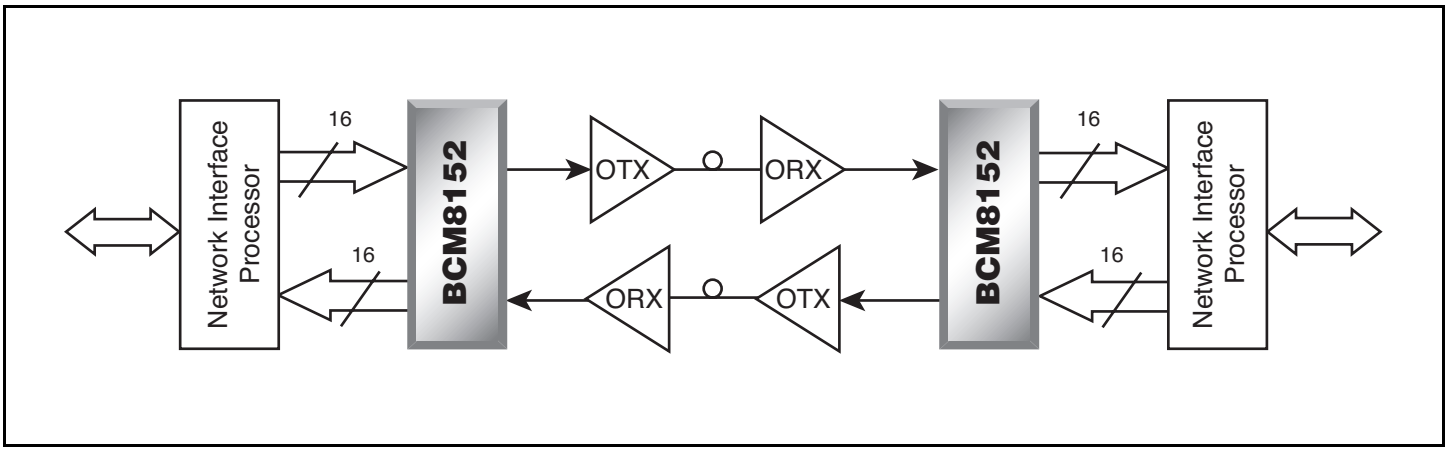
SUMMARY OF BENEFITS

- Provides compliance Optical Internetworking Forum (OIF), Telcordia, ITU-T, and IEEE 802.3ae standards.
- Reduces design cycle and time to market.
- High level of integration allows for higher port density solutions.
- Uses the most effective silicon economy of scale for CMOS-based devices.
- Standard CMOS fabrication process.

APPLICATIONS

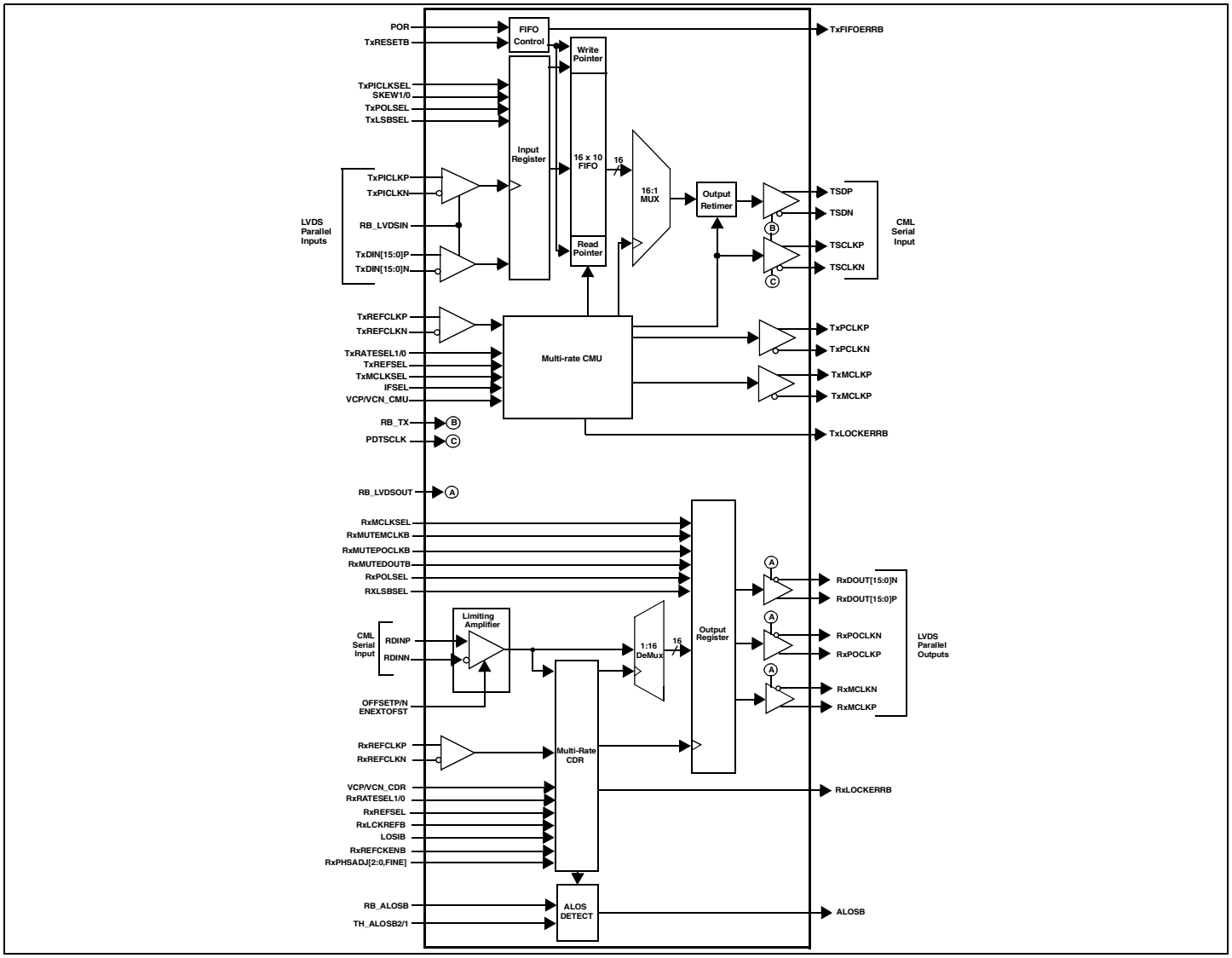
- OC-192/STM-64/10 GE/FEC transmission equipment
- SONET/SDH/10 GE/FEC optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbone
- SONET/SDH/10 GE/FEC test equipment
- Terabit and edge routers

BCM8152 Functional Block Diagram



BROADCOM

OVERVIEW



The **BCM8152** is a fully integrated MSA-compatible multi-rate SONET/SDH/10GE/FEC transceiver operating at the OC-192/STM-64 (9.953 Gbps), 10GE (10.3125 Gbps), 10GFC (10.315 Gbps), or one of three FEC (Forward Error Correction) (10.664/10.709, 11.096, or 11.31 Gbps) data rates with serializer, deserializer, integrated clock multiplication unit (CMU), 10G clock, bus skew, limiting amplifier, data recovery circuit (CDR), and enhanced feature set. On-chip clock synthesis is performed by the high-frequency, low-jitter phase-locked loop (PLL) on the **BCM8152** transceiver chip allowing the use of a low-frequency reference clock selectable to the line rate divided by either 16 or 64.

Clock recovery is performed on the device by synchronizing its on-chip voltage-controlled oscillator (VCO) directly to the incoming data stream. An on-chip phase detector and charge pump plus external VCXO implements a cleanup PLL. The cleanup PLL can be used to clean up the CDR recovered clock for loop timing applications or to clean up a noisy system clock.

The low-jitter LVDS interface guarantees compliance with the bit error rate requirements of the Telcordia, ANSI, ITU-T, and IEEE 802.3ae standards.

The **BCM8152** is packaged in a 15 x 15 mm, 301-pin BGA.

Connecting everything®

BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

8152-PB02-R 04/23/04

Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com